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Solving Digital Circuit Layout Problem based on Graph Partitioning Technique: A Glance

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***Abstract*—Digital Circuit Layout is a combinatorial optimization problem. Due to the complexity of integrated circuits, the first step in physical design is usually to divide a design into subdesigns. The work presents a brief survey of major contributions to solve digital circuit layout problem using graph partitioning technique by dividing the study into three parts: Basic inspiration, Graph Partitioning related preliminary work and role of evolutionary approaches in solving digital circuit layout problem. The study analyses the work of major contributors and concludes the findings.**

***Index Terms*—Partitioning, Min-cut, NP hard, Evolutionary approach**

I. INTRODUCTION

The exponential increase in the size of digital circuit, reduction in chip size and heterogeneity of circuit elements used in modern chips lead to an increase in the complexity of modern digital circuit layout and design of algorithms [1]. Due to the complexity of integrated circuits, the first step in physical design is usually to divide a design into subdesigns. Considerations include area, logic functionality, and interconnections between subdesigns. The complexity of the digital electronic circuit is due to the number of gates used per system as well as the interconnection of the gates. Reduction of the total number of gates used and interconnection in the system would reduce the cost of the design, as well as increase the efficiency of the overall system. The future growth of digital circuits depends critically on the research and development of Circuit Layout automation tools [2].

II. THE PROBLEM IN HAND

The digital circuit layout problem is a constrained optimization problem in the combinatorial sense. Given a circuit represented by net list [3], set of modules, its dimensions, set of pins, the layout problem seeks an assignment of geometric coordinates of the circuit components that satisfies the requirements of the fabrication technology (sufficient wire spacing , restricted number of wiring layers etc.) and that minimizes certain cost criteria .
Practically, all aspects of the layout problem as a whole are intractable; that is, they are NP-hard. Consequently, the alternate is to exploit the heuristic methods to solve very large problems. One of these methods is to break up the problem into sub problems, which are then solved one after the other. Almost always, these sub problems are NP-hard too, but they are more amenable to heuristic solutions than is the entire layout problem itself [4]. Each one of the layout sub problems is decomposed in an analogous fashion. In this way, the procedure is repeated to break up the optimization problems until reaching primitive sub problems. These sub problems are not decomposed further, but rather solved directly, either optimally if an efficient polynomial-time optimization algorithm exists or approximately if the sub problem is itself NP-hard or intractable
Circuit layout is an important part of the digital circuit design process .The input to the circuit layout design cycle is a circuit diagram and the output is the layout of the circuit [5]. This is accomplished in several stages such as partitioning, floorplanning, placement and routing.

III. DESIGN COMPLEXITY IN DIGITAL CIRCUIT LAYOUT

Optimal graph bipartitioning with the edge cut objective is an NP complete problem. Similarly, optimal hypergraph bipartitioning and multi-way partitioning are NP complete problems, which suggest that polynomial time algorithms for these are also unlikely to exist. Some practical consequences of this fact are that the number of problem solutions grows exponentially with the problem size and that there may be multiple optimal solutions .The reality that problem sizes are prohibitively large imposes fairly strict criteria on possible approximation algorithms: the run time complexity should be linear or log linear with the size of the problem. At any level of partitioning, the input to the partitioning algorithm is a set of components and a net list. The output is a set of subcircuits which after connected, function as the original circuit and terminals required for each sub circuit to connect it to the other subcircuits. Other than maintaining the original functionality, the partitioning process optimizes certain parameters subject to certain constraints. The objective functions for a partitioning problem include the minimization of the number of nets that cross the boundaries of partition, and the minimization of the maximum number of times a path crosses the partition boundaries [6]. The constraints for the partitioning problem include area constraints and terminal constraints. The constraints and the objective functions used in the partitioning problem vary depending upon the design style and the partitioning level used. The actual objective function and constraints chosen for the partitioning problem may also depend on the specific problem.

IV. LITERATURE SURVEY

The general graph partitioning problem is NP-complete, approximate methods constitute a natural and useful approach to address this problem. In the past several decades, this

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problem inspired a great number of methods and heuristics such as greedy algorithms, spectral methods, multilevel approaches, as well as algorithms based on well-known metaheuristics like tabu search, ant colony, simulated annealing, genetic and memetic algorithms. Iterative improvement methods produce high quality partitions, but excessive computation time is required to do so. On the other hand, constructive methods yield not as high quality partitions as iterative improvement methods, yet good, in a much shorter time. Ideally, both quality and computational efficiency of the solution are crucial for a practical partition method. Quality of solution is important for performance of the circuit and computational efficiency is essential for curtailing the design procedure, especially for large circuits where weeks, months or even years may be required to realize these circuits. The fact that future partition and routing tasks will be much more complicated due to the increasing size of the circuits and the growing design objectives implies that faster partition and routing tools should be developed to handle such immense complexity.

Some metaheuristics have already been used to partition graphs, like genetic algorithms [49, 50] or ant-like agents [7]. Therefore, for all of these tools, we are looking for a near optimal partition in reasonable time. Because minimum cut algorithms were well studied [8, 9, 52], most partitioning methods use recursive bisections. But these methods often provide a partition which is far from optimal [53], regarding the minimization of the sum of the weight of edge cuts. Conversely, spectral graph partitioning methods [54, 55] and multilevel partitioning algorithms [56] produce good partitions. The most widely used heuristic like Kernighan –Lin algorithm [8] and Fiduccia-Mattheyses algorithm [9] are not very suitable for solving real VLSI partitioning problems-their performance is strongly dependent on the starting point and they are unable to handle any additional constraints in an efficient way. In such a case evolutionary algorithms (EAs) seem to be a promising alternative as they have already turned out to be powerful tools for solving hard combinatorial problems (eg. [7]).A few EA based approaches to VLSI circuit partitioning have been described in the literature [10, 54].

A. Analysis of various approaches

The literature review has been classified into three major categories

- The basic inspiration
- graph partitioning related preliminary work
- evolutionary approaches for digital circuit layout

The work initiated with basic inspiration from B. W. Kernighan and S. Lin[8] in the early 1970s .The authors proposed KL heuristic for graph bipartitioning. D. G. Schweikert and B. W. Kernighan, in 1972[11] extended the work for hypergraph model in the Kernighan–Lin partitioning heuristic. For both of these approaches the complexity of the algorithms was too high even for moderate size problems. The performance of the Kernighan–Lin algorithm largely depends on the quality of the bisection that it starts with. The algorithms produce poor partitions for larger hypergraphs. L.Hagen,et al. [12] proposed FM algorithm in which vertices removed and inserted from the bucket list using a last-in-first-out (LIFO) scheme .B. Krishnamurty,[13] extended FM algorithm using look-ahead scheme for circuit bipartitioning. FM algorithm was able to provide satisfactory solutions only for smaller to medium size problems .The approach produced poor partitions for larger hypergraphs and the results depend on the quality of the initial partitions that it starts with.

In graph related preliminary work, Sanchis in year 1989[14] extended the FM concept to deal with multiway partitioning producing better quality than KL but at the expense of increased runtime.. Johnson et al., [15] used simulated annealing for graph partitioning producing smaller netcuts than iterative methods, albeit with much greater runtimes. S.W. Hadley and B.L. Mark[16] generated initial partitions based on eigen vector decomposition. The approach required transformation of every multi-terminal net into two terminal nets which could result in a loss of information needed for a performance based partitioning. Bultan and Aykanat [17] used meanfield annealing for multi way partitioning algorithm at the cost of greater runtimes. Cong.J, W. labio and N. Sivakumar,(1994) proposed k-way net based multi way partitioning algorithm, producing better quality solutions than the FM algorithm but only for smaller size problems[18]. Yang and Wong,[19] used maximum flow problem which has is no constraint on the sizes of the resulting subsets.Vipin Kumar, et.al.(1999) used multilevel clustering approach (hMetis)[63].The approach provided poor flexibility and objective functions for clustering were difficult to formulate. The approach was less efficient with larger size integrated circuits. Jong-Sheng Cherng and Sao-Jie Chen,[20] work was based on the Multilevel flat partitioning .In the year 2002, Drechsler[21] used recursive partitioning. The increasing recursion depth lead to investment of more run time. Mardhana[22] used neural network to solve the partitioning problem. The results depend on moves generated by a neural network.

In 1987, Ackley started with the evolutionary approach for solving digital circuit layout problem based on graph partitioning technique [51]. The author used GA for min cut bisection problem. Saab and Rao [23] proposed simulated evolution bisection heuristic. Chatterjee and Hartley [24] proposed a simulated annealing based heuristic which performed partitioning and placement simultaneously. The heuristic has no crossover operator. Chandrasekharam et al.[25] proposed a stochastic search by a genetic algorithm (GA).Areibi and Vannelli [26] combined tabu search and genetic algorithm for hypergraph partitioning problem. Alpert et al. [27] integrated the Metis into a genetic algorithm for graph partitioning. Langham and Grant used Ant Foraging Strategy (AFS) for graph partitioning [58]. Merz and Freisleben[28] used a memetic algorithm for graph bipartitioning problem. Kim and Moon [29] proposed a hybrid genetic algorithm for multiway graph partitioning .Cincotti et al. proposed an order-based encoding to evaluate a partitioning of vertices represented by this encoding, taking a long time for the decoding process[59]. Muhlenbein and Mahnig (2002) presented a theory of population based optimization methods using approximations of search

distributions. Kohmoto et al. (2003) incorporated a simple local search algorithm into the GA[64] .Sait.S.M et.al. proposed memetic algorithm based on Genetic Algorithm (GA) and Tabu search [60]. Kim et al. (2004) proposed a combination of a genetic algorithm with an FM-based heuristic for hypergraph bipartitioning. Kucukpetek et al. [30] presented a genetic algorithm for the coarsening phase of a multilevel scheme for graph partitioning. Ganesh et al. [31] presented a swarm intelligence based approach to the circuit-partitioning problem Martin [32] proposed GAs technique as the singular value decomposition (SVD), This spectral technique has high running time and is suitable where the fitness function is expensive to compute Sun and Leng [33]) presented an effective multi-level algorithm based on simulated annealing for bisecting graph. Moraglio et al. [34] provided a new geometric crossover for graph partitioning based on a labelling-independent distance that filters out the redundancy of the encoding. Coe et al. [35] investigated the implementation of a Memetic algorithm for VLSI circuit partitioning by exploiting parallelism and pipelining .Datta et al. [36] proposed a multi-objective evolutionary algorithm (MOEA) for solving the graph partitioning problem. Leng et al. [37] proposed an effective multi-level algorithm for bisecting graph based on ant colony optimization (ACO). Farshbaf and Derakhshi (2009) proposed a multi-objective GA method to optimize the graph partitioning [61]. Armstrong et al. [38] presented six different parallel Memetic Algorithms for solving the circuit partitioning problem..Subbaraj et al. [39], presented an efficient hybrid Genetic Algorithm (GA) incorporating the Taguchi method as a local search mechanism to solve both bipartitioning and recursive partitioning. Peng et al. [40]A multi-objective discrete PSO (DPSO) algorithm for VLSI partitioning Soliman et al. [41] gave an ant Model (SCAM) to solve graph partitioning problem. Chen and Wang (2011), presented an efficient genetic algorithm to solve m-way graph partitioning problem. Galinier et al. [43] proposed a memetic algorithm, which used both a tabu operator and a specialized crossover operator. Kim et al.[44] discussed a number of problem-specific issues in applying genetic algorithms to the graph partitioning problem Kurejchik and Kazharov[45] described the block diagram of swarm intelligence as a graph or hypergraph Lee et al. [46] offered a novel Memetic Quantum-Inspired Evolutionary Algorithm (MQEA) framework. Shanavas & Gnanamurthy [47] presented a memetic algorithm which hybrids Genetic Algorithm and Simulated Annealing to solve the graph partitioning.

B. Findings for evolutionary approaches for digital circuit layout problem

Non- hybrid approaches:

- ill occupied to search a prescribed region of the solution space for local optima., may take fairly long to find a good solution

Both Non- hybrid approaches & hybrid approaches: Their effectiveness is greatly dependent on

- the representation of the solution space
- initial population chosen
- Crossover method used,
- Population size used
- Hybrid variants.
- Produced quality solutions for small sized circuits

While going through the literature survey of various evolutionary approaches genetic algorithm, memetic algorithm, Ant based Optimization, Particle swarm intelligence, following gaps have been traced.

- Many of the surveyed evolutionary algorithms are competitive with respect to the solution quality only. However to be of interest in the VLSI design area, a measure of running time must also be included. Whenever possible, the presented approach should be compared with state-of-the art algorithms regarding both the solution quality and run time.
- Constraints of the other algorithms have to be taken into account, when comparing with their results. For example it is not a fair comparison when the routing quality of an evolutionary algorithm is expressed only in terms of number of vias [62]and then compared with the results of other approaches that minimize the net length concurrently.
- Due to the large number of CAD tools in VLSI design, benchmarks data are available for all major design steps, eg.,[EDA Benchmarks (1997)].An evolutionary algorithm developed for VLSI design will not create any interest within the VLSI community unless its performance is tested with the appropriate benchmarks. It is only by examining the results of these benchmarks that we can compare a particular evolutionary algorithm with any other given approach. These test examples should be large, reflecting real-world VLSI design problems.
- Major work in literature has been focused on using genetic algorithm for circuit partitioning. Less attention has been paid on rest of evolutionary approaches.

V. CONCLUSION

Digital circuit layout is an NP hard problem. The alternate is to exploit the heuristic methods to solve very large problems. One of these methods is to break up the problem into sub problems, which are then solved one after the other. Almost always, these sub problems are NP-hard too, but they are more amenable to heuristic solutions than is the entire layout problem itself. The paper presents a brief study of various graph partitioning approaches in the context of digital circuit layout and extracts use of evolutionary approaches and their research gaps in solving digital circuit layout based on graph partitioning.

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