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Design and implementation of low power 16 bit ALU with clock gating

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***Abstract*—The ALU is one of the most frequently accessed modules in a CPU and is utilized during most instruction executions. Hence the power consumption of the ALU is a major concern.In this paper a low power 16 bit ALU is designed using VHDL. Lower power consumption is achieved by using clock gating technique and the results are compared with conventional ALU design. A carry skip adder with variable block length is used for the arithmetic unit to achieve better performance. The design is then implemented inXilinx Spartan 3E FPGA . The ALU achieves a maximum frequency of 65.19 MHzwith a dynamic power dissipation of 1.98mW when operated at 15 MHz.**

***Index Terms*— ALU, clock gating, CPU,CMOS,FPGA, MOSFET, Spartan3E, VHDL**

I. INTRODUCTION

THE OPTIMIZATION for lower power dissipation and faster device performance is of prime concern. The ideal design is one which consumes minimum power, requires minimum area but has the highest throughput. However, these parameters are often contradictory and a suitable solution has to be formulated to maintain a tradeoff between these parameters. Power optimization is possible at every level of digital design flow, however, benefits are maximum at the algorithmic and architectural design level.

Modern day microprocessors are designed to operate at maximum speed but consume minimum power at the same time. This is necessary to improve battery life of portable systems, improve reliability and reduce heat removal costs. The ALU, being one of the most computationally intensive modules in a CPU almost always falls in the datapath during the execution of an instruction. Hence the power consumption of the ALU should be kept at a minimum.

In this paper a 16 bit ALU is designed in VHDL and clock gating technique is used to lower power consumption. A carry skip adder with variable block length is used as the primary computational element of the arithmetic unit. The design is then simulated in ISim simulator and finally implemented in Xilinx Spartan 3E FPGA. The results are compared with that of a conventional ALU which revealed significant improved performance of the clock gated ALU over the conventional design.

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II. SOURCES OF POWER DISSIPATION

A. Dynamic power dissipation

Dynamic power dissipation of CMOS circuit has two parts- dynamic switching power and short-circuit current power [4]. Dynamic switching power is dissipated every time the logic state of the gate changes. It is represented as $P = nfC_L Vdd^2$, where f is the frequency of switching,$C_L$is the load capacitance,Vdd is supply voltage and n is the probability of switching. This power can be reduced by lowering switching frequency;however it is not desirable as it limits the speed of operation of the device. n can be reduced by reducing redundant switching activity. Vdd can also be reduced, however it leads to increased propagation delays and hence not desirable. Hence a proper tradeoff must be met between these parameters to obtain satisfactory device performance.

Short circuit current power is dissipated when both the NMOS and CMOS MOSFETs are partially on, during a switching activity. In this case a direct short circuit path is momentarily formed between power supply and ground, leading to significant power dissipation. This can be controlled by regulating the slew rate and applying sharp clock edges. However, generating such a clock is difficult.

B. Static power dissipation

Static or quiescent power dissipation is independent of the switching activity of the circuit. This is caused due to leakage current in the device during steady state. Sub-threshold conduction is the reason for this power dissipation and can be controlled by biasing the MOSFETs well below their threshold voltages and using multiple threshold CMOS designs.

III. CLOCK GATING

Clock power constitutes a significant portion of dynamic power. In a synchronous circuit several modules are clocked at the same time. However, at any particular instant only a single module may be functional. Hence, unnecessary clocking of the other modules lead to a lot of power dissipation. Clock gating technique is a power down methodology, which involves selectively clocking modules as and when required while keeping other inactive modules in sleep mode. Thus the power dissipation due to charging

and discharging of the clock at unused gates, is avoided in this strategy.

Clock gating is achieved by ANDingthe clock signal with a control signal to form a gated clock, which is then applied to different components of the circuit. To which module the gated clock should be applied is decided based on the control signal.

IV. DESIGNING THE 16 BIT ALU

In this paper the above clock gating technique is used to achieve low power dissipation. The ALU is composed of a clock gating circuit, an arithmetic unit, a logic unit and an output multiplexer [1]. Data is loaded into the arithmetic and logic units through input registers and the output is delivered to an output registers. Loading and unloading of data in the registers are controlled by gated clocks from the clock gating circuit.

A. Arithmetic unit

The arithmetic unit is designed to perform four operations - addition, subtraction, increment and decrement [2]. The core of the arithmetic unit is a variable block length carry skip adder. The maximum combinational path delay(pad to pad) from carry input to carry output has been found to be 22.005 ns which is almost same as that of a ripple carry adder, however, the power dissipation is a little lower than the ripple carry adder [3]. The effect of using carry skip adder with variable block length to minimize carry propagation delay is more pronounced for higher number of bits.

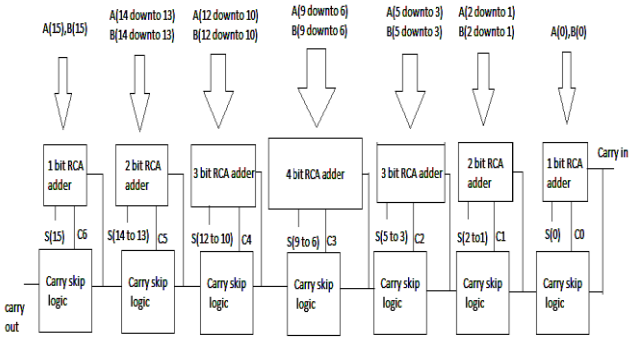

Fig.1. Structure of variable block length carry skip adder

Each individual block is a ripple carry adder. The carry generated in each block enters the ripple carry logic along with the carry generated in previous block. A bitwise XOR operation between the operands is done in the skip logic block and the results are ANDed together to form the propagation bit given by $((A_i \text{ XOR } B_i).(A_{i+1} \text{ XOR } B_{i+1})\ldots(A_m \text{ XOR } B_m))$, where m is the block length. If propagation bit is 1, it indicates no carry has been generated in the block and the previous carry input is sent directly to the next block. If the propagation bit is 0, a carry has been generated or killed in the block and this is sent to the next block. Variable block length gives better performance in terms of delay with almost 40 percent faster operation than fixed block design.

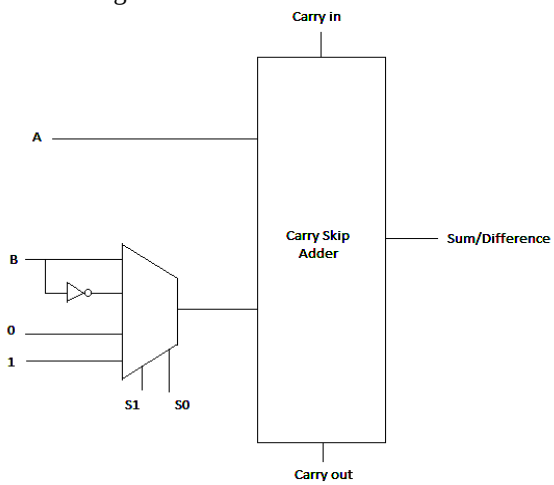

Fig.2. Architecture of the Arithmetic Unit

The 16 bit operand A is applied directly to the Carry skip adder. The operand B goes through a multiplexer and is selected based on select inputs S1 and S0. The nature of the output is based on the signals S0, S1 and carry input. The arithmetic unit can perform seven exclusive operations. The entry of input operands A and B are controlled through registers clocked by the gated clock from the clock gating circuit. Hence, the arithmetic unit is brought into operation only when required and remains inactive during other operations of ALU.

TABLE I
OPERATIONS PERFORMED IN THE ARITHMETIC UNIT BASED ON S1, S0 AND CARRY IN.

S1	S0	Carry in	OPERATION
0	0	0	A+B
0	0	1	A+B+1
0	1	0	A+(not B)
0	1	1	A-B
1	0	0	A
1	0	1	A+1
1	1	0	A-1
1	1	1	A

B. Logic Unit

The operands A and B enter the logic unit through registers controlled by the gated clock, like the arithmetic unit, giving it exclusivity of operation only when required by the ALU.

The logic unit can perform four operations based on the select inputs S0 and S1.

TABLE II
OPERATIONS PERFORMED IN LOGIC UNIT BASED ON S0 AND S1 SELECT INPUTS

S1	S0	OPERATION
0	0	A AND B
0	1	A XOR B
1	0	A OR B
1	1	NOT B

V. SIMULATION AND IMPLEMENTATION

C. Clock gating circuit

The clock gating circuit takes in the clock input and generates a gated clock based on a control signal S2. The gated clock signal is used to activate the arithmetic or logic unit. Preventing unnecessary charging and discharging of the clock signal in inactive modules leads to lower dynamic power dissipation.

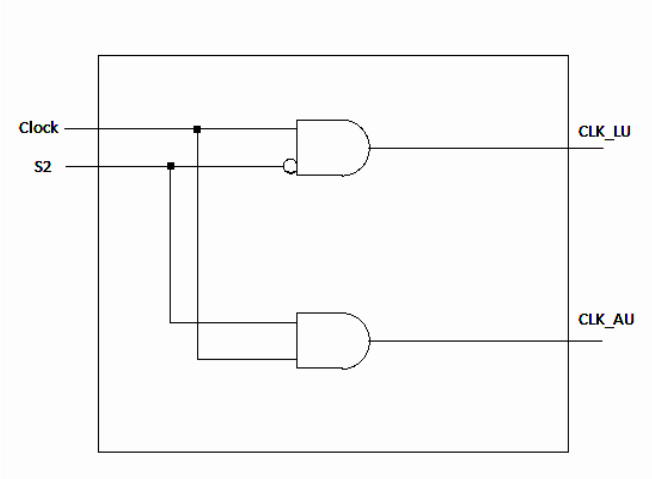

Fig.3.Clock gating circuit with clock and control signal input and gated clock outputs

The master clock input is fed to the circuit . When control signal input S2 is zero, clock is gated through first AND gate to the Logic unit. When S2 is one, clock is gated through second AND gate to Arithmetic unit. Thus, at a time only one gated clock output is active.

TABLE III
SIGNAL S2 ACTIVATING DIFFERENT UNITS OF ALU

S2	ACTIVATION
0	Logic Unit
1	Arithmetic Unit

D. Output multiplexer and register

The computed outputs from the arithmetic and logic units are fed into the output multiplexer. The proper output is selected based on a control signal. This output is then sent to the output register which is clocked by either of the two gated clocks.

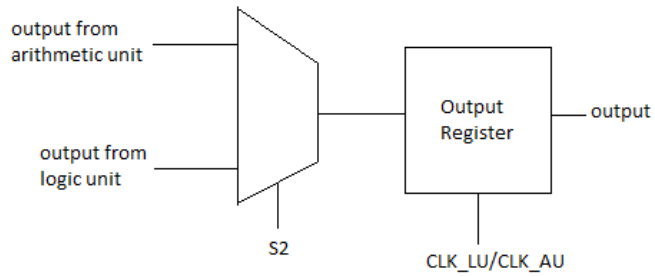

Fig. 4.Structure of output register and multiplexer

When S2 is zero, the multiplexer output is taken from the logic unit and when S2 is one the output is taken from the arithmetic unit. The selected output is delivered via the output register clocked by either of the gated clocks.

The above modules are designed in VHDL using Xilinx ISE 13.4 design suite. The behavioral simulation is done using ISim simulator with a clock period of 1 us. After this the design was synthesized for the target device. Finally the design was implemented through translate, map and place and route stage.

A. Simulation waveforms

The simulations are performed with a 1 us clock period using ISim Simulator.

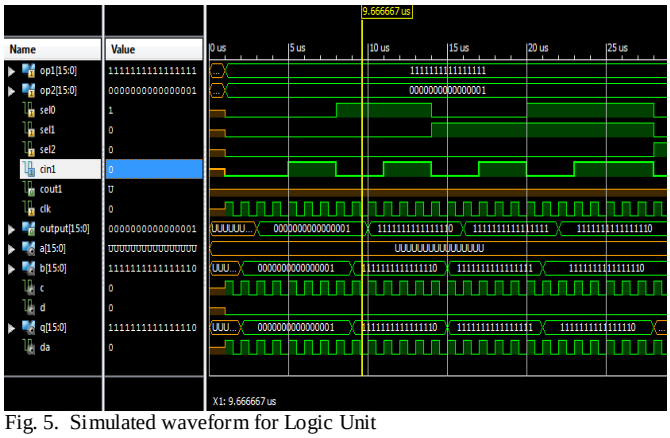

Fig. 5. Simulated waveform for Logic Unit

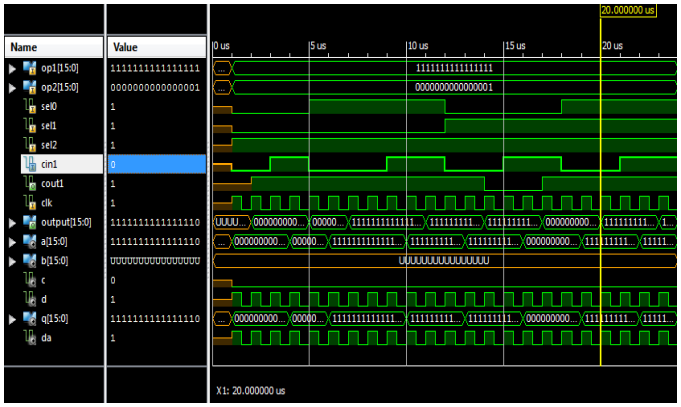

Fig. 6. Simulated waveform for Arithmetic Unit

B. RTL Schematic

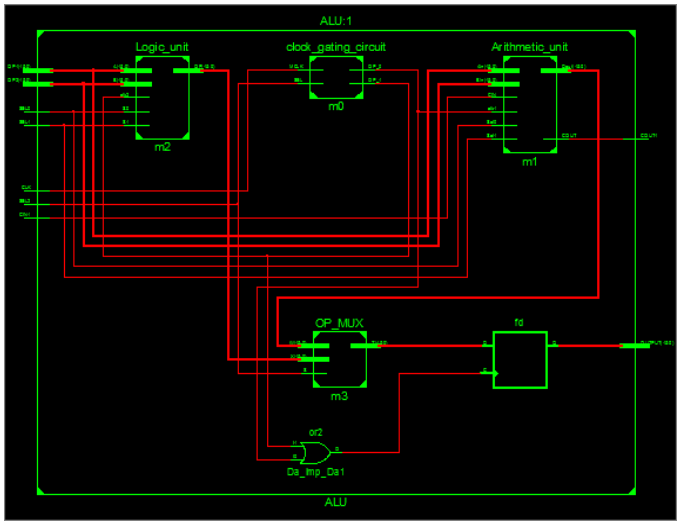

Fig.7.Register transfer Level schematic of the ALU

C. Technology Schematic

The technology schematic exhibits the design based on the logic elements of the target technology, in this case the FPGA[6]. The circuit is represented using Lookup tables, multiplexers and flipflops. The input and output pins are driven through input/output buffers and the clock is driven through a clock buffer.

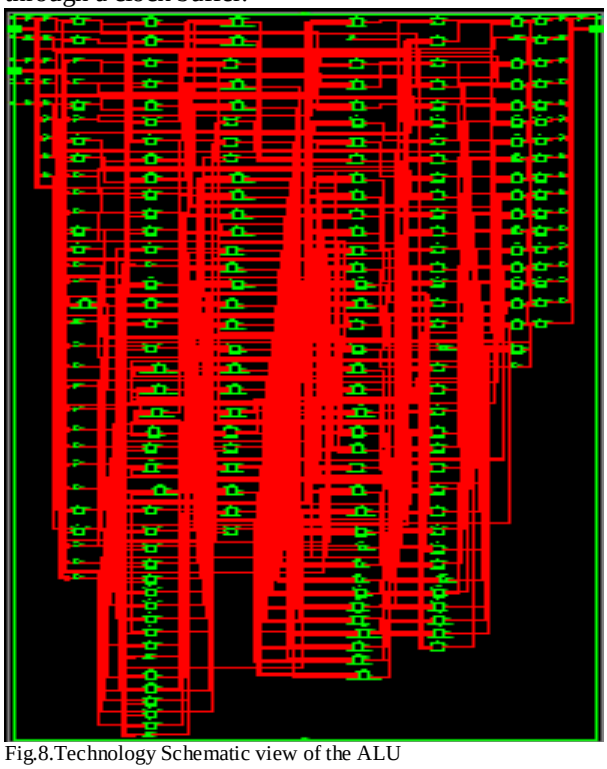

Fig.8.Technology Schematic view of the ALU

D. Experimental Results

After synthesis, the design is implemented in the spartan3E FPGA. The synthesized netlist is translated, mapped in the device and finally routed. The maximum frequency of operation is obtained from the post place and route timing report [5].

TABLE IV
DEVICE STATISTICS FOR THE IMPLEMENTED ALU

Maximum Frequency	65.19 MHz
Total Number of 4 input LUT	107
Number of bonded IOBs	54
Number of occupied Slices	94

The power consumption of the ALU is analyzed using XilinxXpowerAnalyser. A comparative analysis has been done between the clock gated ALU and the conventional ALU. The test is done at a supply voltage of 2.4 V and 15 MHz clock frequency. The output load is of 5 pF.

TABLE V
POWER CONSUMPTION OF ALU WITH AND WITHOUT CLOCK GATING

	DYNAMIC POWER(mW)	**QUIESCENT POWER(mW)**
ALU Without Clock Gating	5.96	51
ALU With Clock Gating	1.98	51

The dynamic power consisted of clock domain power, Logic power, signal power and power consumed by I/O buffers. It is observed that the dynamic power consumption of clock gated ALU is considerably less than without clock gating.

The quiescent power is the static power dissipated in the FPGA when it is turned on. It is a function of supply voltage, junction temperature and device family. Power gating can be used to reduce leakage current which causes static power dissipation in the device.

VI. CONCLUSION

Power consumption in modern devices are a growing concern as demands for increased battery life, lower heat dissipation and increased device reliability is on the rise. In this paper the power optimization at architectural level is demonstrated by the design of a 16 bit ALU using clock gating. It is observed that clock gating reduces dynamic power dissipation of the ALU by approximately 66.7 percent. The arithmetic unit of the ALU is based on a carry skip adder to reduce carry propagation delays and its performance increases for higher number of bits. The ALU is capable of performing eleven operations and can be readily placed in the datapath of a 16 bit microprocessor.

REFERENCES

[1] M. Morris Mano, "Register transfer and Microoperations," in *Computer System Architecture*, 3rd ed. Pearson, India, pp. 106-118.
[2] S. Salivahanan and S. Arvazhagan, "Digital Circuits and Design", 3rd ed. Vikas publishing, India, pp. 168-169.
[3] R.Uma and P.Dhavachelvan (2012, August). Logic optimization using technology independent MUX based adders in FPGA.*International Journal of VLSI design & Communication Systems*.[online].*3 (4)*, pp. 135-147.
Available: http://airccse.org/journal/vlsi/papers/3412vlsics12.pdf
[4] KanikaKaur and Arti Noor (2011,May). Strategies and Methodologies for low power VLSI designs: A review. *International Journal of Advances in Engineering & Technology*.[online]. ISSN: 2231-1963. pp. 159-164. Available: http://www.ijaet.org/media/18STRATEGIES-METHODOLOGIES-FOR-LOW-POWER-VLSI-DESIGNS-A-REVIEW-Copyright-IJAET.pdf.
[5] Rajeev Kumar (2012, June).Design & Implementation of 64 bit ALU for Instruction Set Architecture & Comparison between Speed/Power Consumption on FPGA.*International Journal of Advanced Research in Computer Engineering & Technology*.[online]. 1(4), pp.186-192. Available: http://ijarcet.org/index.php/ijarcet/article/view/132/PDF.
[6] Xilinx XST user guide, UG627 (v 12.4), 2010.

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