ISSN: 2278 – 1323
International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)
Volume 2, Issue 6, June 2013

Analysis of Sleep Mode Energy Consumption in CMOS Circuits Using Power Gating Switches

R.Aishwarya[1], S.P.Valan Arasu[2]

[1]PG Student, Dr. Sivanthi Aditanar College of Engineering,

[2]Assistant professor (SG), Dr. Sivanthi Aditanar College of Engineering,

Tiruchendur -628215, India

***Abstract*- As the electronic devices such as computers, mobile phones etc. are shrinking in size and are becoming easily portable, power dissipated by the device gets increased. To reduce the total energy consumption of CMOS circuits, the sleep mode energy has to be calculated and analyzed. Because in many applications, the processor and the peripherals does not run continuously and spend most of the time in sleep mode or low power mode. The proposed work is to analyze the sleep mode energy consumption of a 8-bit Arithmetic and Logic Unit (ALU) circuit with and without Power Gating Switches (PGS). Power-gating refers to switching off the power supply for a portion of the circuit completely, resulting in total elimination of power consumption for that part. The simulation of the proposed ALU circuit is performed in LTSPICE IV and DSCH software and the reduction in energy consumption has been analysed. The area requirements of the proposed ALU is analysed using Microwind by creating a layout.**

***Index Terms*- Arithmetic and Logic Unit (ALU), Leakage current, Power Gating Switch (PGS), Sleep energy.**

I. INTRODUCTION

For a CMOS circuit, the total power dissipation includes dynamic and static power dissipation during the active mode of operation. In the standby mode, the power dissipation is due to the leakage current. Voltage scaling is an effective method to reduce power dissipation due to the quadratic relationship between switching energy and supply voltage. Therefore, dynamic voltage scaling (DVS) has been used in microprocessors to scale down the supply voltage, thereby saving a significant amount of energy. But it results in increased delay in the circuits and cannot be used in practical applications.

Sleep energy, becomes more significant in ultra-low power operations for two reasons. First, the reduced switching energy consumption from scaled supply voltages renders the sleep energy a more significant portion of total energy consumption. The ultra-low power applications have low duty cycles and so there is a considerable amount of sleep time between the moment of completing a task and the start of a new task. Since there is a large amount of sleep energy consumption during this period, an optimization method that considers sleep energy consumption is vital to an energy-optimal design [1].

The rest of the paper is organized as follows: section 2 describes the proposed architecture; section 3 includes simulation and results; section 4 presents conclusion.

II. SYSTEM ARCHITECTURE

In this paper, we proposed an 8-bit Arithmetic and Logic Unit (ALU) circuit with Power Gating Switches (PGS) to reduce sleep mode energy consumption. Power Gating Switches are a sleep energy reduction scheme, which is an effective method for reducing overall energy consumption of a circuit. While many other methods can be used in sleep mode, such as reverse body-biasing, transistors stacking etc., PGSs are considered the most effective measure to reduce leakage energy consumption.

The purpose of employing PGSs in CMOS circuits is to reduce sleep power by closing the leakage paths completely during sleep modes. The basic strategy of power gating is to provide low power mode and an active mode. The goal is to switch between these two modes at the appropriate time and in the appropriate manner to maximize power savings and performance.

The Power Gating Switches can be added to a circuit in two forms such as a header or as footer. The header switch is implemented by PMOS transistors which are less leaky than NMOS transistor of a same size. A header switch implementation usually consumes more area

than a footer switch implementation [5]. The footer switch is implemented by NMOS transistor that has a high drive and smaller area [3] and so it is implemented in our proposed method. Fig.1 shows the various types of adding PGS to a circuit.

To analyze the sleep mode energy consumption in circuits using PGS, two parameters are proposed. The first parameter is Sleep Energy Reduction factor which is based on the sleep power of a circuit with and without PGS. The second parameter is Delay Degradation Factor that depends on circuit delay of the circuit with and without the PGS.

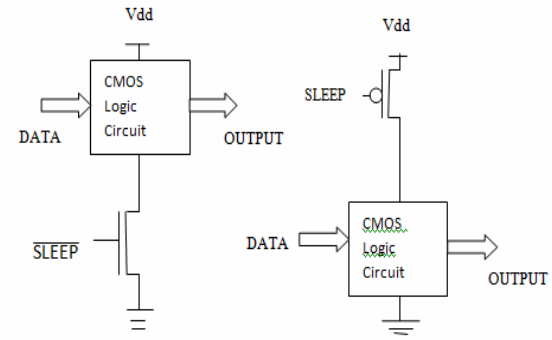

Fig. 1 Footer and Header implementation in logic blocks.

In our proposed method, an Arithmetic and Logic Unit with sleep transistors is proposed to measure the reduction in energy consumption. The arithmetic logic unit (ALU) is the core of a CPU in a computer. The proposed 8-bit ALU design consists of different kinds of logic such as Carry Look Ahead adder, Subtractor, Multiplexers, Inverter, NAND, NOR, EX-OR, etc.

The 8-Bit ALU is constructed using static complementary CMOS logic style. i.e., transistor level implementation of 8-Bit ALU is constructed and the required output can be selected by means of a multiplexer. Static complementary CMOS logic style is preferred over other logic styles because the number of transistors required to implement a logic function is less. The primary advantage of the CMOS structure is it's low sensitivity to noise, good performance, and low power consumption. Then the leakage current that flows through the ground is measured for ALU circuit. It is measured by means of Microwind software.

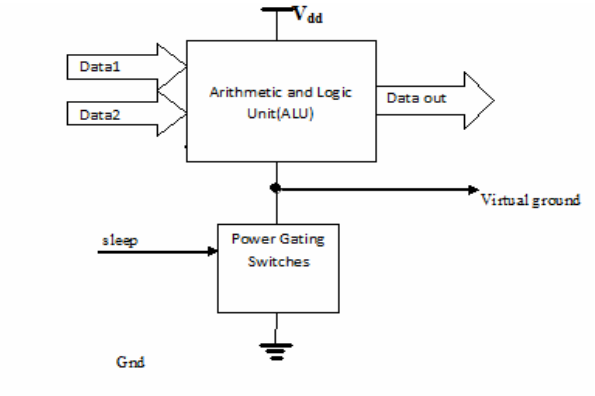

Fig.2 ALU circuit with PGS implementation

Whenever input transitions occur, leakage current that flows through the ground also increases. Power gating switches are added to reduce the leakage current that flows through the ground when the circuit enters sleep mode. So the PGS are also called as sleep transistors. PGS are connected between the circuit and the ground as shown in Fig.2 and the reduction in leakage current has to be analyzed.

III. EXPERIMENTAL RESULTS

The experimental results of an 8-bit ALU are analyzed using various softwares such as LTSPICE IV 4.15p, DSCH 2.7f and Microwind 2.6a. From Fig.3, the leakage current of 8-bit ALU without power gating switches is in the range of 5.9145mA. This can be reduced by adding the proposed Power Gating Switches in series with the circuit. Whenever the input and output voltage levels of CMOS changes, the leakage current flows through the ground is also increased. As a result, power consumption of the circuit gets increased which leads to increased heat dissipation and reduced life time of VLSI circuits.

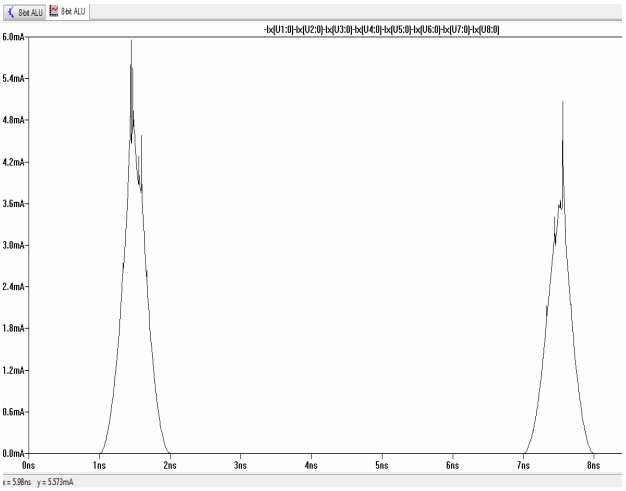

Fig.3 Leakage current of 8-bit ALU circuit

The leakage current is the current that flows through the ground whenever an input combination is applied to the circuit. The high leakage power dissipation is due to high supply voltage, large switching transitions etc. When a chip dissipates too much power, it will either become too hot and cease working or will need extra expensive cooling. Besides, there is a special category of applications such as portable equipments powered by batteries, for which low power consumption is of primary importance. Designing for low power may lead to an increase in the chip area. Leakage power is already a major concern in current technologies, because it impacts battery lifetime even if the circuit is completely idle.

TABLE I: Leakage current analysis of various components in 8-Bit ALU.

Component	Leakage current without PGS	Leakage current with PGS
1-Bit arithmetic unit	523.13µA	0.35mA
1-Bit logic unit	49nA	0
4 to 1 Multiplexer	291.45µA	0
2 to 1 Multiplexer	222.91µA	0
8-Bit Arithmetic and Logic unit	5.914mA	0.78mA

In fact, CMOS technology has traditionally been extremely power-efficient when transistors are not switching, and system designers expect low leakage from CMOS chips. To meet leakage power constraints, Power Gating Switches are proposed and the Table I shows the reduction in leakage current with the addition of Power Gating Switches in 8-bit ALU. The following table shows the leakage power of 8-Bit ALU when the supply voltage is about 1.2V.

TABLE II: Leakage power analysis in 8-Bit ALU

COMPONENT	LEAKAGE CURRENT	LEAKAGE POWER
1-Bit arithmetic unit	523.13µA	0.1405µw
1-Bit logic unit	49nA	0.24412µw
8-Bit Arithmetic and Logic unit	5.946mA	29.786mW

An 8-Bit ALU performs various operations depending upon the combination of inputs given to it such as addition, subtraction, increment, decrement etc. and logic functions such as AND, OR , EXOR etc. Table III shows the delay and power required for various operations that are performed using 8-Bit ALU. Leakage current analysis is carried out for various arithmetic and logic operations performed by ALU.

By controlling the data inputs to the arithmetic circuit, it is possible to obtain different types of arithmetic operations. Select lines of multiplexer such as S0, S1 can be used to control input B. The logic circuit can be combined with the arithmetic circuit to produce logical operations. Selection variables S_1 and S_0 can be common to both circuits and a third selection variable S_2 can be used to differentiate between the logic and arithmetic operations.

TABLE III: Power-Delay analysis of various operations performed in 8-Bit ALU

S.No	OPERATION	DELAY	POWER	LEAKAGE CURRENT
1	Addition	2.7nS	0.210mW	0.188mA
2	Subtraction	16.1nS	0.067mW	0.202mA
3	Transfer Data	1.5nS	0.293mW	0.607mA
4	Increment	19.5nS	0.134mW	0.184mA
5	Decrement	20nS	0.050mW	0.643mA
6	Add with Carry	16nS	0.178mW	0.246mA
7	EXOR	5.9nS	0.128mW	1.360mA
8	NOT	5.1nS	0mW	1.397mA
9	AND	8.7nS	0.475mW	1.360mA
10	OR	5.2nS	0.006mW	1.397mA

The area of a 8-Bit ALU with and without PGS are analyzed using Microwind tool and the layouts are

generated for the schematics provided. Table IV shows the increase in area of 8-bit ALU due to the addition of PGS.

TABLE IV: Area requirement of 8-Bit ALU with PGS

COMPONENT	AREA WITHOUT PGS	AREA WITH PGS
1-Bit arithmetic unit	109x20µm	111x18µm
1-Bit logic unit	54x12µm	57x13µm
4 to 1 Multiplexer	101x16µm	103x19µm
2 to 1 Multiplexer	45x13µm	48x13 µm
8-Bit Arithmetic and Logic unit	1952x17µm	2002x26µm

IV. CONCLUSION

An Arithmetic and Logic Unit (ALU), which is commonly used in microprocessors, is constructed by means of separate blocks such as Adder and Subtractor block, Logic block and Multiplexers for selecting the outputs. All these blocks are constructed by using MOS transistors in LTSPICE IV and DSCH and also the leakage current that flows through the ground has been measured with and without PGS. The energy consumption of 8-bit ALU with PGS is found to be 0.387pJ/cycle. The total area of 8-bit ALU is increased by about 22.14% due to the addition of Power Gating Switches (PGS). The leakage power of 8-bit ALU is decreased by about 13.12%. Thus, the leakage current has been reduced by adding power gating switches to an 8-Bit ALU circuit.

REFERENCES

[1] Blaauw. D, Hanson.S, Seok.M, and Sylvester.D, "Sleep Mode Analysis and Optimization with Minimal-Sized Power Gating Switch for Ultra-Low V_{DD} Operation," IEEE Journal of Very Large Scale Integration (VLSI) Systems, vol. 20, no. 4,pp. 605-615 April 2012.

[2] Chandrakasan.A, and Wang "A 180-mV subthreshold FFT processor sing a minimum energy design methodology," IEEE Journal of Solid- State Circuits, vol. 40, no. 1, pp. 310–319, January 2005.

[3] Austin.T, Blaauw.D, Helfand.R, Minuth.M, Nazhadili.L, Olson.J, Pant.S, Reeves.A, and Zhai.B, "A 2.60 pJ/Inst subthreshold sensor processor for optimal energy efficiency," in Proc. Symp. VLSI Circuits, pp. 154–155, 2006.

[4] Austin.T, Minuth.M, and Nazhadili.L, "SenseBench: Toward an accurate evaluation of sensor network processors," in Proc.Workload Characterization Symp., pp. 197–203, October 2005.

[5] Paul B.C, Raychowdhury.A, and Roy.K, "Device optimization for digital subthreshold logic operation," IEEE Transactions on Electron Devices, vol. 52, no. 2, pp. 237–247, February 2005.

[6] Blaauw.D, Hanson.S, Seok.M, and Sylvester.D, "Nanometer device scaling in subthreshold circuits," in Proc. Des. Autom. Conf. (DAC), pp. 700–705, June 2007.

[7] Blaauw.D, Seok.M, and Sylvester.D, "Optimal technology selection for minimizing energy and variability in low voltage applications," in Proc. Int. Symp. Low Power Electron. Des., pp. 9–14, August 2008.

[8] Calhoun.B, Chandrakasan.A, and Wang.A, "Device sizing for minimum energy operation in subthreshold circuits," in Proc. Custom Integr. Circuits Conf., pp. 95–98, September 2004.

[9] Eom.H, Keane.J, Kim.C, KimT.H, and Sapatnekar.S, "Subthreshold logical effort: A systematic framework for optimal subthreshold device sizing," in Proceedings. DAC, pp. 425–428, 2006.

[10] Kim.K, Kulkarni.J.P, and Roy.K, "A 160 mV robust schmitt trigger based subthreshold SRAM," IEEE J. Solid-State Circuits, vol. 42, no. 10, pp. 2303–2313, October 2007.