Design of 4-bit Carry look Ahead Adder with Logic Gates and Cells

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Abstract— **Carry look ahead adder is by default high speed structure but with sacrificing area and power. In this paper we proposed Carry look ahead adder with low area and low power. We have designed xor and xnor cells in which it generates two outputs. Xor outputs the xor and nor logic where as xnor outputs the xnor and nand logic.We can design adder by efficiently utilizing the hardware required for sum logic to the carry logic. But the choice of using only xor or only xnor or combination of both for designing sum logic has considerable impact on the hardware requirements of the carry logic. Total transistor count for proposed 4-bit carry look ahead adder is 164 with existing design transistor count of 236.**

Index Terms— CMOS, Optimization, universal gates, XNOR.

I. INTRODUCTION

Carry look ahead adder proposed was designed by Amita consumes more PDP(Power Delay Product) as well as more ADP(Area Delay Product) but gives more speed[1]. Carry look ahead adders presented was designed by jagannath samanta with many logic styles[2]. K.Ueda designed carry look ahead adder by using pass transistor logic which has limitation of supply voltage and does have problem of noise margin reduction[3]. Y.T Pai proposed a design for low delay but with out much sacrificing other design considerations[4]. ADP(Area Delay Product) optimized design of carry look ahead adder proposed in[5].

II. CARRY LOOK AHEAD ADDER

Carry look ahead adder needs XOR, XNOR, NAND, NOR and NOT gates. We have used efficiently universal gates as well as XOR and XNOR. We have done the necessary boolean optimization. Fan-in and Fan-out has also been taken into consideration.

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The number of levels in our proposed design are more than existing design but the hardware in that particular levels does vary the results in optimization of hardware. Delay does not depend on the number of levels in the circuit but the actual hardware in that levels and also the number of levels. Carry look ahead adder does have need of optimizing the area and power but with out sacrificing much of those.

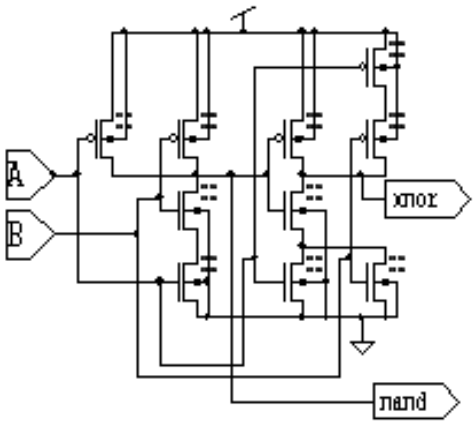

Fig.1 Circuit of XNOR.

Above figure indicates that it is a cell consisting of two outputs which are XNOR and NAND. It requires 10 number of transistors.It consists of 5 number of P-MOSFETS and N-MOSFETS.It has 4 number of paths possible out of which two are logic1 and two are which logic0 giving paths but the total paths are 6 out of which only 4 are activated at any point of time. It does have two demarcation lines and each demarcation line corresponds to one function. XOR also have a similar kind of design but with just first demarcation line pull-up becoming pull-down and pull-down becoming pull-up. Second demarcation line also needs the inversion of pull-up and pull-down region.We have proposed the equations of sum and carry part of the adder.

It does have a combination of XOR,XNOR and few gates. The maximum fan-in is only 5 and the levels in the above equations requires only 6 but we have considerably saved the hardware which results in optimization of area and power.As a VLSI designer we need to keep in mind the constraints like power, area and speed as well as cost.

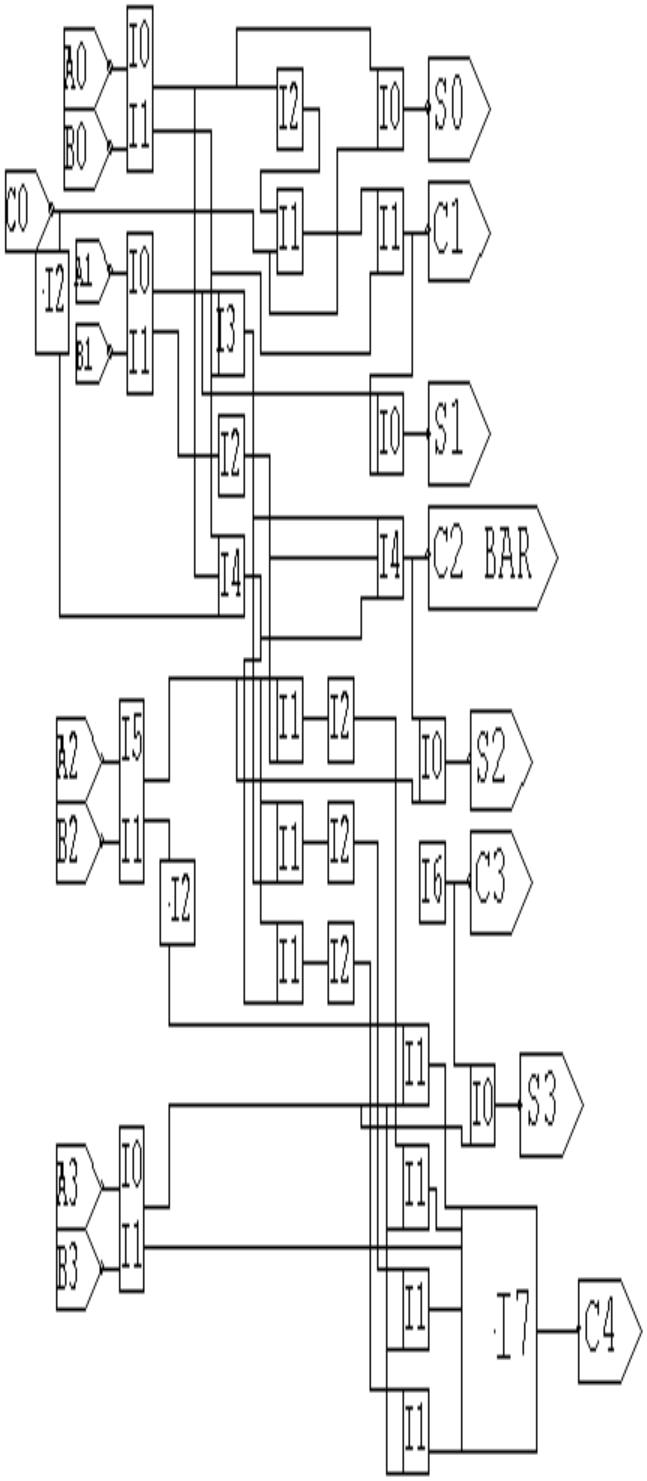

Fig.2 Circuit of CLA.

Above figure [I0,I1] indicates that it is a cell consisting of XNOR and NAND logic and [I5,I1] indicates that it is a cell consisting of XOR and NOR logic. Total of 7 not gates, 9 two input nand gates, one 4-input nand gate, one 5-input nand gate, one 2-input nor gate, 2 3-input nor gates, 4 xnor gates, 3 xnor cells and one xor cell.

Table1 Gate Identifiers.

IDENTIFIER	LOGIC GATE(FAN-IN)
I0	XNOR(2)
I1	NAND(2)
I2	NOT(1)
I3	NOR(2)
I4	NOR(3)
I5	XOR(2)
I6	NAND(4)
I7	NAND(5)

Above table indicates that [I1,I6, I7] are the NAND gates but with fan-in of 2,4,5 respectively.[I3,I4] are the NOR gates but with fan-in of 2,3. I0 is XNOR cell, I2 is NOT gate and I5 is XOR cell.

III. UNIVERSAL GATES

Universal gates has the advantage of realizing any function but with sacrificing the design constraints like Area, Power and Speed. NAND/NOR gate is a better gate when compared to AND/OR gate in CMOS. Design should consist of as many as NAND,NOR and NOT Gates. Cost is also one more important constraint needs to be taken into consideration and if the total number of cells needed in our design are less then we would get reasonable regularity factor. Proposed design used only 4 number of cells in which requirement was NOT,NAND,NOR and XNOR. Designing a universal gate based design is a different one from designing a circuit with universal gates and our proposed design has utilized universal gates but our design is not a universal gate based design.

IV. PERFORMANCE ANALYSIS

Implementation of 4-bit carry look ahead adder has been done using Static CMOS logic style. Table1 indicates proposed design has 30% reduction in transistor count with respect to the existing design. Table1 shows the proposed design needs XOR as well as XNOR and universal gates and not gate.

TABLE1 Comparison of Area in Two Designs

Gates	Design in reference2	Proposed design
XOR	8	1
XNOR	-	7
NAND2	-	9
NAND4	-	1
NAND5	-	1
AND2	8	-
AND3	3	-
AND4	2	-

AND5	1	-
OR2	1	-
NOR2	-	1
NOR3	-	2
OR3	1	-
OR4	1	-
OR5	1	-
NOT	-	7

Table2 shows there is 30% reduction in transistor count for the proposed design with respect to the existing design.

TABLE2 Comparison of Total Area in Two Designs

Area(4-bit)	Design in reference2	Proposed design
Transistors	236	164

V. CONCLUSION

Proposed design has been optimized with respect to the design constraints of VLSI. This optimization is not only applicable for 4-bit but also for N-bit. There is 30% reduction in transistor count for the proposed design with respect to the existing design for 4-bit.Proposed design requires only four cells and this helps layout designers a lot specifically when we go for manual layout design and layout designers can come up with the required VLSI constraints only when the circuit is an optimized one. Delay not only depends on the number of levels in the design but the prime factor is the logic requirement in that level.. It shows an 4-bit carry look ahead adder of the proposed architecture needs 164 transistors.

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