Area Efficient Design of 4-Bit Carry Select Adder with Low Power

Lekkala Ramadevi, D.Pavana Kumari, Bhaskara Rao Doddi

Abstract— **Adder is an vital operation in ALU. Out of Many existing adders, Carry select adder have much significance. In this paper we proposed CMOS Carry select adder with low area as well as low power. We have designed a cell such that it can produce multiple outputs and this is what lead to the optimization. Universal gates like NAND and NOR also used instead of using basic logic gates like AND and OR has lead to optimization. Half sum generation unit has been optimized from 64 to 46 transistors. In Carry unit with zero carry input block transistor reduction is from 36 to 24. Carry unit with one carry input block there was limited reduction in transistor count from 42 to 36. Carry unit block has been optimized from 48 to 32 transistors. Sum unit block has not given us any scope to do optimization. Total transistor count reduction for 4-bit is from 230 to 178 with existing design and in equal proportion optimization is possible for N-bit.**

Index Terms— CMOS, Optimization, universal gates, XNOR.

I. INTRODUCTION

Optimized constraints of VLSI systems are the need for the industry and many applications can be seen in[1],[2]. An adder is vital component of central processing unit's (CPU) main unit . A ripple carry adder has uniform structure, but delay due to the carry is a concern. Carry look-ahead and carry select structures have been proposed to increase the speed of adders. A conventional carry select adder generates a twin of sum words and carry words [3]. A conventional CSLA has high speed than an RCA, but the design occupies huge area. Few designs have been proposed to avoid huge area. Kim and Kim [4]circuit is proposed with the implementation of data selector.

Design was proposed with large bit-width adders with high speed by using a square-root (SQRT)[5].The main intention of SQRT-CSLA design is to give a parallelism structure which helps to increase the overall speed of the adder. Ramkumar and Kittur [6] suggested a binary to BEC-based CSLA. The BEC-based CSLA has less hardware than the existing CSLA, but it has minor less speed in comparison. A CSLA based on common Boolean logic is also proposed in [7] and [8]. The CBL-based CSLA of [7]involves significantly less logic elements than the existing CSLA but it has less speed, which is nearer to RCA .To enhance the speed, a SQRT-CSLA based on CBL was proposed in [8]. However, the CBL-based SQRT CSLA design of [8] requires more logic elements and delay than the BEC-based SQRT-CSLA of [6]. Design in [10] used basic logic gates and XOR for their design.

II. CARRY SELECT ADDER

Carry select adder has five blocks namely half sum generation unit, carry block when input carry is '0', carry block when input carry is '1', carry unit and sum unit.Half sum generation unit produced half sum output and generate part of carry output[1]. Proposed half sum generation unit will produce half sum output and complemented generate part of carry output. carry block when input carry is '0' produced carry outputs with AND and OR gates [1]. Proposed carry block when input carry is '0' will produce carry outputs with NOR gates. Carry block when input carry is '1' produced carry outputs with OR and AND gates [1]. Proposed carry block when input carry is '1' will produce carry outputs with NOR gates. Carry block produced carry outputs with AND and OR gates [1]. Proposed carry block will produce carry outputs with NAND gates. Sum block produced sum outputs with XOR gates [1]. Proposed Sum block will produce sum outputs with XNOR gates.

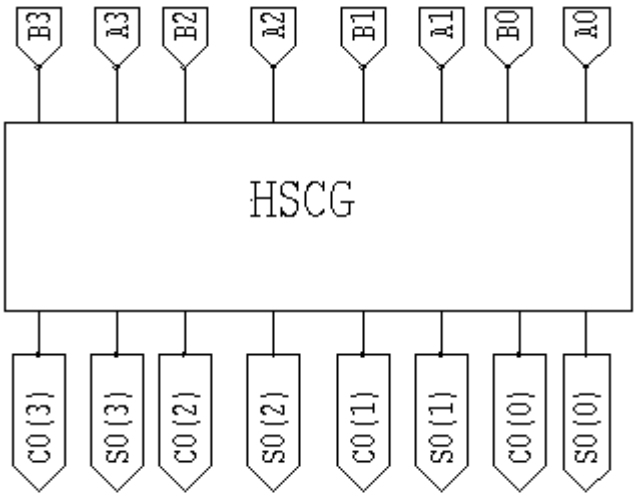

Fig.1 Symbol of Half Sum Carry Generation.

Fig.1 indicates there are 8 inputs and 8 outputs out of which 4 are the inputs of A, 4 are the inputs of B, 4 are the half sum outputs and 4 are the generate part of carry outputs.

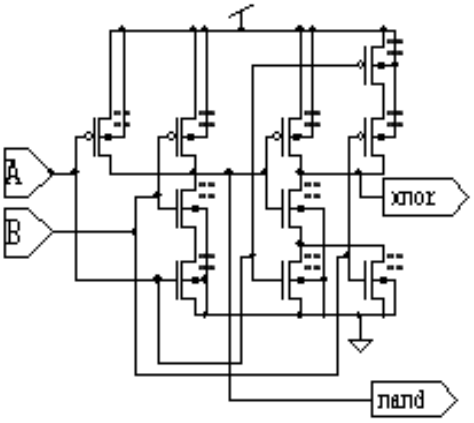

Fig.2 Circuit of XNOR.

Fig.2 indicates there are 2 inputs and 2 outputs out of which 1 is the input of A, 1 is the input of B, 2 are the outputs of XNOR and NAND.

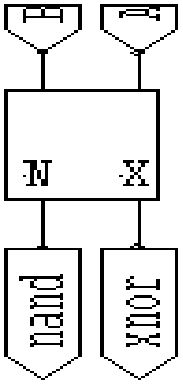

Fig.3 Symbol of XNOR.

Fig.3 indicates there are 2 inputs and 2 outputs out of which X stands for XNOR and N stands for NAND.

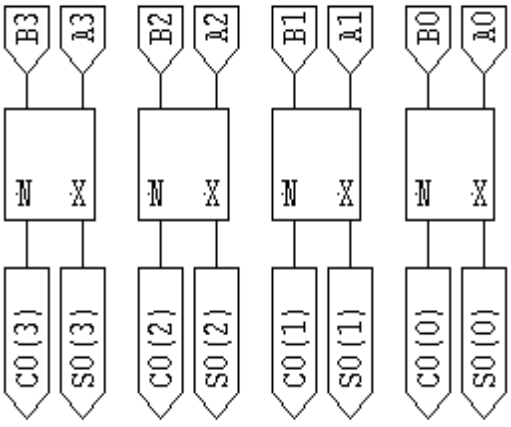

Fig.4 Circuit of Half Sum Carry Generation.

Fig.4 indicates that XNOR is needed for half sum generation And NAND is needed for complemented generate part of carry output.

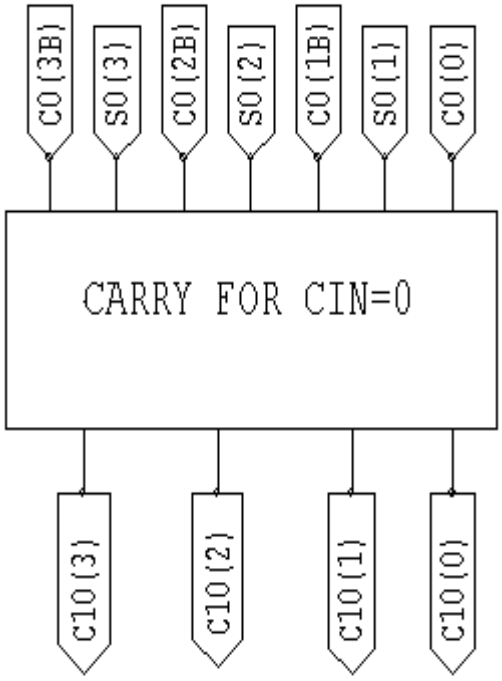

Fig.5 Symbol of Carry Block When Input Carry is '0'.

Fig.5 indicates there are 7 inputs and 4 outputs out of which 4 are the inputs of carry, 3 are the inputs of sum, 4 are the carry outputs.

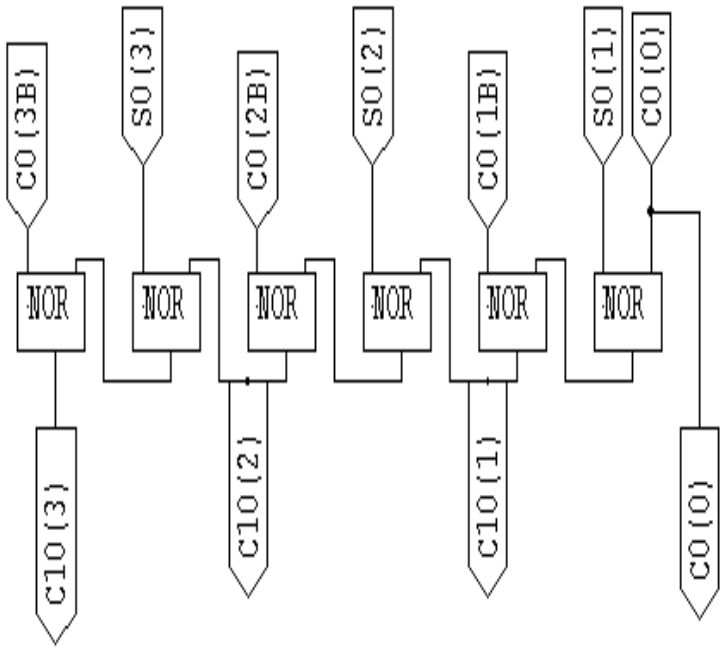

Fig.6 Circuit of Carry Block When Input Carry is '0'.

Fig.6 indicates that NOR gate is needed to generate complemented carry outputs. Universal gate of NOR is alone enough to produce carry outputs when carry input is '0'.

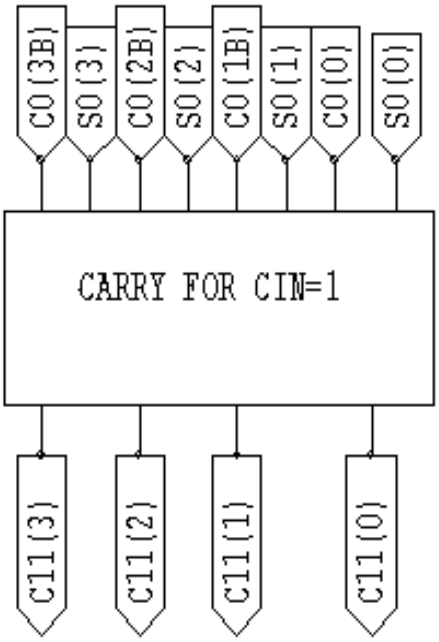

Fig.7 Symbol of Carry Block When Input Carry is '1'.

Fig.7 indicates there are 8 inputs and 4 outputs out of which 4 are the inputs of carry, 4 are the inputs of sum, 4 are the carry outputs.

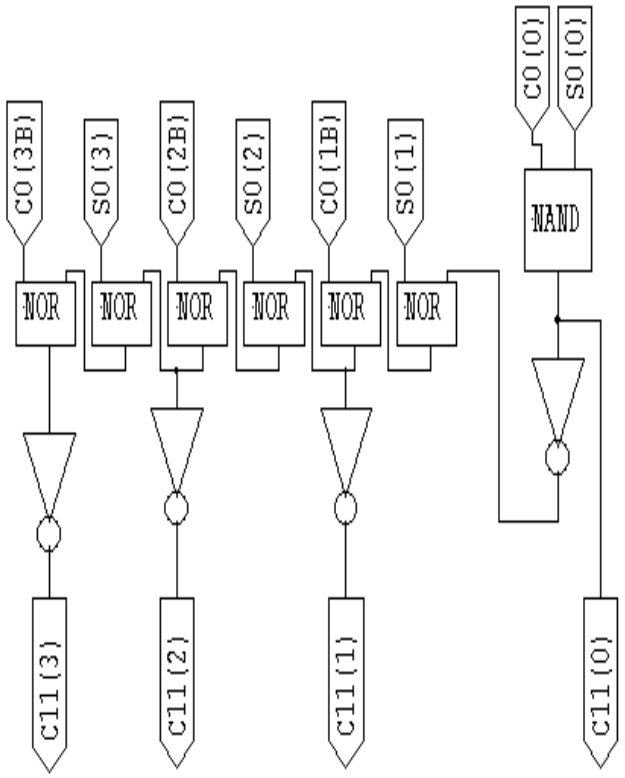

Fig.8 Circuit of Carry Block When Input Carry is '1'.

Fig.8 indicates that NOR, NAND and NOT gate is needed to generate carry outputs. This block generates true form of carry outputs.

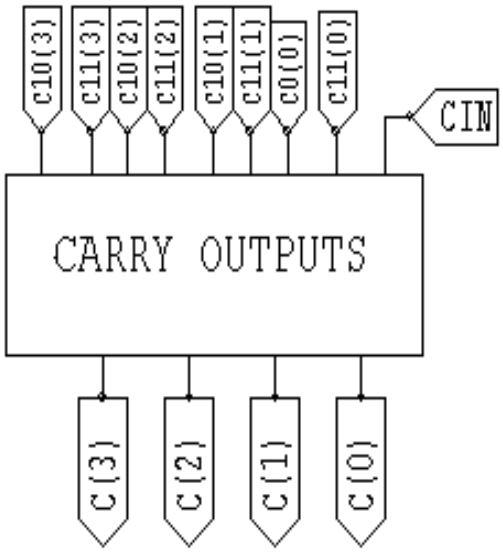

Fig.9 Symbol of Carry Block.

Fig.9 indicates there are 9 inputs and 4 outputs out of which 4 are the inputs of carry when carry input is'0', 4 are the inputs of carry when carry input is'1, 1 is the initial carry input and 4 are the carry outputs.

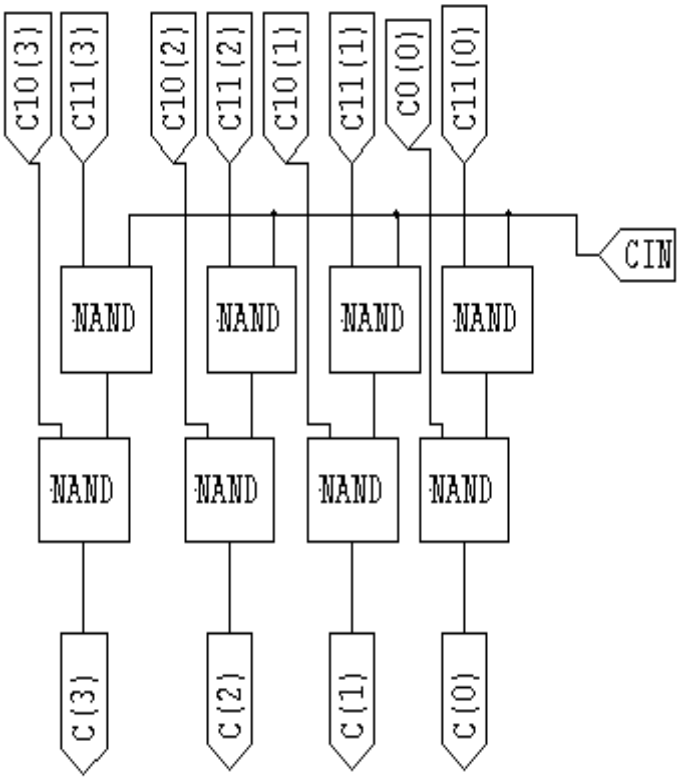

Fig.10 Circuit of Carry Block.

Fig.10 indicates that NAND gate is needed to generate carry outputs. This block generates true form of carry outputs.This block has used universal gate of NAND.

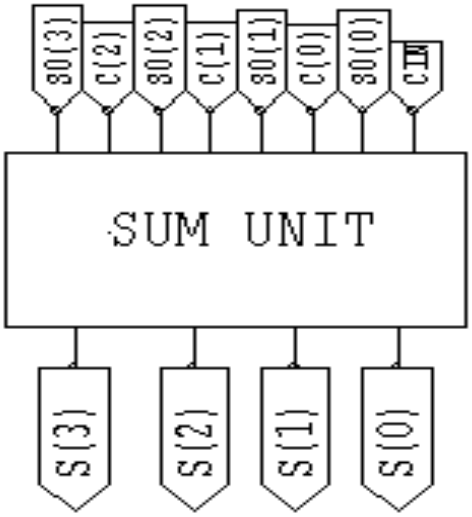

Fig.11 Symbol of Sum Block.

Fig.11 indicates there are 8 inputs and 4 outputs out of which 4 are the inputs of carry , 4 are the inputs of half sum and 4 are the sum outputs.

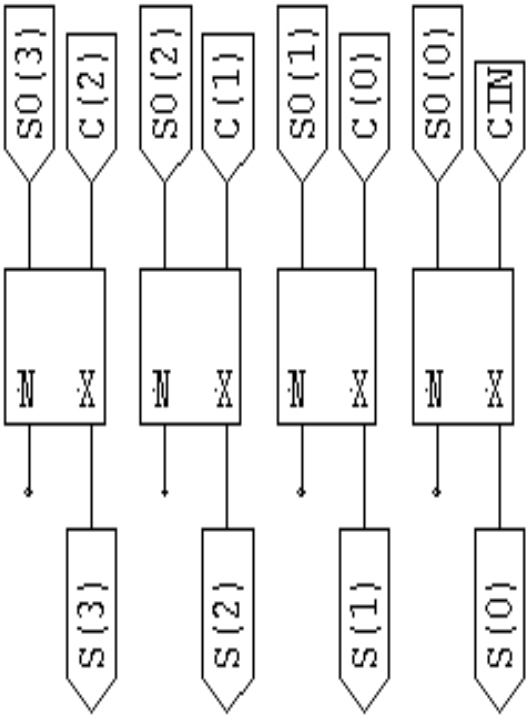

Fig.12 Circuit of Sum Block.

Fig.12 indicates that XNOR gate is needed to generate Sum outputs. This block generates true form of sum outputs.

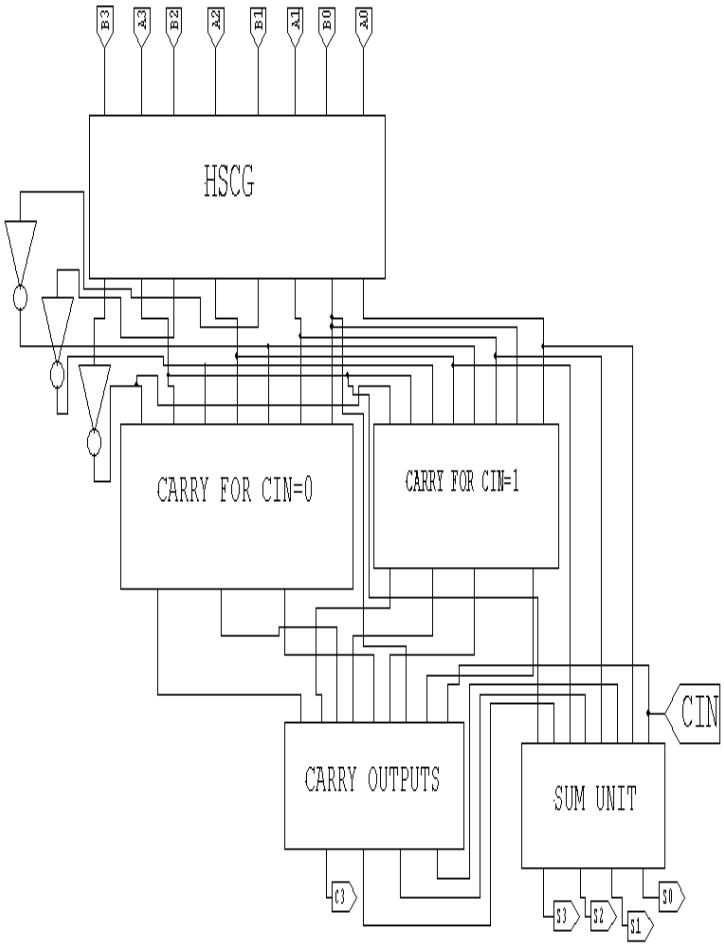

Fig.13 Circuit of Carry Select Adder Block.

Fig.13 indicates that HSCG generates half sum and generate part of carry outputs. Outputs of HSCG Will be the inputs of carry for cin=0 and carry for cin=1. Outputs of carry for cin=0 and carry for cin=1 will be the inputs of carry outputs. Outputs of the carry outputs will be the inputs of the sum unit.

III. UNIVERSAL GATES

Universal gates has the advantage of realizing any function but with sacrificing the design constraints like Area, Power and Speed. NAND/NOR gate is a better gate when compared to AND/OR gate in CMOS. Design should consist of as many as NAND,NOR and NOT Gates. Cost is also one more important constraint needs to be taken into consideration and if the total number of cells needed in our design are less then we would get reasonable regularity factor. Proposed design used only 4 number of cells in which requirement was NOT,NAND,NOR and XNOR. Designing a universal gate based design is a different one from designing a circuit with universal gates and our proposed design has utilized universal gates but our design is not a universal gate based design.

IV. PERFORMANCE ANALYSIS

Implementation of 4-bit carry select adder has been done using Static CMOS logic style. Table1 indicates proposed

design has 27% reduction in transistor count with respect to the existing half sum generation unit. There is 33% reduction in transistor count with respect to the existing Carry unit with zero carry input. There is 14% reduction in transistor count with respect to the existing Carry unit with one carry input. There is 32% reduction in transistor count with respect to the existing Carry unit. There is no reduction in transistor count with respect to the existing Sum unit.

TABLE1 Comparison of Area in Two Designs

Transistor count(4-bit)	Design in reference10	Proposed design
Half sum generation unit	64	46
Carry unit with zero carry input	36	24
Carry unit with one carry input	42	36
Carry unit	48	32
Sum unit	40	40

Table2 shows there is 23% reduction in transistor count for the proposed design with respect to the existing design.

TABLE2 Comparison of Total Area in Two Designs

Area(4-bit)	Design in reference10	Proposed design
Transistors	230	178

Table3 shows there is considerable reduction in average power consumption when the supply voltage is scaled down and the simulation has run for three cycles with each cycle duration is 10 ns and the first cycle with all the primary inputs to logic '1' and second cycle with all the primary inputs to logic '0' and last cycle with all the primary inputs to logic '1'.

TABLE3 Average Power Consumption of Proposed Design

SUPPLY VOLTAGE	PROPOSED DESIGN
2V	8.527308e-004 watts
1.5V	5.156378e-005 watts
1V	1.404432e-005 watts

V. CONCLUSION

Proposed design has been optimized with respect to the design constraints of VLSI. Four out of five blocks in the carry select adder has been optimized in comparison with the existing design. This optimization is not only applicable for 4-bit but also for N-bit. There is 23% reduction in transistor count for the proposed design with respect to the existing design for 4-bit.Proposed design requires only four cells and this helps in designing the layout such that Time to market constraint of manufacturing companies will be met. Universal gates are also utilized instead of going for basic logic gates design. It shows an 4-bit carry select adder of the proposed architecture needs 178 transistors.

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