Design of an 8-bit Magnitude Comparator with Small Transistor Count and Low Power Using Hybrid STATIC CMOS/ TG Logic

Bhaskara Rao Doddi, Y E Vasanth Kumar, Sankara Rao Palla

Abstract— **COMPARATOR is the basic module in digital system. It is widely used in communication and calculation areas. Traditional comparator circuit is based on truth table leads to non-optimized design with respect to area, power and speed. The main objective of this paper is to provide new low power, area solution for very large scale integration (VLSI) designers. At circuit level, STATIC CMOS logic style can give better results over others when we design efficiently and at the same time if we are going for STATIC CMOS only means that we are not taking the advantage of other Logic styles instead we go for mix of STATIC CMOS and TG(Transmission Gate). In this project the proposed comparator has been designed by using STATIC CMOS/TG 180nm TECHNOLOGY. Layout for comparator will be implemented by using tanner tool.**

Index Terms— Comparison Cell, MUX21, Magnitude COMPARATOR, STATIC CMOS.

I. INTRODUCTION

Geetanjali Sharma[1] has Designed Comparator by using CMOS/PTL. Fan Yong-jie[2] has Designed Comparator by using Dynamic Logic/PTL. C-H HUANG[3] developed priority encoder based on logic and module. S-W CHENG[4] employed conditional sum adder to design efficient comparator. J-Y KIM and H-J YOO[5] proposed a design without arithmetic operation which is even more efficient. Now we need to design a comparator by following our own technique such that low power and low area is achieved. We have designed comparator by using STATIC CMOS/TG logic style.

STATIC CMOS has advantage of low power consumption but dis-advantage of area with respect to number of Transistors, so here we will have the Challenge to design the comparator with less number of transistors. Logic style like PTL(Pass Transistor Logic) has advantage of less number of transistors but it has the problem of logic level degradation, so we went for TG which has the full output voltage swing and dis-advantage is it takes more number of transistors. here the challenge is to Design Comparator with small Transistor count by using Logic styles which by default takes more number of Transistors.

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II. MAGNITUDE COMPARATOR

Comparator is going to compare 8 bits of A(A7 to A0) and 8 bits of B(B7 to B0) and decides whether ALTB(A<B) or AGTEQB(A>=B).Proposed Comparator consists of total four stages, stage1 has only Comparison cells and stage2,stage3,stage4 consists of only two-to-one Multiplexers. we can design the circuit for any one of the two conditions either ALTB(A<B) or AGTEQB(A>=B) then we can arrange the second one but which output to design is the concern, if we try to design AGTEQB(A>=B) as the output might not be a good idea, because we need to check all the 8-bits of A and B then only we can say AEQB(A=B) is true or not but even 1-bit of A and B can be enough to judge whether AGTB(A>B) or not, so circuit has been designed for ALTB(A<B) because here the output is straightforward and also has one condition.

How can circuit be designed for ALTB(A<B) we need to know what are all the conditions for ALTB(A<B) to become true, there will be N-conditions for ALTB(A<B) to be TRUE for an N-Bit Comparator if (A7<B7) then ALTB(A<B) should be true, so we have designed a sub-circuit for this condition so till now we have designed for one condition of ALTB(A<B) out of 8 conditions, sub-circuit is Comparison cell which has the two sub-circuits.

If (A6<B6) and (A7>B7) is not TRUE then ALTB(A<B) should be TRUE. so we have designed a sub-circuits for this condition so till now we have designed for two conditions of ALTB(A<B) out of 8 conditions, sub-circuits are one is Comparison cell and other has two two-to-one multiplexers. So total for Designing two conditions we need two Comparison cells and two two-to-one multiplexers at stage1.

If(A5<B5) and(A7>B7),(A6>B6) are not TRUE and If(A4<B4) and(A7>B7),(A6>B6),(A5>B5) are not TRUE then ALTB(A<B) should be TRUE for this we need two Comparison cells and two two-to-one multiplexers. So total for Designing four conditions we need four Comparison cells and four two-to-one multiplexers at stage1.

If(A3<B3) and(A7>B7),(A6>B6) (A5>B5),(A4>B4) are not TRUE and If(A2<B2) and(A7>B7),(A6>B6),(A5>B5) ,(A4>B4),(A3>B3) are not TRUE then ALTB(A<B) should be TRUE for this we need two Comparison cells and two two-to-one multiplexers. So total for Designing six conditions we need six Comparison cells and six two-to-one multiplexers at stage1.

If(A1<B1) and(A7>B7),(A6>B6), (A5>B5),(A4>B4) (A3>B3),(A2>B2) are not TRUE and If(A0<B0) and(A7>B7),(A6>B6),(A5>B5) ,(A4>B4),(A3>B3) ,(A2>B2),(A1>B1) are not TRUE then ALTB(A<B) should be TRUE for this we need one Comparison cell,one inverter and one two input nand gate and one two-to-one multiplexer. So total for Designing eight conditions we need seven Comparison cells,one inverter,one two input nand gate and seven two-to-one multiplexers at stage1.

Now we need to merge first four conditions which has four two-to-one multiplexers at stage1 into two two-to-one multiplexers at stage2 so till now we have finished 4-Bit Comparison that to from MSB(MOST SIGNIFICANT BIT) to MSB(MOST SIGNIFICANT BIT-3).

Now we need to merge last four conditions which has three two-to-one multiplexers at stage1 into one two-to-one multiplexer at stage2 so till now we have finished 4-Bit Comparison that to from MSB(MOST SIGNIFICANT BIT-4) to LSB(LEAST SIGNIFICANT BIT).
We have three two-to-one multiplexers at stage 2 and finally merging of entire eight conditions result in having one two-to-one multiplexer at stage3.

There are 2 cells in this comparator named Comparison cell and MUX21 . Comparison cell which is needed at stage0 only compares Bits of A and B that is (An, Bn) where n starts from 7 down to zero and determines whether A is less than B or not at that corresponding Bit . MUX21 compares two Bit result coming from the previous stage and selection line will also come from earlier stage and selection will be like if s=1 top line will be selected , so for an 8-bit comparator there will be 7 Comparison cells , 11 two-to-one multiplexers, 1 inverter and 1 two-input nand gate. Comparison cell, MUX21, Inverter and nand gate are used in our design.

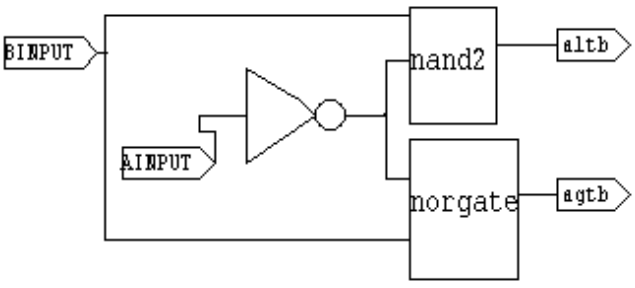

Fig. 1 Comparison Cell.

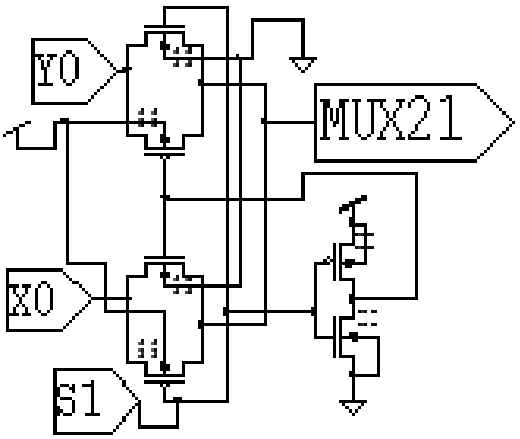

Fig. 2 TG based MUX21.

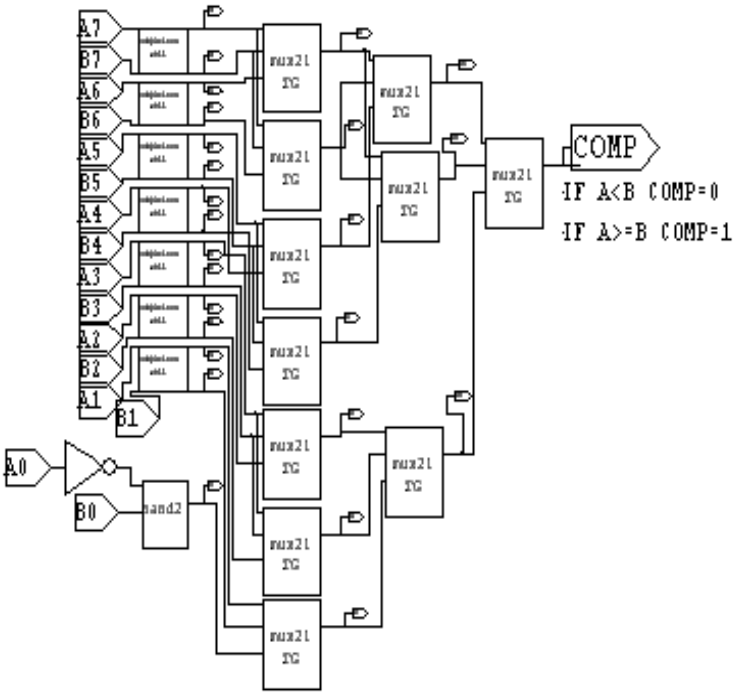

Fig. 3 8-BIT MAGNITUDE COMPARATOR

Comparison cell has two inputs and two outputs, inputs are ainput ,binput and outputs are agtb(a>b) and altb(a<b) and if these are "00" means that altb(a<b) is TRUE with that corresponding bit , "11" means that agtb(a>b) is TRUE with that corresponding bit, "01" means that decision is postponed to next level, "10" never happens.

MUX21 has three inputs X0,Y0,S1 and one output that is MUX21 when S1='1' then Y0 will be transferred to the output else X0. we have Designed MUX21 by using TG(Transmission Gate) to overcome the dis-advantages of PTL(Pass Transistor Logic) like Logic level degradation and also difficult to layout the Design.

III. STATIC CMOS/TG

CMOS has the advantage of low power consumption since if N-MOSFET is on then corresponding P-MOSFET is OFF.STATIC CMOS needs more number of transistors because if we require N-number of TRANSISTORS in the PULL-UP network we also need N-number of TRANSISTORS in the PULL-DOWN network.

STATIC CMOS has advantage of full output voltage swing, so we can easily differentiate between output voltage high logic level and output voltage low logic level and this will be even more beneficial when the technology is scaled down. it is recommended that not more than 4 number of transistors are there in series either in PULL-UP or PULL-DOWN region as delay is going to be worse.

If we need more number of transistors in either pull-up or pull-down in series then we need to introduce Buffer in between to reduce the number of transistors in series. For example if we have 7 N-MOSFET'S in series then we need 1 buffer and this will add 1 more N-MOSFET resulting in 8 N-MOSFET'S so that we can achieve two sections containing 4 N-MOSFET'S in series each.

Here the challenge alsoLies in Designing the layout for comparator by using STATIC CMOS cells and Advantage of using STATIC CMOS is we can Merge the cells comfortably so that unnecessary spacing between the cells can be optimized.

TG(Transmission Gate) based pass transistor logic has advantage of full output voltage swing and it normally requires complementary versions of the input signals but dis-advantage of taking more number of transistors when compared to NMOS only pass transistor logic, so we need to achieve our Design by taking less number of transistors even though by default TG(Transmission Gate) takes more number of transistors.

IV. PERFORMANCE ANALYSIS

Implementation of 8-bit magnitude comparator has been done using Hybrid STATIC CMOS/TG logic style. Table1 shows AREA comparision of IMPROVED HYBRID and STATIC CMOS/TG. power dissipation comparision for 8-bit magnitude comparator using IMPROVED HYBRID and STATIC CMOS/TG for various supply voltage(VDD) are shown in TABLE2. This table clearly shows that STATIC CMOS/TG has very less power dissipation than IMPROVED HYBRID over various supply voltage(VDD).

The comparator which we designed using STATIC CMOS/TG logic style uses less number of transistors. It uses 7.7% less area(number of transistors) than IMPROVED HYBRID.

TABLE1 COMPARISON OF AREA IN TWO DESIGNS

	Design in reference (Improved hybrid)	Design in this paper (Static CMOS/TG)
Area(number of transistors)	154	142

TABLE2 COMPARISON OF POWER IN TWO DESIGNS

VDD(V)	Average power consumption(µ W)	
	Design in reference paper (Improved hybrid)	Design in this paper (Static cmos)
1.4	21.4	0.109
1.2	12	0.079
1	6.05	0.053

V.CONCLUSION

High speed, low area and low power are the three design constraints, we need to achieve all these things but by ensuring that the functionality should not be disturbed so the primary motive is to achieve the functionality then start concentrating on the design constraints, if the circuit designer has the capability to design the circuit with intended functionality then by default we can get maximum optimization, we might look for low-power consumption and also low-area depending upon the requirement by sacrificing the performance up to some extent. We have designed our comparator by using Hybrid STATIC CMOS/TG logic style, we are able to design the comparator by using less number of transistors than IMPROVED HYBRID which is a mix of HYBRID PTL / CMOS logic style. It shows an 8-bit comparator of the proposed technique only needs 142 transistors.

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