Design of an N-Bit Extendable Ripple Carry Adder with Small Transistor Count Using STATIC CMOS Logic.

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Abstract— **The main intention of this paper is to provide new low area solution for very large scale integration (VLSI) designers. At transistor level, STATIC CMOS logic style can give better results when we design N-types of circuits and then select the best one over others. In this project the proposed Adder has been designed by using STATIC CMOS 180nm TECHNOLOGY. Layout for Adder has been implemented by using tanner tool.**

Index Terms— **24t circuit, Inverter, Static Cmos, Ripple carry adder.**

I. INTRODUCTION

Now we need to design a Adder by following our own technique such that low power and low area is achieved. We have designed Adder by using STATIC CMOS logic style, it has advantage of low power consumption but dis-advantage of area with respect to number of transistors, so here we will have the task to design the Adder with less number of transistors. Logic style like PTL (Pass Transistor Logic) has advantage of less number of transistors but it is difficult to layout.

Adder is going to add N bits of A and N bits of B and gives the N+1 bits result out of which N-bits are the SUM resulting bits and 1-bit is the CARRY resulting bit.

We need to design the N-bit ripple carry adder and the operation starts from LSB(Least Significant Bit) to MSB(Most Significant Bit) that is after checking the status of LSB(Least Significant Bit) then it's CARRY OUT will be the CARRY IN to the(LSB(Least Significant Bit)+1)and finally (MSB(Most Significant Bit)-1)'s CARRY OUT will be the CARRY IN to the MSB(Most Significant Bit).

II. RIPPLE CARRY ADDER

Universal 1-bit FULL-ADDER by using STATIC CMOS Logic style needs 28 number of Transistors out of which 14 will be in the pull-down network and 14 in the pull-up network.

so for a N-bit FULL-ADDER it takes N*28 number of Transistors.

We need to reduce the transistor count not by using some other logic styles which by default takes less number of transistors, so started investigating from LSB(Least Significant Bit) how the functionality has been achieved then we found that out of those 28 number of Transistors there are 2 inverters and remaining is one 24T Circuit and one inverter is needed to achieve resulting SUM OUTPUT and other inverter is needed to achieve resulting CARRY OUTPUT.

There is difference between SUM OUTPUT and CARRY OUTPUT that is SUM OUTPUT is the final resulting OUTPUT but CARRY OUTPUT is not the final resulting OUTPUT, so we cannot modify the SUM OUTPUT section of 28 Transistor 1-bit FULL-ADDER arrangement of LSB(Least Significant Bit). we found that extra inverter which is used to achieve CARRY OUTPUT is not necessary, so LSB(Least Significant Bit) arrangement of N-bit Ripple Carry Adder needs one 24T Circuit and one inverter.

Now we need to design the (LSB(Least Significant Bit)+1) section of N-bit Ripple Carry Adder but here if input's of A and B are '1' and '1' and if CARRY INPUT is '1' then normally we should get SUM OUTPUT='1' and CARRY OUTPUT='1' but we modified the design in LSB(Least Significant Bit) such that sum output will be 1 and carry output will be 0.

The truth table arrangement is not normal and if we try to achieve the functionality for this modified truth table arrangement then the Transistor count is very high, so we need to do something such that Transistor count can be reduced .

we found that if A and B inputs of (LSB(Least Significant Bit)+1) section are inverted and these inverted inputs and CARRY OUTPUT of LSB(Least Significant Bit) section as the inputs to the (LSB(Least Significant Bit)+1) section then the 24T Circuit satisfy's our functionality requirement and gives the output in true form.

Now we need to design the (LSB(Least Significant Bit)+2) section of N-bit Ripple Carry Adder and it is just the Replication of LSB(Least Significant Bit) section only with input and output names changed and both the sections have equal number of Transistors and the circuit structure is also the same so that it can be reused.

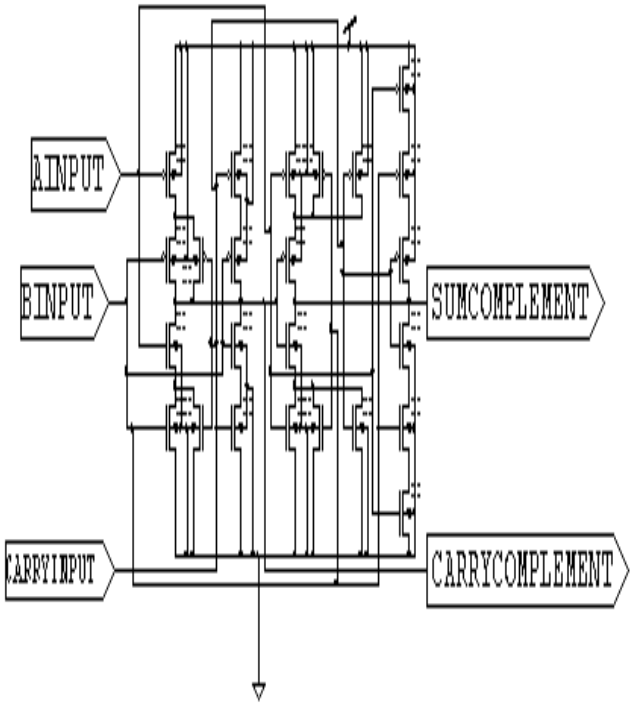

Fig. 1 24T Circuit

Now we need to design the (LSB(Least Significant Bit)+3) section of N-bit Ripple Carry Adder and it is just the Replication of (LSB(Least Significant Bit) +1) section only with input and output names changed.

Design which we presented can also be extended up to N-bits out of which N/2 sections needs 26 Transistors in each section and N/2 sections needs 28 Transistors in each section (N is even).

There are 2 Cells in this adder named 24T Circuit and Inverter. 24T Circuit has three inputs, two outputs and gives the result of SUM and CARRY OUTPUTS but with complementary values when all the inputs are in true form.

When all the inputs are in complementary form then the SUM and CARRY outputs will be in true form. Maximum Number of Transistors in series either in PULL-UP Network or PULL-DOWN network are 3. So maximum fan-in is 3 and fan-out is 1.we need finally N number of 24T Circuits and N+N/2 inverters for N-Bit Adder.

In LSB(Least significant bit)If (SUM OUTPUT and CARRY OUTPUT) are "00" then S0 is LOW and C0 is HIGH, "01" S0 is LOW and C0 is LOW, "10" S0 is HIGH and C0 is HIGH, "11" S0 is HIGH and C0 is LOW.

In LSB(Least significant bit+2)If (SUM OUTPUT and CARRY OUTPUT) are "00" then S2 is LOW and C2 is HIGH, "01" S2 is LOW and C2 is LOW, "10" S2 is HIGH and C2 is HIGH, "11" S2 is HIGH and C2 is LOW.

In LSB(Least significant bit+1) If (SUM OUTPUT and CARRY OUTPUT) are "00" then S1 is LOW and C1 is LOW, "01" S1 is LOW and C1 is HIGH, "10" S1 is HIGH and C1 is LOW, "11" S1 is HIGH and C1 is HIGH.

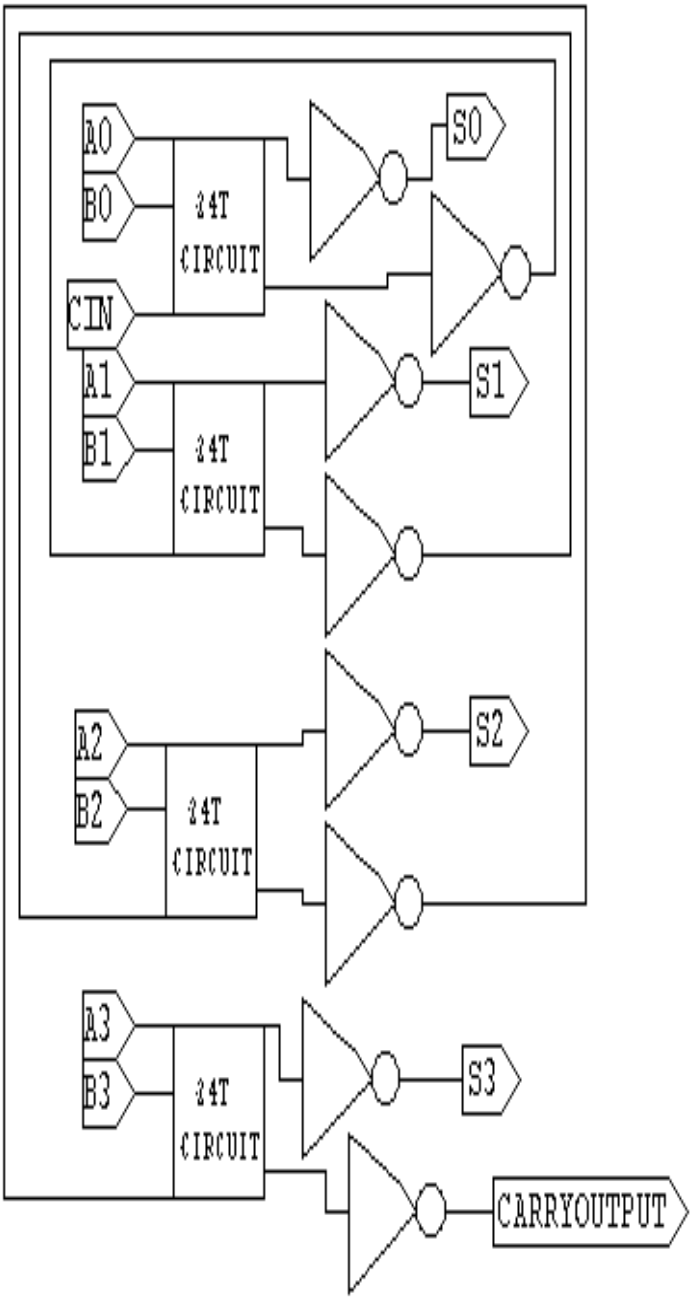

Fig. 2 Universal 4-Bit Ripple Carry Adder.

In MSB(Most significant bit) If (SUM OUTPUT and CARRY OUTPUT) are "00" then S3 is LOW and CARRY OUTPUT is LOW, "01" S3 is LOW and CARRY OUTPUT is HIGH, "10 " S3 is HIGH and CARRY OUTPUT is LOW, "11" S3 is HIGH and CARRY OUTPUT is HIGH. So total number of transistors for an N-BIT ADDER (N is even) will be (N*28-N).

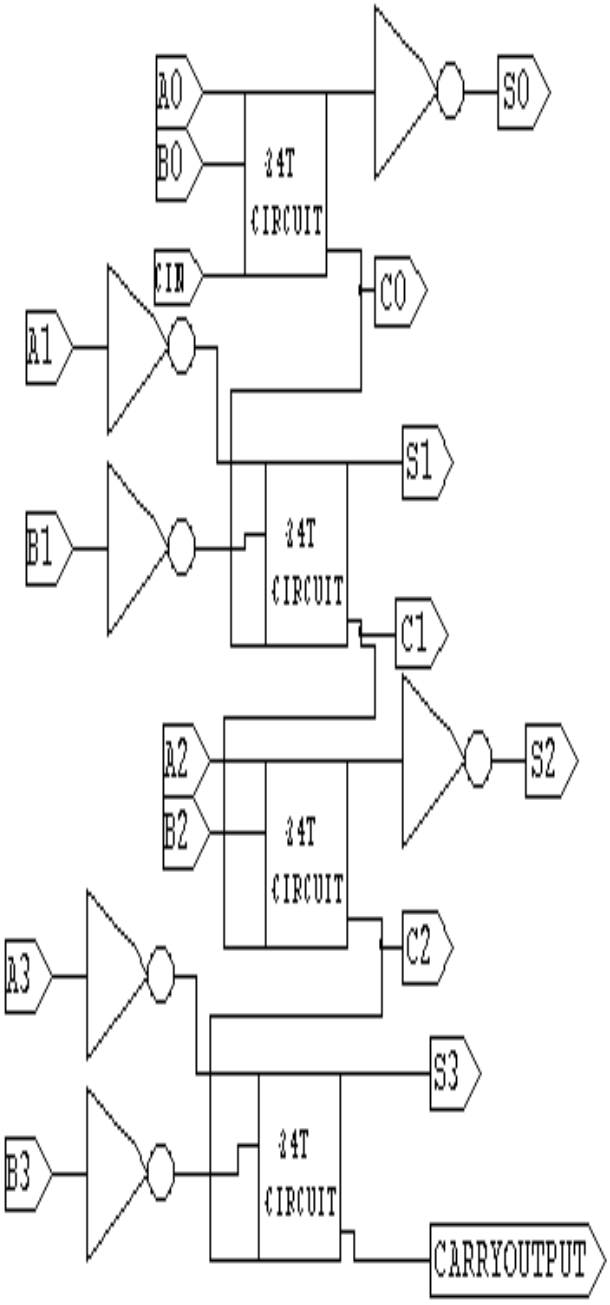

Fig. 3 Proposed 4-Bit Ripple Carry Adder Extendable to N-Bit.

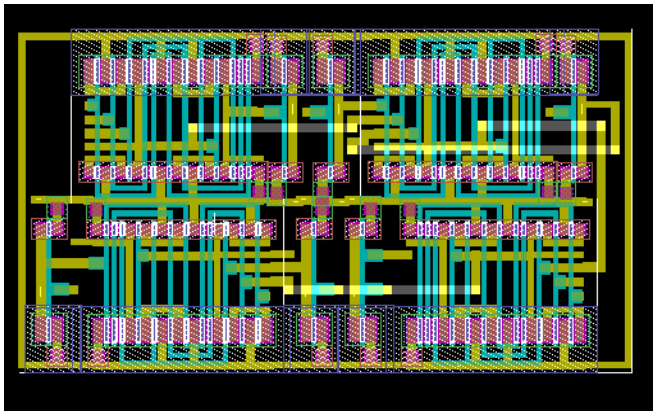

Fig. 4 Full custom layout of the 4-bit Ripple Carry Adder

III. STATIC CMOS

STATIC CMOS has the advantage of high noise immunity and low power consumption but it needs more number of transistors. STATIC CMOS has advantage of full output voltage swing at every node in the circuit, so we can easily differentiate between output voltage high logic level and output voltage low logic level and this will be even more beneficial when the technology is scaled down because the supply voltage will be lowered. It is recommended that not more than four number of transistors are there in series either in PULL-UP or PULL-DOWN region as delay is going to be worse.

Here the challenge also Lies in Designing the layout for adder by using STATIC CMOS cells and Advantage of using STATIC CMOS only is we have Power rails so that we can Merge the cells comfortably and it will also allow for efficient manual placement which in turn also gives efficient routing resulting in the optimization of layout area as well as post layout timing simulation.

IV. PERFORMANCE ANALYSIS

Implementation of 4-bit Ripple Carry Adder has been done using STATIC CMOS logic style. Table1 shows AREA comparison of Universal Ripple Carry Adder and Proposed Ripple Carry Adder. Power dissipation comparison for 4-bit Ripple Carry Adder using Universal Ripple Carry Adder and Proposed Ripple Carry Adder for various supply voltage (VDD) are shown in TABLE2.

This table clearly shows that Proposed Ripple Carry Adder has less power dissipation than Universal Ripple Carry Adder over various supply voltage (VDD).

The Adder which we designed using STATIC CMOS logic uses less number of transistors. It uses (N*0.9)% less

area (number of transistors) than Universal Ripple Carry Adder.

Layout Area of the adder is 30.7 µm × 17 µm equal to 521.90 µm² which is far better than many of the adder's mentioned in the references.

TABLE1 COMPARISION OF AREA IN TWO DESIGNS

N-Bit	Universal Design (Static cmos)	Proposed Design (Static cmos)
Area(number of transistors)	N*28	(N*28)-N

V. CONCLUSION

Area, Power and speed are the important Design constraints. Speed can be achieved by default because carry computation has been modified in our proposed design and area is also minimized as well and we can expect better power consumption since the switching activity will be reduced as well as active number of transistors also will be reduced since we have taken up to 4-bit only optimization of power might be less but if we go for larger size then Proposed Design will be very effective with respect to power.

It shows a 4-bit Ripple Carry Adder of the proposed technique only needs 108 transistors, the technique which we presented can be easily extendable up to N-bit. N number of transistor count has been reduced for an N-bit proposed Ripple Carry Adder when compared to N-bit Universal Ripple Carry Adder.

ACKNOWLEDGEMENT

This material is based upon work supported by the faculty of Raghu engineering college. Any opinions, findings, conclusions or recommendations expressed in this material are those of the authors and do not necessarily react the views of Raghu Engineering College.

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