# Implementation and Study of Reversible Binary Comparators

**Harith M, C Vasanthanayaki**

***Abstract*—Reversible logic contains a feature of recovering bit loss from unique input-output mapping. Using traditional (irreversible) logic gates always lead to energy dissipation because of loss of information bits. Thus the recovering bit loss feature of reversible logic reduces power dissipation. This will eventually lead to higher densities and speed. Comparators are used in most of the digital computation systems like micro controllers and microprocessors, communication systems, encryption and decryption devices and many more. This extensive use of comparators demands low power and high speed. For meeting this demand, many reversible comparators are being proposed. In this paper, four efficient reversible comparators are implemented and their performance is analyzed. A comparative study has been done and the best performer is determined.**

***Index Terms*—Binary comparators, reversible Logic, quantum computing**

## I. INTRODUCTION

One of the serious problem faced by today's computer chips is power dissipation and therewith heat generation. The fundamental reason for power dissipation came into light from the observations made by Landauer in 1961 [1]. Landauer proved that using traditional (irreversible) logic, gates always lead to energy dissipation. More precisely, exactly kT log 2 Joules of energy is dissipated for each information bit lost during the irreversible operation (where k is the Boltzmann constant and T is the temperature). While this amount of power currently does not sound significant, it may become crucial considering the fact that millions of operations are performed and thereby leading to loss of lot of information bits.

Bennett showed that energy dissipation is reduced or even eliminated if computation becomes information-loss less [2]. The amount of energy dissipated in a system has a direct relationship to the number of bits erased during computation. Reversible computation in a system can be performed only when the system consists of reversible gates. These circuits generate a unique output vector from each input vector, and vice-versa. In a reversible circuit, there is a one-to-one mapping between input and output vectors [3], [4]. The extreme importance of Bennett's theorem [2] lies in the fact that every future technology would have to use reversible gates to reduce power.

Comparison of binary numbers finds diverse range of applications in general purpose microprocessors, communication systems, encryption device, sorting networks etc.. In traditional binary comparators, traditional (irreversible) logic gates are used and it dissipate power as information bits are lost. Reversible Binary comparators dissipates less power. Due to its significance, several reversible comparator circuits have been proposed. An efficient reversible logic circuit should be designed with minimum number of gates, Constant inputs, Garbage outputs and Quantum cost [5]. In this work, four existing efficient reversible binary comparators are implemented and analyzed. From comparison of parameters like power, area, delay, minimum number of gates, Constant inputs, Garbage outputs and Quantum cost, the best one is identified. Thus aiding the researchers in choosing a suitable comparator.

The paper is organized with the following sections: Section II describes reversible gates and the definitions of parameters being compared. Section III gives details about four reversible comparators. Section IV gives the comparisons of all the reversible comparator circuits. Finally, the paper is concluded in Section V.

## II. BASIC DEFINITIONS AND LITERATURE OVERVIEW

### *A. Reversible Gates*

Reversible gates are gates that have the same number of inputs and outputs and are one-to-one mappings between vectors of inputs and outputs, thus the vector of input values can be always uniquely reconstructed from the vector of output values. Fig. 1 shows a k x k reversible gate.

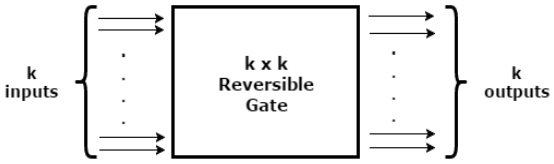



Fig. 1: k x k Reversible gate

The reversible gates used in this paper are:

1) NOT Gate

NOT gate [Fig. 2] is the simplest reversible gate with zero Quantum cost. It is a 1 x 1 reversible gate.

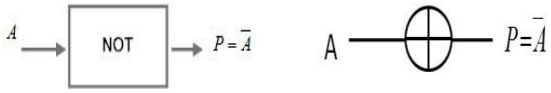
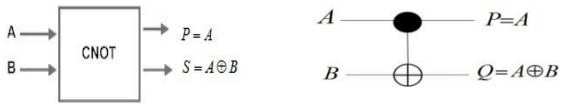



Fig 2: NOT gate

2) FEYMAN Gate

Fig. 3 shows a 2 x 2 Feynman gate [6]. Quantum cost of a Feynman gate is 1.

Fig. 3: FEYMAN Gate

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3) TOFFOLI Gate

Toffoli gate (Fig. 4) [7] which is a 3x 3 gate with inputs (A, B, C) and outputs P = A, Q = B, R = AB⊕ C. It has Quantum cost 5.

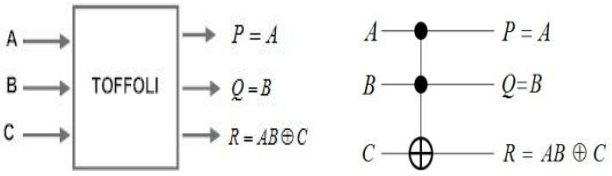



Fig. 4: TOFFOLI Gate

4) PERES Gate

Peres gate [8] which is a 3 x 3 gate having inputs (A,B,C) and outputs P = A; Q = A ⊕ B; R = AB⊕C. It has Quantum cost 4.

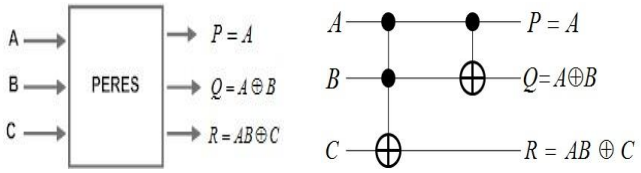



Fig. 5: PERES Gate

5) TR Gate

TR gate [9] is a 3 x 3 gate and its logic circuit and its quantum implementation is as shown in the Fig.6. It has quantum cost 6.

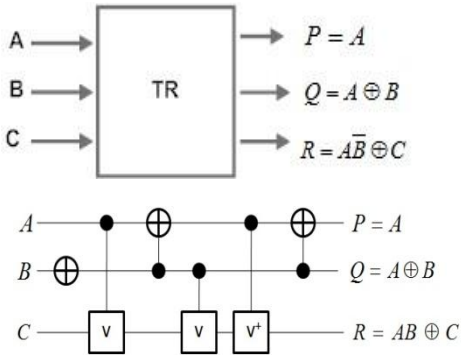



Fig. 6: TR Gate

6) BJS Gate

BJS gate [10] is a 4 x 4 gate with inputs (A, B, C, D) and outputs $P = A, Q = A\overline{C} \oplus \overline{A}B, R = \overline{A}C \oplus AB$, $S = \overline{A \oplus B \oplus C \oplus D}$. It has a quantum cost of 6.

7) HLN Gate

HLN gate [10] is a 3 x 3 gate with inputs (A, B, C) and outputs $P = A, S = \overline{A \oplus B \oplus C}$, $R = \overline{A}C \oplus AB$. It has a quantum cost of 5.

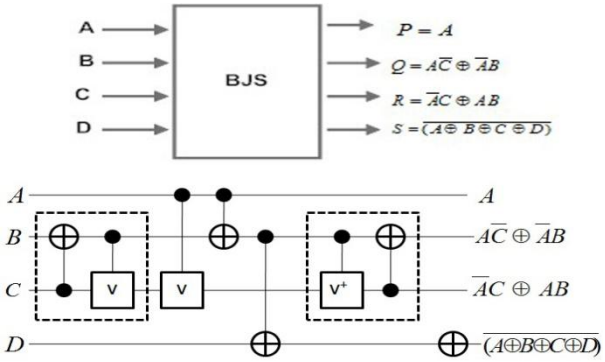



Fig. 7: BJS Gate

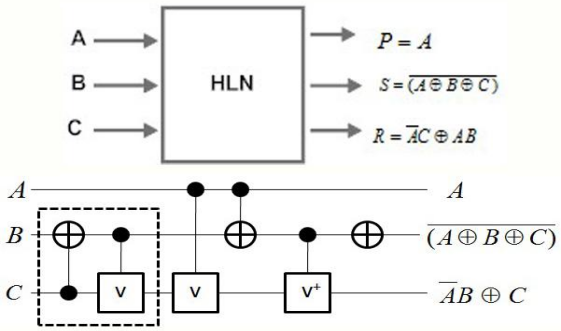



Fig. 8: HLN Gate

*B. Quantum Cost*

Quantum cost refers to the cost of a circuit in terms of elementary quantum gates [11]. The most used elementary quantum gates are the NOT gate (a single qubit is inverted), the CNOT gate (the target qubit is inverted if the single control qubit is 1), the controlled-V gate (also known as a square root of NOT, since two consecutive V operations are equivalent to an inversion), and the controlled-$V^+$ gate (which performs the inverse operation of the V gate and thus is also a square root of NOT [11]).

*C. Delay*

The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. This definition is based on the following two assumptions [12]: firstly, each gate performs the computation in one unit time. Secondly, all inputs to the circuit are known before the computation begins.

*D. Garbage Output*

Garbage Output is the unwanted or unused output of a reversible gate (or circuit). Garbage output(s) is (are) needed only to maintain the reversibility [12].

*E. Power*

The power dissipation of a logic circuit is the summation of individual power dissipations of each gate of the circuit.

*F. Area*

The area of a logic circuit is the summation of individual

area of each gate of the circuit.

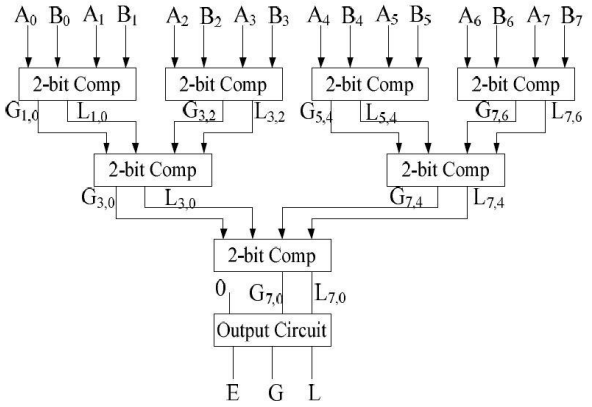
## III. REVERSIBLE BINARY COMPARATORS

In 2010, Himanshu Thapliyal et al. proposed the idea of tree based design of a reversible comparator [13]. This design is based on a new reversible gate called the TR gate [Fig. 6]. This comparator has a binary tree structure in which each node is a 2-bit comparator cell that will compare two 2-bit numbers *A* ($A_1A_0$) and *B* ($B_1B_0$) to generate two outputs $G_{1;0}$ and $L_{1,0}$ indicating $A > B$ and $A < B$ respectively. A 2-bit comparator design was also proposed by them which use R-Bcomp modules. The R-Bcomp module uses TR gates and is shown in the figure 9b.The R-Bcomp module is a circuit which generates $\bar{e} = A_1 \oplus B_1$ where e indicates $A_1 = B_1$, $l_1 = \bar{A}_1 B_1$ which indicates $A_1 < B_1$, and $g_1 = A_1 \bar{B}_1$ indicates $A_1 > B_1$. The R-Bcomp is basically a 1-bit comparator which generates greater, lesser and equal signals and are combined together using TR gates according to the equations (1) to design a 2-bit comparator.

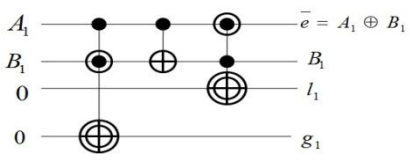
$$L_{1,0} = l_1 \oplus e \cdot l_0$$
$$G_{1,0} = g_1 \oplus e \cdot g_0 \qquad (1)$$

The 2-bit reversible comparator design using the R-Bcomp modules is shown in Fig. 9c. The design of 8-bit comparator along with a reversible output circuitry is shown in Fig. 9a.Output circuitry (Fig. 9d) generate $E = \overline{L + G}$ signal.

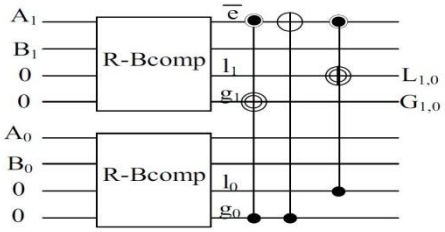
In 2011, Rangaraju H G et al. proposed a serial based reversible comparator in their work titled, "Design of low power Reversible Binary Comparator" [14]. The design is based on the reversible gates such as NOT, Feynman (CNOT) and Peres (PG).



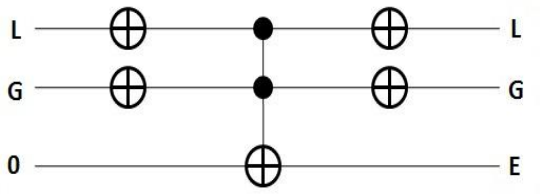

(a) 8-bit reversible Comparator




(b) R-Bcomp Design




(c) 2-bit reversible Comparator

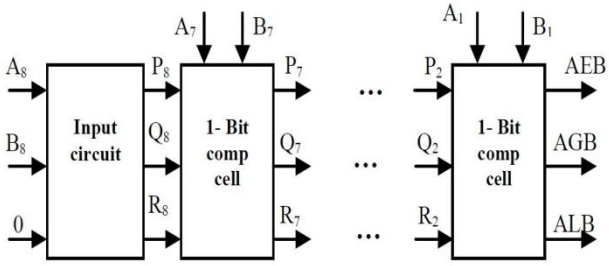



(d) Reversible implementation of output circuit

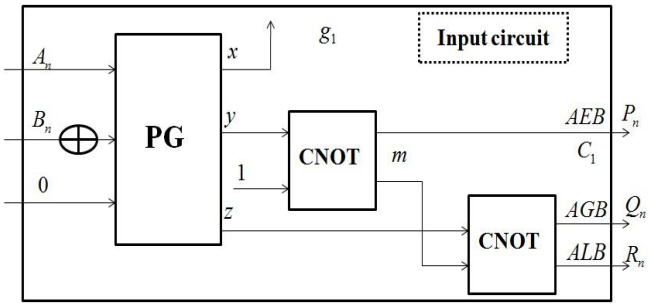
Fig. 9: Design of 8-bit reversible Comparator [13]

In this design, a*n*-bit binary comparator is designed using two types of blocks, an input circuit block andn 1x1-bit reversible comparator blocks. The design of a 8-bit comparator is shown in the Fig.10a. First stage is input circuit stage which compares the MSB bits of the two numbers, here $A_8$, $B_8$. Second stage is a one-bit comparator cell in which the result of the first stage and the input bits $A_7$, $B_7$ is compared and so on. The final stage compares the output of the seventh stage and the LSB bits $A_1$, $B_1$ and produces the final output of the 8-bit numbers A and B. The input circuit to binary comparator using reversible logic is shown in Fig.10b. The reversible input circuit is designed using one PG, two CNOT and one NOT gates. The input circuit alone can function as one-bit comparator and has one garbage output and two constant inputs. Block A shown in Fig. 10d is used in one-bit comparator cell, which consists of two NOT, one PG and one CNOT gates. The outputs of block A are $C_1 = A\bar{B}$ and $C_2 = \bar{A}B$. 1-bit reversible binary comparator consists of three PG and four CNOT gates. It has five inputs viz., $P_n$ (AEB), $Q_n$ (AGB), $R_n$ (ALB), $A_{n-1}$and $B_{n-1}$ and three outputs $Q_{n-1}$ i.e., AGB, $P_{n-1}$ i.e., AEB and $R_{n-1}$i.e., ALB as shown in the Fig. 10c.

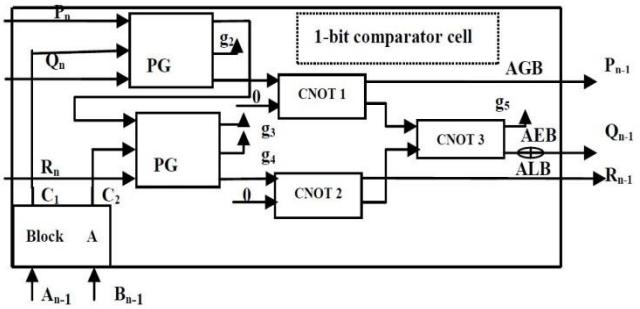
In 2012, Chetan Vudadha et al. in their paper, "Design of Prefix-Based Optimal Reversible Comparator" [16], proposedan improved version of the tree based architecture.



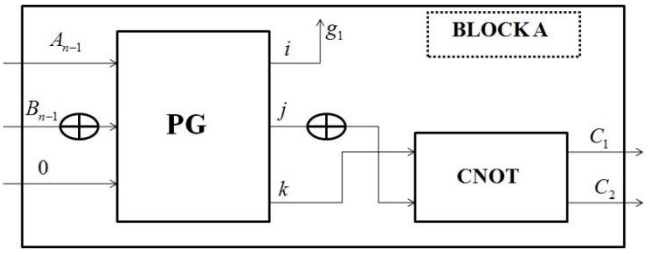

(a) 8-bit reversible Comparator




(b) Reversible implementation of input circuit




(c) 1-bit reversible Comparator




(d) Block A Design

Fig. 10: Design of 8-bit reversible Comparator [14], [15]

The basic idea of the design is to generate $g_i$ and $e_i$ signals for each operand bit pairs $A_i$ and $B_i$, where, $g_i$ (greater) indicates $A_i > B_i$ and $e_i$ (equal) indicates $A_i = B_i$. For an example, the design of an 8-bit comparator is shown in the Fig. 11a. In the first stage, the equal and greater than signals for $i^{th}$ bit are generated as given by the equations (2):

$$e_i = A_i \oplus \overline{B}_i$$
$$g_i = A_i \cdot \overline{B}_i \qquad (2)$$

In the second stage, the black cells generate greater and equal signals out of each bit positions are grouped together by grouping logic which is based on idea presented in [17]. First stage grouping is done based on the equations (3).

$$G_{i,j} = g_j + e_j \cdot g_i$$
$$E_{i,j} = e_j \cdot e_i \qquad (3)$$

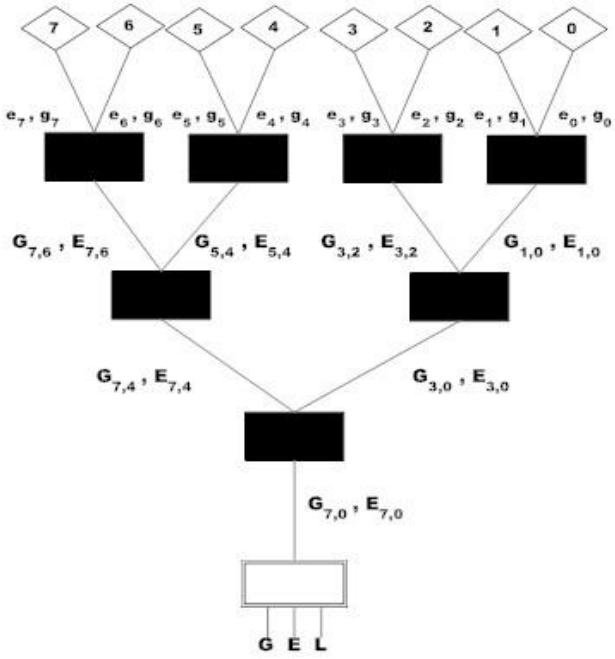
$g_i$ and $e_i$ indicate the greater and equal signals for $i^{th}$ operand bits. $g_j$ and $e_j$ indicate the greater and equal signals for $j^{th}$ operand bits such that $j > i$ (i.e. $j^{th}$ bits are significant than $i^{th}$ bits). At the intermediate stage of grouping the greater and equal signal grouping is defined by the equations

$$G_{i,j} = G_{i,k} \oplus E_{i,k} \cdot G_{k-1,j}$$
$$E_{i,j} = E_{i,k} \cdot E_{k-1,j} \qquad (4)$$

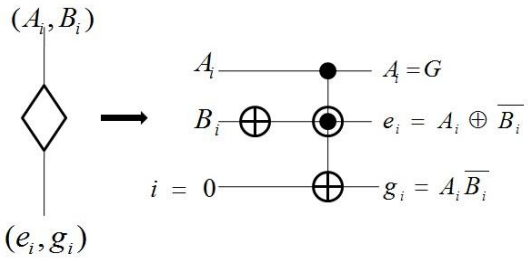
where $i > k > j$. In the final stage the final greater and equal signals are further used for generation of final lesser signal L using the NOR operation as given below

$$L_{N0} = E_{N0} + G_{N0} \qquad (5)$$

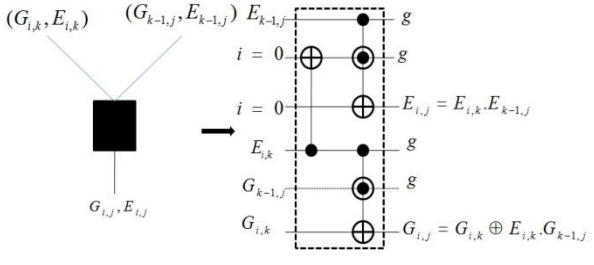
Reversible implementation of first stage, black cell and final stage is shown in Fig. 11.



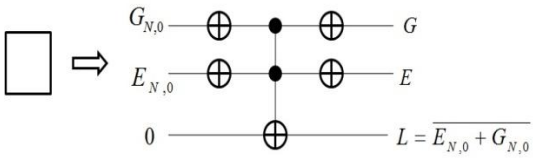

(a) 8-bit reversible Comparator [16]



(b) Reversible implementation of first stage



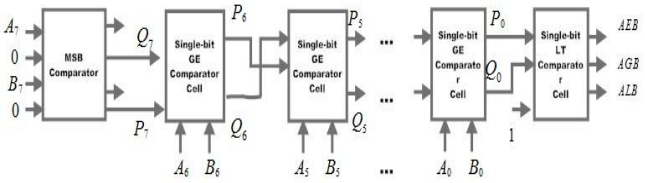
(c) Realization of Black cell used for grouping



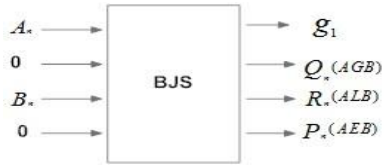

(d) Reversible implementation of output circuit

Fig. 11: Design of 8-bit reversible Comparator [16]

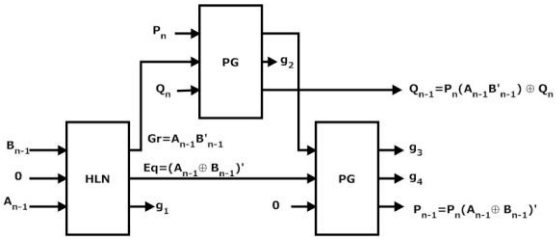
In 2014, Hafiz Md. Hasan Babu et al. proposed a new serial Binary comparator in their paper titled 'Approach to design a compact reversible low power binary comparator' [10]. To construct the optimized n-bit comparator, two new reversible gates, namely BJS (Babu-Jamal-Saleheen) gate [Fig. 7] and HLN (Hasan-Lafifa-Nazir) gate [Fig. 8] were proposed. The design consists of three main blocks: MSB comparator cell, single-bit GE (greater or equal) comparator cell and single-bit LT (less than) comparator cell. An MSB comparator cell [Fig. 12b] is used for comparing the $n^{th}$ bit (MSB) of two n-bit numbers and it consists of only one BJS gate. It takes MSBs of two binary numbers $A_n$, $B_n$ and sets two constant inputs as 0. It produces three outputs based on the bits present at the input level. ALB ($R_n$), AGB ($Q_n$) and AEB ($P_n$) are the three outputs produced from this circuit. A single-bit GE (greater or equal) comparator cell[Fig. 12c] which consists of one HLN gate and two Peres Gates has been designed to generate greater and equal signal for the remaining (*n-1*) bits of two numbers with the previous comparison result of MSB. It takes $(n-1)^{th}$ bits of two binary numbers A and B and two more inputs $P_n$ and $Q_n$ from previous comparison result. Together they work to produce two outputs AEB ($P_{n-1}$) and AGB ($Q_{n-1}$) which indicates whether the given numbers A and B are equal or greater than each other. A single-bit LT (less than) comparator cell [Fig. 12d] is designed to determine the less than signal. The circuit requires two Feyman Gates. The design of an 8 bit comparator is given in Fig. 12a.



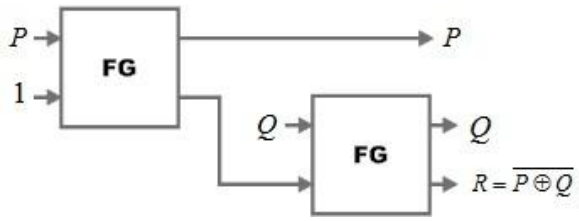

(a) 8-bit comparator circuit




(b) BJS as MSB comparator circuit




(c) Single-bit GE (greater or equal) comparator cell




(d) Single-bit LT (less than) comparator cell

Fig. 12: Design of 8-bit reversible Comparator [10]

## IV. COMPARISONS

The Reversible binary comparators described in the above section are implemented in 180nm technology using Cadencetool and synthesized. The comparators are compared in terms of Number of gates [Table I], Number of garbage outputs [Table II], Quantum Cost [Table III], Delay [Table IV], Power [TABLE V] and Area [Table VI] for 2-bit, 4-bit and 8-bit.

Table I: Number of Gates

| No. of bits | H.Babu et al.[10] | Thapliyal et al.[13] | Rangaraju et al.[14], [15] | Vudadha et al [16] |
|---|---|---|---|---|
| 2 | 6 | 18 | 10 | 6 |
| 4 | 12 | 36 | 24 | 14 |
| 8 | 34 | 72 | 52 | 30 |

Table II: Number of Garbage Outputs

| No. of bits | H.Babu et al.[10] | Thapliyal et al.[13] | Rangaraju et al.[14], [15] | Vudadha et al [16] |
|---|---|---|---|---|
| 2 | 5 | 6 | 6 | 6 |
| 4 | 13 | 18 | 16 | 16 |
| 8 | 29 | 42 | 36 | 36 |

Table III: Quantum Cost

| No. of bits | H.Babu et al.[10] | Thapliyal et al.[13] | Rangaraju et al.[14], [15] | Vudadha et al [16] |
|---|---|---|---|---|
| 2 | 21 | 22 | 27 | 28 |
| 4 | 47 | 54 | 63 | 56 |
| 8 | 99 | 118 | 135 | 112 |

Table IV: Delay in ps

| No. of bits | H.Babu et al.[10] | Thapliyal et al.[13] | Rangaraju et al.[14], [15] | Vudadha et al [16] |
|---|---|---|---|---|
| 2 | 2951 | 2886 | 3438 | 2852 |
| 4 | 3364 | 3299 | 5133 | 3149 |
| 8 | 4517 | 4311 | 8522 | 3479 |

## V. CONCLUSION

Four existing comparators are implemented and synthesized in 180nm technology using Cadence tool. From the comparative analysis, it can be inferred that the reversible binary comparator circuit proposed by Hafiz Md. Hasan Babu et al. in their work titled 'Approach to design a compact reversible low power binary comparator' [10] has been constructed with the optimum number of gates, garbage outputs and quantum cost. It also shows considerable improvement in power and area consumed. The only parameter of this that do not outperforms the others is the delay but there is not much difference. As [13], [16] both are tree-based design, they require $O(\log_2 n)$ delay, whereas [10], [14], [15] requires O(n) delay. The comparison of all parameters for an n-bit comparator is shown in the table VII. Considering the optimization of all the parameters, the circuit outperforms the existing ones in terms of scalability and efficiency.

Since comparison of two numbers is useful in manyapplications, this comparative study will help the researchers in choosing a suitable comparator. From analysis of the design in the paper by Chetan Vudadha et al. [16], it can be observed that more number of gates are used to realize the black cell. If the number of gates in the black cell is reduced, it can provide a significant decrease in the power and area consumed. Also since it has a prefix based tree architecture, delay will also be less. So a more efficient binary reversible comparator can be developed by designing a new reversible gate that will replace the gates used in black cell.

Table V: Total Power in nW

| No. of bits | H.Babu et al.[10] | Thapliyal et al.[13] | Rangaraju et al.[14], [15] | Vudadha et al [16] |
|---|---|---|---|---|
| 2 | 6851.108 | 13906.177 | 9565.376 | 6036.276 |
| 4 | 9277.133 | 38547.896 | 18658.098 | 15955.442 |
| 8 | 15329.660 | 91141.660 | 39995.277 | 28965.655 |

Table VI: Area in $cm^2$

| No. of bits | H.Babu et al.[10] | Thapliyal et al.[13] | Rangaraju et al.[14], [15] | Vudadha et al [16] |
|---|---|---|---|---|
| 2 | 166 | 359 | 253 | 186 |
| 4 | 296 | 1025 | 605 | 393 |
| 8 | 556 | 2355 | 1311 | 805 |

Table VII: Comparison of parameters for n-bit

| Parameters | H.Babu et al.[10] | Thapliyal et al.[13] | Rangaraju et al.[14], [15] | Vudadha et al [16] |
|---|---|---|---|---|
| Number of Gates | 3n | 9n | 7n-4 | 4n-2 |
| Number of Garbage Outputs | 4n-3 | 6n-6 | 5n-4 | 5n-4 |
| Quantum Cost | 13n-5 | 18n-9 | 16n-10 | 14n |
| Delay | 256.5n+2438 | 413 log 2n | 847.5n + | 297 log |
| | | + 2473 | 1743 | 2n + 2555 |
| Power | 1213.01 n +4425 | 12320.86n-10735.5 | 4546.36n+ 472.65 | 4959.6n-3882.99 |
| Area | 90n-14 | 333n-306 | 176n-99 | 104n-20 |

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