Innovative Design of CMOS 8-bit Comparator using conditional tracking for low area

M. Meena Kumari, Bhaskara Rao Doddi, G.Sunil Kumar

Abstract— **In this paper we are going to design a circuit based on conditional tracking in which we will not realize the circuit based upon the expressions but off course the circuit which we have designed will have internally some expression. We are not going to do any Boolean algebra manipulations and we will only be tracking the conditions and then convert that condition into CMOS circuit and we are going to utilize more the AOI and OAI circuits and we ensure that not more number of transistors are in series. Our design does not fix initially blocks going to be used and in our design approach whatever the blocks needed that we will be using. N-bit output can be obtained after N cell delays but speed not only depends on the number of levels but also on the hardware requirements at that levels. Maximum number of inputs in our circuits are 4 and Maximum Fan-out will be 1. Transistor reduction was achieved in range of 16% to 53% with the existing designs.our design is low area with respect to number of transistors that too in Static CMOS. Total transistor count for N-bit comparator is 6+[10*(N-1)]+10+[12*(N-1)]+4.Tanner tools are being used for schematic entry and for simulation.**

Index Terms— Comparison Cell, MUX21, Magnitude COMPARATOR, STATIC CMOS.

I. INTRODUCTION

Low density parity check needs comparators and was designed by gallager in 1962[1]. HUANG developed priority encoder to encode the compared bits[2]. CHENG employed conditional sum adder to know greater and less then conditions[3]. J-Y KIM and H-J YOO proposed a design which is even more efficient with number of transistors[4].

Asynchronous design is complicated as clock will not be applied synchronously[5]. Cmos will have good logic1 and logic0 regions as almost 30% of supply voltage treated as logic0 and as well as logic1 regions with only 40% left for unknown regions so,mostly Cmos based Digital IC are the choice of Digital Designers[6].If we are more concerned with Speed for our Design then make sure that number of levels in our circuit are less and also hardware that is required in that levels is also a concern[7].

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Any expression can be directly translated into equivalent Cmos Circuit by following De-morgan's law but to do so we need to have a expression[8]. Geetanjali Sharma comparator is based on mux based design and it cannot differentiate between < and = condition[9].Saleh Abdel Hafeez proposed high speed comparator with less number of active transistors at expense of Area[10]. Hensley proposed design which was too slow[11]. Perri design was not power efficient and supports one of < and > status.

Designers can chose gate diffusion input technique in which transistor count can be reduced but has logic level degradation corresponding to the threshold voltage loss which will effect the speed and sometimes data wont be reaching the destination instead Static cmos though by default takes huge transistor count we want to design in static and reduce the count.

II. MAGNITUDE COMPARATOR

Comparator is going to compare 8 bits of A(A7 to A0) and 8 bits of B(B7 to B0) and decides whether ALTB(A<B) or AGTB(A>B) or AEB(A=B). we can design the circuit for any of the two conditions then third condition can be achieved and we have chosen AGTB(A>B) and AEB(A=B) and finally two input nor gate can be utilized to form the ALTB(A<B) condition. Conditional Tracking

Any digital logic circuit can be designed using basic logic gates or universal gates but they all based upon Boolean algebra manipulations and we need to find out the expression. Here we propose new method for designing circuits in CMOS.we need to know what are all the conditions for AGTB(A>B) to become true and there will be 8 conditions for 8-bit comparator and in similar manner N conditions for N-bit comparator.

Condition1: A[7]>B[7]
Condition2: A[6]>B[6]and A[7]=B[7]
Condition3:A[5]>B[5]and A[7:6]=B[7:6]
Condition4:A[4]>B[4]and A[7:5]=B[7:5]
Condition5:A[3]>B[3]and A[7:4]=B[7:4]
Condition6:A[2]>B[2]and A[7:3]=B[7:3]
Condition7:A[1]>B[1]and A[7:2]=B[7:2]
Condition8:A[0]>B[0]and A[7:1]=B[MSB:1]
ConditionN:A[LSB]>B[LSB]andA[MSB:LSB+1]=
B[MSB:LSB+1]

Our design has transition of 01010101 means to say that one bit output which is x0 will be 0 if A>B is true and two bit output which is x1 will be 1 when A>B and for all odd output positions we will get 0 and for all even bit positions of output will be 1.

$x0_{=(A}15.B15')'$

$x_1=(x_0.(B_{14}+y_0+A_{14}'))'$

$x_2=(x_1+(y_1A_{13}B_{13}'))'$

$x_3=(x_2.(B_{12}+y_2+A_{12}'))'$

$x_4=(x_3+(A_{11}.y_3B_{11}'))'$

$x_5=(x_4.(y_4+B_{10}+A_{10}'))'$

$x_6=(x_5+(A_9.y_5.B_9'))'$

$x_7=(x_6.(B_8+y_6+A_8'))'$

Above x[0] gives condition1 which is one bit comparison, x[1] gives conditions 1,2 which is two bit comparison. x[2] gives conditions 1,2,3 which is three bit comparison.x[3] gives conditions 1,2,3,4 which is four bit comparison. x[4] gives conditions 1,2,3,4,5 which is five bit comparison.x[5] gives conditions 1,2,3,4,5,6 which is six bit comparison. x[6] gives conditions 1,2,3,4,5,6,7 which is seven bit comparison. x[7] gives conditions 1,2,3,4,5,6,7,8 which is eight bit comparison.

we need to know what are all the conditions for AETB(A=B) to become true there will be 8 conditions for 8-bit comparator and in similar manner K conditions for K-bit comparator.

Condition1: A[7]=B[7]

Condition2: A[7:6]=B[7:6]

Condition3: A[7:5]=B[7:5]

Condition4: A[7:4]=B[7:4]

Condition5: A[7:3]=B[7:3]

Condition6: A[7:2]=B[7:2]

Condition7: A[7:1]=B[7:1]

Condition8: A[7:0]=B[7:0]

ConditionN: A[MSB:LSB]=B[MSB:LSB]

our design has transition of 01010101 means to say that one bit output which is y0 will be 0 if A=B is true and two bit output which is y1 will be 1 when A=B and for all odd output positions we will get 0 and for all even bit positions of output will be 1

$y_0=(A_{15}.B_{15}+(A_{15}+B_{15})')'$

$y_1=(y_0+(A_{14}.B_{14})'(A_{14}+B_{14}))'$

$y_2=(y_1((A_{13}+B_{13})'+(A_{13}.B_{13})))'$

$y_3=(y_2+(A_{12}.B_{12})'(A_{12}+B_{12}))'$

$y_4=(y_3((A_{11}+B_{11})'+(A_{11}.B_{11})))'$

$y_5=(y_4+(A_{10}.B_{10})'(A_{10}+B_{10}))'$

$y_6=(y_5((A_9+B_9)'+(A_9.B_9)))'$

$y_7=(y_6+(A_8.B_8)'(A_8+B_8))'$

Above y[0] gives condition1 which is one bit comparison, y[1] gives condition2 which is two bit comparison. y[2] gives condition3 which is three bit comparison. y[3] gives condition4 which is four bit comparison.y[4] gives condition5 which is five bit comparison.y[5] gives condition6 which is six bit comparison. y[6] gives condition7 which is seven bit comparison. y[7] gives condition8 which is eight bit comparison.

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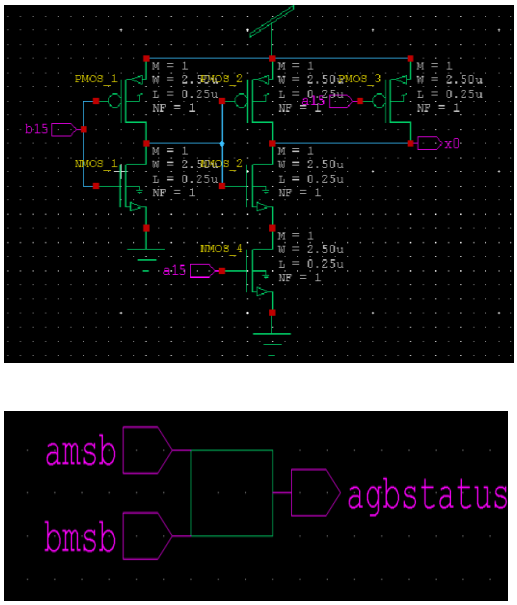

Fig. 1 Schematic and Symbol of AGTB Condition1

Fig 1 shows circuit for knowing the MSB status for A>B and output is designed for 0 when condition is satisfied and it 6 transistors in which internally we has one not gate and one 2 input nand gate and maximum 2 number of transistors are in series of pull-down which can enhance speed.

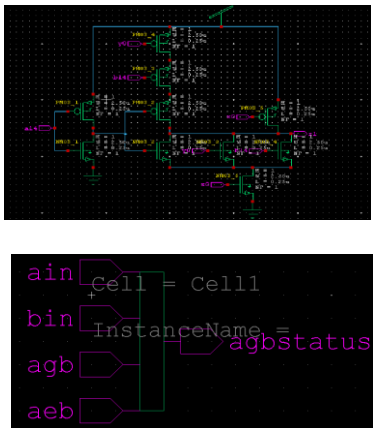

Fig. 2 Schematic and Symbol of AGTB Condition (2,4,6,8 …)

Fig 2 shows circuit for knowing the greater then conditions for all the even bit positions and output is designed for 1 when condition is satisfied and it has 10 transistors in which internally we has one not gate and one OAI13(OR-AND-INVERT) and maximum 3 number of transistors are in series of pull-up and the maximum 4 number of

transistors are allowed such that enough strength will be there for signal.

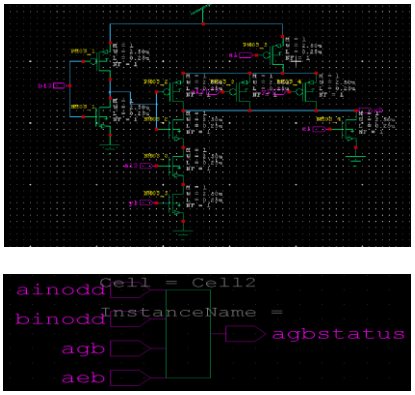

Fig. 3 Schematic and Symbol of AGTB Condition

(3,5,7…)

Fig 3 shows circuit for knowing the greater then conditions for all the odd bit positions and output is designed for 0 when condition is satisfied and it has 10 transistors in which internally we has one not gate and one AOI13(AND-OR-INVERT) and maximum 3 number of transistors are in series of pull-down that enough strength will be there for signal.

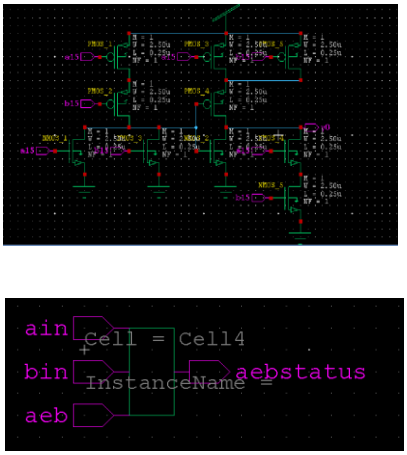

Fig. 4 Schematic and Symbol of AETB Condition1

Fig 4 shows circuit for knowing the Equality condition for the MSB and output is designed for 0 when condition is satisfied and it has 10 transistors in which internally we has one nor2 gate and one AOI12 and maximum 2 number of transistors are in series of pull-down and pull-up and it has two demarcation lines.

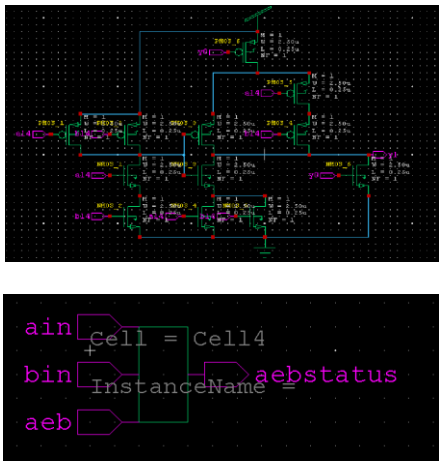

Fig. 5 Schematic and Symbol of AETB Condition (2,4,6,8 …)

Fig 5 shows circuit for knowing the Equality condition for all the even bit positions and output is designed for 1 when condition is satisfied and it has 12 transistors in which internally it has one nand2 gate and 8 Transistors circuit and maximum 3 number of transistors are in series of pull-up.

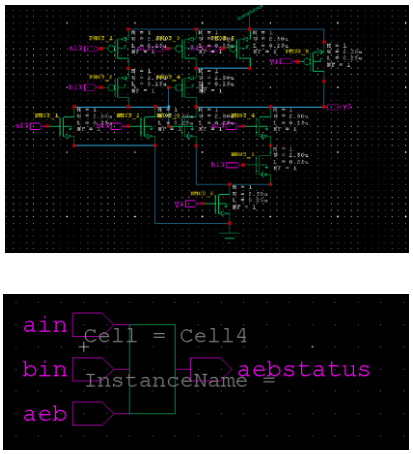

Fig. 6 Schematic and Symbol of AETB Condition (3,5,7 …)

Fig 6 shows circuit for knowing the Equality condition for all the odd bit positions and output is designed for 0 when condition is satisfied and it has 12 transistors in which internally it has one nor2 gate and different 8 Transistors circuit. and maximum 3 number of transistors are in series of pull-down.

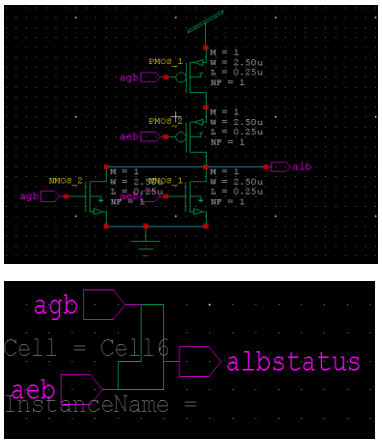

Fig. 7 Schematic and Symbol of AETB Condition (3,5,7 …)

Fig 7 shows circuit for knowing the less then condition once AGTB and ALTB are known then NOR gate will achieve the functionality of the ALTB. 4 number of transistors are required.

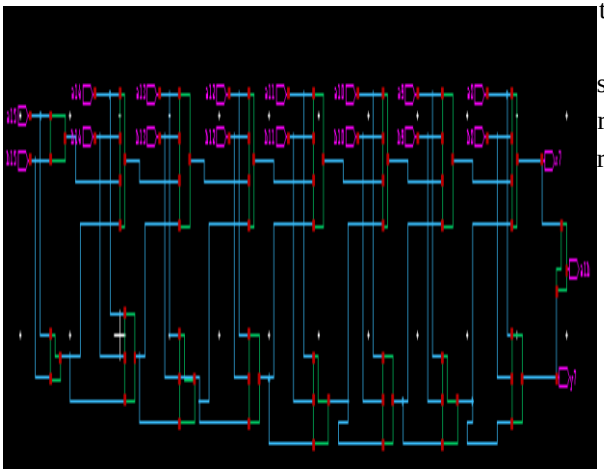

Fig. 8 Schematic of 170 transistor Comparator cell.

Fig 8 has 2 rows and in each row we have 8 columns and here row1-column1 corresponds to fig1 and row1-column(2,4,6,8) corresponds to fig2 and row1-column(3,5,7) corresponds to fig3. Row2-column1 corresponds to fig4 and row2-column(2,4,6,8) corresponds to fig5 and row2-column(3,5,7) corresponds to fig6.
There are 6 blocks used in our design one for knowing the MSB status of A and B, second for knowing the MSB-(2,4,6,8), third for knowing the MSB-(3,5,7), fourth for knowing the equality status of MSB, fifth for knowing the MSB-(2,4,6,8), sixth for knowing the MSB-(3,5,7).compares two Bit result coming from the previous stage and selection line will also come from earlier stage and selection will be like if s=1 top line will be selected , so for an 8-bit comparator there will be 7 Comparison cells , 11 two-to-one multiplexers, 1 inverter and 1 two-input nand

III. STATIC CMOS

Designing in full-custom has freedom for the designer unlike semi-custom design in which HDL description will be converted into the logic circuit. so, half of the work done by HDL coder and remaining by the logic synthesis tool. So we can never expect optimization with respect to the design constraints of VLSI.

Full-custom design is one in which we need to design circuit with maximum optimization and STATIC CMOS has the advantage of having very less idle state power dissipation Layout designers can find our design to be attractive as we need only 6 cells for N-BIT design and coming to the routing phase just there was requirement from bit to bit interconnections.

IV. PERFORMANCE ANALYSIS

8-bit magnitude comparator has been designed by using STATIC CMOS logic style. Table shows AREA comparision of Hensley, Saleh Abdel Hafeez, perri and the proposed COMPARATOR. The comparator which we designed using STATIC CMOS logic style has fewer transistor count.

TABLE I
COMPARISON OF TRANSISTOR COUNT WITH SIMILAR LOGIC STYLES

Comparator type	Technology / power supply	Transistor count
Proposed (Static type)	0.18 μm/1.8 V	526 (24-b) 1406 (64-b)
Abdelhafeez *et al.* [5] (Static type)	0.15 μm/1.5 V	2976 (64-b)
Hensley *et al.* [13] (static type)	0.18 μm/1.8 V	624 (24-b)
Perri *et al.* [6] (static type)	0.35 μm/3.3 V	1960 (64-b)

V.CONCLUSION

Transistor count is one of the important design consideration and since we have used Static CMOS which

has equal amount of hardware in the top and bottom of the demarcation line and physical interpretation of the circuit designers can have efficient floor planning. Since dynamic power consumption is the major contributor of the total power consumption and it depends upon the switching activity and by reducing the transistor count we have ensured that power can be somewhat minimized. Since our design is based on Static CMOS and at any given time half of the devices will be on. Static logic needs by default more number of transistors.

Total 98 number of transistors are reduced when in compared with design mentioned in [11] and 1570 number of transistors are minimized when related to [10] as well as 554 transistors are optimized with that of[12].

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