Review on Power Dissipation Analysis of Conventional SRAM Cell Architecture

S.Munaf[1], M.E., L. Malathi[2], M.E., Dr.A.Bharahi[3], Dr. A.N.Jayanthi[4]

Abstract— **Memories are the crucial part of any digital system and no digital system can be completed without memories. Compact devices and embedded systems are emerging, so the low power consumption is very essential to the architectural system design .Optimization of the power at the logical level is one of the most important task to minimize the power. With increasing technology, usage of SRAM Cells has been increased in large extent while designing the system on-chips in CMOS technology, this review article is also based on that. In this article focuses on the analysis in terms special types of SRAM are designed in order to satisfy low power, high performance, delay and area**.

Index Terms—**SRAM, Low Power, Delay, Area**

I. INTRODUCTION

SRAM chips are made up of flip-flop circuit which does not need constant refreshing. Static random access memory consumes very fast access speed, much faster than DRAM. The name is derived from the fact that memory locations are accessed in random order at a fixed rate, independent of physical location, for reading or writing. The six transistors control the speed of the current flow in one direction or vice versa. The chip does not require a capacitor to fill up or drain because each state can be written and read instantly. Static RAM is used for high-speed registers, caches and small memory banks like a frame buffer on a display adapter. SRAM is used in scientific and industrial subsystems, Modern appliances, automobile electronics, electronic toys, mobile phones, synthesizers and digital cameras. It is also used in PCs, peripheral devices, printers, LCD screens, hard disk buffers, router buffers and buffers in CDROM or CDRW drives. Arrangement of horizontal rows and vertical columns is used for storage purpose. The horizontal lines, which are driven only from outside the storage array are called word lines, and the vertical lines, there data flow into and out of cell share called bit lines. A cell can be accessed for reading or writing by selecting its row and column. Each Cell can store 0 or 1. From the last more than five decades the size of the CMOS devices is being scaled down to accommodate maximum memory on Soc. More memory means more information can be stored, that makes the system faster. Several bit cell design was proposed to improve the bit cell area, density, lower supply voltage and power consumption. From the design a 6T SRAM cell both the bit lines are driven for both read and write process. Consequently recharging for faster read access time and driving of these bit lines increases the power consumption of SRAM cells further. The low power operation of system can be achieved by lowering the leakage current which can reduce the leakage power consumption. We mainly focus on short circuit power dissipation, delay and area. We analyze several models of static random access memory cells by calculating their power dissipation, delay, area and conclude the best among the existing models.

II. LITERATURE SURVEY

Mo Maggie Zhang [1] suggested that the performance comparison of 6, 7 and 8T SRAM cell topologies is shown in the figure1, 2, and 3. As process technologies continue to advance, the speed of SRAMs will increase, but devices will be more susceptible to mismatches, which worsen the static-noise margin (SNM) of SRAM cells. Due to stability concerns, the dual port designs that implement read disturb-free feature such as that seen in the 7T and 8T cell implementation might become more practical in the future SRAM cell implementation. Even though 7T and 8T cell implementation result in a reported 13% and 30% area increase, respectively, these two topologies allow for better cell stability due to their read-disturb-free operation, which is beneficial as process technologies continue to scale down.

Manuscript received Nov, 2017.

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Proposed : SRAM cell Schematic[1]

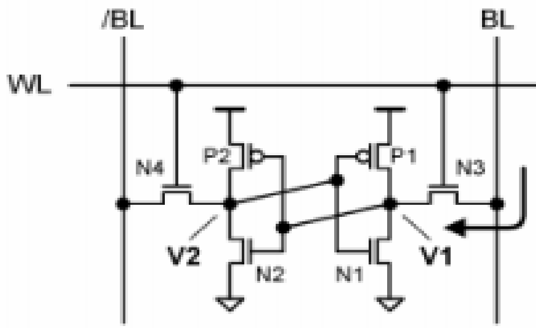

Figure 1. 6T-SRAM Cell

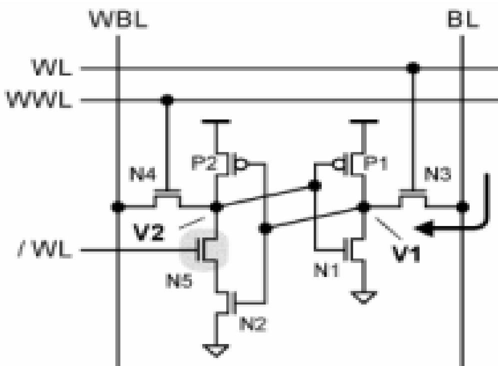

Figure 2. 7T-SRAM Cell

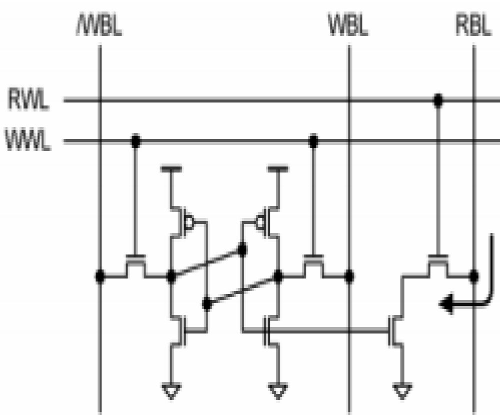

Figure 3. 8T-SRAM Cell

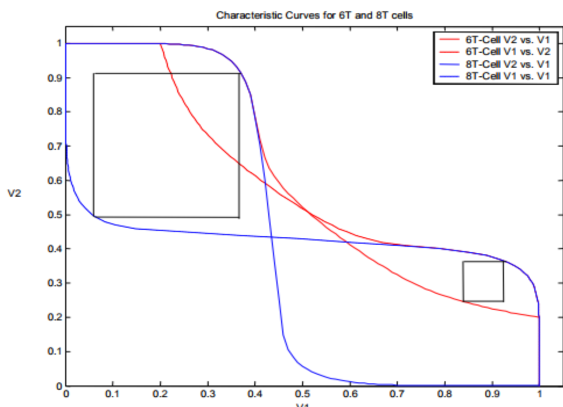

Figure 4. Characteristic Curves for 6T and 8T Cells

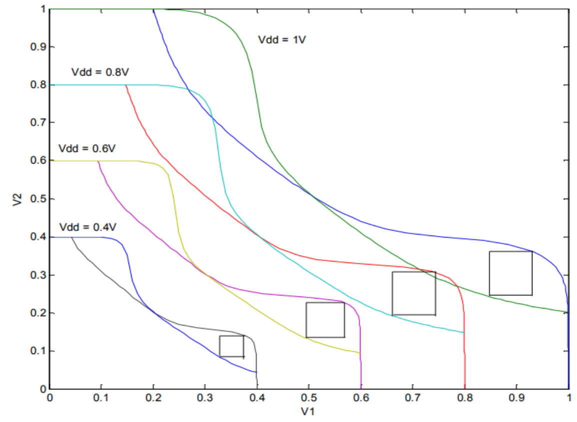

Figure 5. SNMs for 6T and 8T Cell Designs

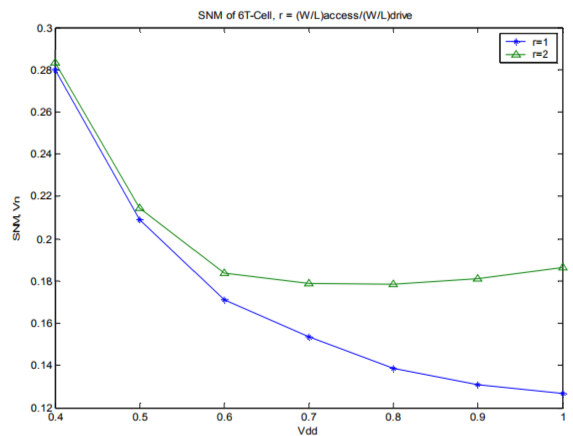

Figure 6. SNM vs. VDD for 6T Cell Design

Nakkala Suresh and Dr.Vangala Padmaja [2] proposed a robust Schmitt trigger based SRAM suitable for low voltage applications is shown in the figure 7 and 8. This feedback mechanism can be effective for nanoscaled technologies in process tolerant, low voltage SRAM operation. Research Simulation results are analyzed in Mentor Graphics EDA Tools with TSMC-250nm, TSMC-350nm technology.

Proposed: Bit cell schematic [2]

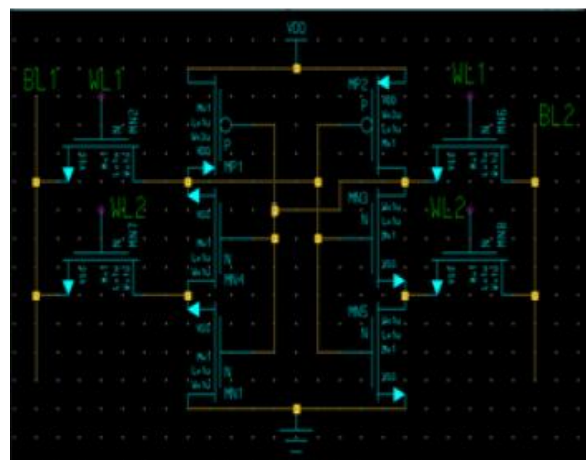

Figure 7. ST-1SRAM Bit Cell

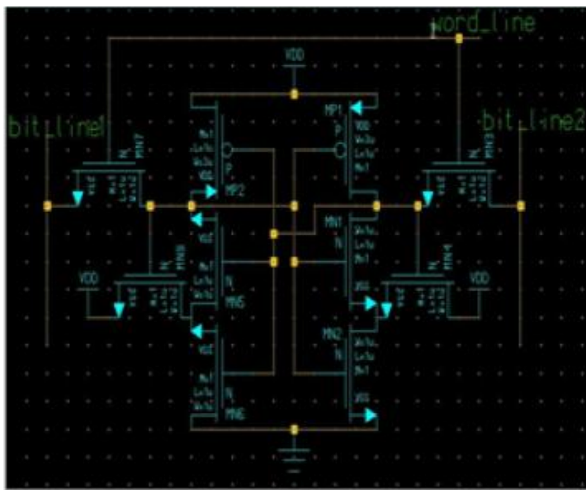

Figure 8. ST-2SRAM Bit cell

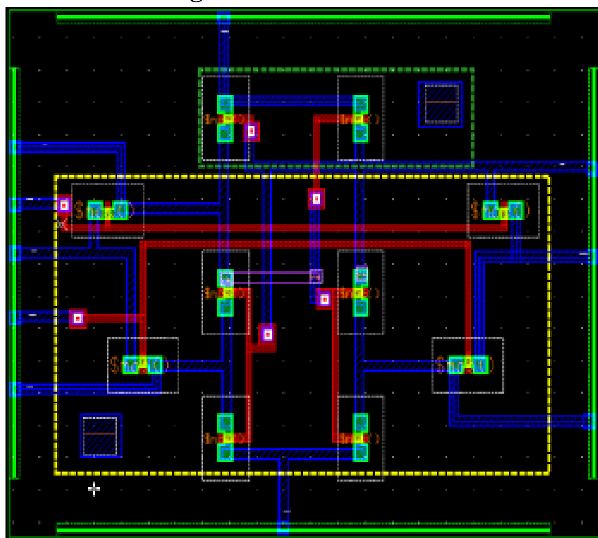

Figure 9. ST-2SRAM Bit Cell Layout

Table.1: Comparison Analysis of Bit Area /Vmin/power

S. N O	BITCELL TOPOLOGY	Vmin (V)	AREA (um)	Total Power Dissipation (W)
1	6T SRAM	1.5	116X170	541.62P
2	8T SRAM	2	110X192	1.26N
3	10T SRAM	3.3	195X260	1.89N
4	ST-1 SRAM	0.9	180X215	1.71N
5	ST-2 SRAM	0.8	162X217	0.98N

Vinesh Srinivasan ,Varshad Venkatraman.R, Senthil kumar.K.K[3] suggested the excessive power consumed during the operation of the conventional 6T SRAM cells causes limitations of read and write access of the cell thereby creating conflicts which results. The Schmitt trigger based cell design offers a solution to this issue by providing a built in feedback mechanism to modulate the switching threshold of the inverter depending on input transition. The ST SRAM cell has a built in feedback mechanism to tackle the PVT variations, along with CNFET is shown in the figure10 which provides exceptional electrical Characteristics at nanometer range, proves to be the ideal combination for future generation SRAM cells. During transition at the input node the feedback transistor preserves the 1 at the output node by raising the source voltage of NCNFET transistor N1. This gives sharper switching of the inverter. During input transition time the feedback mechanism is not present mean which gives smoother transfer characteristics for write operation. As a result transfer characteristics that vary with respect to the input of the cell and improve the read and write stability of the SRAM bit cell.

Proposed: Bit cell schematic [3]

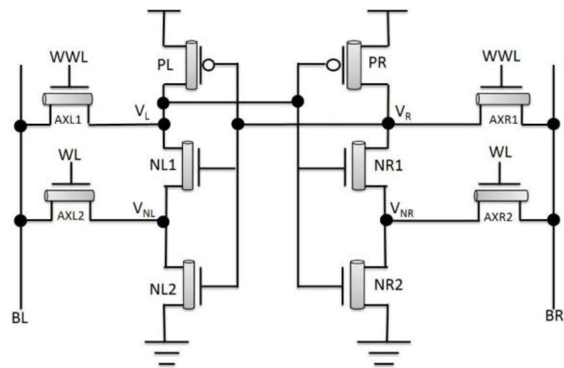

Figure 10. CNFET based Schmitt trigger SRAM cell

Table.2: Power Analysis

S.N O	Parameter Conventional CMOS	6T SRAM cell	Schmitt Trigger based SRAM using CMOS cell	Schmitt Trigger based SRAM Cell using CNFET
1	Average power	1.3726mW	0.2151 Mw	4.8916µ W
2	Dynamic power	2.3mW	2.3mW	42.4µW

Mahendra Kumar and Kailash Chandra [4] suggested that Data retention and leakage current are among the major area of concern in today's CMOS technology. In order to obtain higher noise margin along with better of the performance new SRAM cells have been introduced. In most of the cases cell read and write operation are secluded to obtain higher noise margin. In large memory capacity RAM chips, active power reduction is vital to realizing low-cost, high-reliability chips because it allows plastic temperature. Hence, various low power circuit technologies concerning reductions in charging capacitance, operating voltage, and static current have been developed. As a result, active power has been reduced at every generation despite a fixed supply voltage, increased chip size, and improved access. The trend of SRAM technology is moving towards high-density, high-speed and low-power. Higher density and higher speed are achieved by scaling. Reduction of the gate oxide leakage current is essential to achieve high-speed keeping low standby current. Low power consumption is achieved by reduction of the power supply and invention of the circuit

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design. New technology, such as Cu interconnects and low ‘K’ dielectrics are introduced for high-speed operation.

Simran Kaur and Ashwani Kumar [5] suggested the power dissipation during the Write operation in six-T CMOS SRAM as well as read operation also. In his research work, SRAM cell is shown in the figure11, will include one more extra transistor that will control the overall capacitances during the write and read operation and will optimize the total capacitance will result out the decrease in the power dissipation. Here in this work, they are targeting the short circuit power dissipation as well as switching power dissipation which is also known as dynamic power. The circuit is characterized by using the 130nm technology which is having q supply voltage of 1.5volt and threshold voltage is 0.40volts. The results are compared with Conventional 6T SRAM cell which is also being characterized in this thesis with the same technology. This modified low power cell consumes lesser power, maximum it is saving 54% as compared to existing SRAM cell.

Proposed: Bit cell schematic [5]

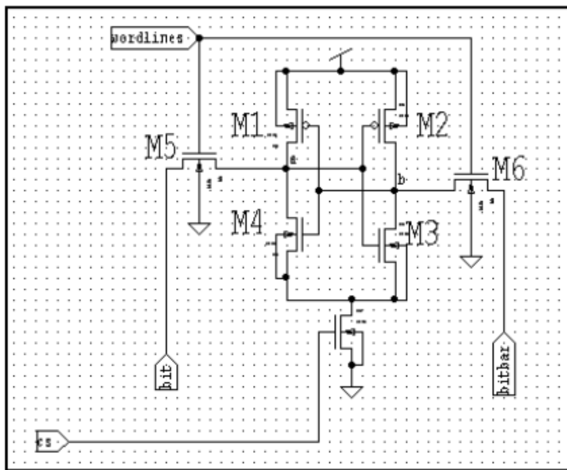

Figure 11. Low Power SRAM Cell

Table.3: Average Dynamic power

S. No	Power Dissipation	Average Dynamic power		% saving
		Conventional SRAM cell	Low power SRAM cell	
1	Write 0 power	7.78 µW	6.5 µW	16 %
2	Write 1 power	15 µW	6.8 µW	54 %

Table.4: Short Circuit Dissipation

S. No	Power Dissipation	Short-circuit power		% saving
		Conventional SRAM cell	Low power SRAM cell	
1	Write 0 power	52 µW	42 µW	19 %
2	Write 1 power	67 µW	42µW	37 %

Deepali Verma, Shyam Babu and Shyam Akashe [6] suggested to avoid noise immunity, leakage power, leakage current issues using FinFET based SRAM technology is shown in the figure12. It’s working process same as conventional based SRAM but the lower dissipation, leakage is less. The FinFET technology designs, works comparatively less power due to the absence of body biasing and it works on less power supply, but this power supply can be reduced up to certain value this value is data retention value.

Proposed: Bit cell schematic [6]

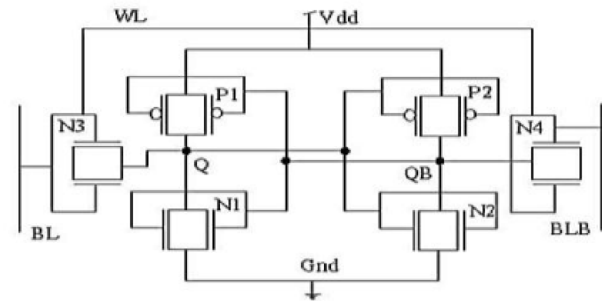

Figure 12. FinFET based 6T SRAM Cell

Table.5: Parameter Analysis

Parameters	Conventional 6T SRAM		FinFET Based 6T SRAM	
	Write	**Read**	**Write**	**Read**
Technology	45 nm	45 nm	45 nm	45 nm
Supply	700 mV	700 mV	700 mV	700 mV
Leakage current	69.22 pA	54.88pA	69pA	53.90 pA
Leakage power	7.346 nW	1.710×10 -6 W	7.561 nW	1.709 ×10-6 W
Delay	20.57 ns	21.70 ns	20.55 ns	21.44 ns

III. CONCLUSION

In this paper Combination of different techniques of SRAM is discussed. This review motivates a lot of scope for improving the performance and power reduction of SRAM circuits. By combing all the specialized techniques which is proposed in the previous research, the optimized low power SRAM can be designed. The combined low power SRAM design will be having reduced power which can be used in high speed applications.

ACKNOWLEDGMENT

The authors would like to thank the authorities of Sri Ramakrishna Institute of Technology – Coimbatore for providing research support grants and environments for carrying out the research works.

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