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FPGA Realization of FIR Digital Filter

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Abstract— In signal processing, a digital filter is a system that performs mathematical operations on a sampled, discrete time signal to reduce or enhance certain aspects of that signal. A digital filter takes a digital input, gives a digital output, and it consists of digital components. To implement compact FIR Filter, the algorithm should have less multipliers or multiplier less design is used.so the design only consist of adder, sub tractor and shifter. In this paper, we study FPGA implementation of digital filter and Complexity of FIR Filter hardware is reduce by the Multiple Constant Multiplication (MCM) Algorithm.MCM consist of fixed point constant that multiplies with fixed point of variable. MCM reduces no. of additions for multiplication. MCM gives optimized solution when block formulation of FIR filter is implemented. MCM scheme for FIR Filter effectively reduced area, power and complexity of solution by using horizontal and vertical common sub expression elimination technique.
The FPGA implementation of proposed structure gives less area delay product than existing structure for fixed and reconfigurable application.

Keywords- Block processing, finite-impulse response (FIR) Filter, reconfigurable architecture, VLSI, Multiple Constant Multiplication (MCM)

I. INTRODUCTION

Digital Filters widely used in the signal processing application like speech processing, noise cancellation, channel equalizer, various communication as well as industrial application. VLSI system with low power, high performance and area efficient design widely used in the digital application. Digital filter performs signal processing function of given input. It attenuates the unwanted frequency component and passes only require components to the further processing block. Electronics filters are digital and analog. Digital filter performs filtering operation on the digital signal. FIR and IIR are digital filters.
FIR Filter have finite duration Impulse Response as well as it have many advantages like they are stable, flexible and less sensitive to Finite Word Length Effect. But it require more computational power than IIR.
During last decades no. of FIR Filter design schemes are implemented on FPGA as well as ASIC platforms. ASIC based implementation have many limitations like the design become expensive ,design cannot easily reprogrammed also reused for other application not easily possible. Depending upon the application the multiplication and addition are increase to get filter output.
FPGA Based implementations of design provide better solution for real time application. Also the complex designs can be easily implemented on the FPGA. Thus due to efficient platform FPGA Designs are popular now days. For real time

application where coefficient vary with time the design of FIR filter become more complex. To reduce the complexity design many algorithms are design for filter like Canonic Sign Digit, Distributed Arithmetic, Multiple Constant Multiplication. In MCM algorithm fixed point constant are multiplies with the fixed point variables. MCM reduces the complexity of multiplication so it widely used for Filter implementation.

II. RELATED WORK

K.-H. Chen and T.-D. Chiueh, 2006[8] this paper present a finite-impulse response (FIR) filter architecture for digit reconfigurable with fine granularity. It provides a low power solution, flexible and compact FIR filters with a wide range of precision. The proposed architecture of an 8-digit reconfigurable FIR filter chip is implemented in 0.35-mum CMOS technology. [2]

A. P. Vinod and E. M. Lai, 2006 [6] this paper shows a FIR Filter implementation method for SDR receivers. The result shows that it require minimum number of adders.

Pramod Kumar Meher, Shrutisagar Chandrasekaran, 2008 [9] This paper gives area delay power efficient solution for FIR Filter for systolic decomposition of distributed arithmetic (DA)-based inner-product computation. DA-based computation reduces memory size but it leads to increase latency and adder complexity.

Ruan, A.W., Liao, Y.B., Li,P. , Li,J.X., (2009) this paper presented An ALU based universal FIR filter. FIR filters can be implemented by programming instructions in the ROM with same hardware architecture. They presented Arithmetic Logic Unit (ALU) based universal FIR filter used for implementation in Field Programmable Gate Arrays (FPGA). In the proposed ALU architecture implements FIR functions by using accumulators and shift-registers controlled by the instructions of ROM. Conventional FIR implemented by the Multiplier and accumulator based architecture

Nekoei, F., Kavian, Y.S., Strobel, O (2010) [12] This paper presented realization of digital FIR filters on field programmable gate array devices. Direct and transposed architectures were employed for implementing FIR filters on a Xilinx SPARTAN2 FPGA using Verilog hardware description language codes.

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X.Jiang, Y.Bao(2010) In this paper proposed a structure use MATLAB FDA Tool to determine filter coefficients. 16 order FIR Filter designed on FPGA and performance and results are analyzed.

Li,J., Zhao,M., Wang., (2011) [13] In this paper they used distributed algorithm(DA) to implementation 60-order FIR filter based on FPGA . Distributed algorithm (DA) converts multiplication to look-up table structure, and then it implement multiplication operation. They used FPGA as hardware. This proposed system gives good performance, the filter speed is higher and the resource require is fewer.

R. Mahesh and A. P. Vinod (2010) [6] For multi standard wireless communication system this paper proposed system provide Re-configurability and low complexity to finite impulse response (FIR).In this paper low complexity FIR filters is proposed, which provide re-configurability. The proposed FIR filter architecture uses constant shifts method and programmable shifts method.

S. Jayashri and P. Saranya (2014) [10] In Analog and Digital areas the hardware implementation of FIR Filter has important applications. In digital signal processing FIR filters are used in separation of signals and in signal restoration purpose. The existing method of Filter is designed using multiplier technique which gives increases the area, delay, power and so using binary input, they designed Filter using multiplier less technique.

Pramod Kumar Meher (2010) [11] In this paper Distributed arithmetic (DA)-based computation was explain for implementation of FIR Filter. Distributed arithmetic (DA)-based computation gives efficient memory-based implementation of finite impulse response (FIR) filter where inner-product of input-sample vectors and filter-coefficient vector produces Filter Output.

III. SYSTEM ANALYSIS

A. Problem Definition

1. For high speed application Filter require high sampling rate.
2. Large order filter require more no. of addition and multiplication to calculate output.
3. When the coefficients are dynamically change then the design become more complex.
4. For reconfigurable application the design should not provide the area-delay efficient structure.
5. Earlier design algorithm provide efficient solution for lower order filter.

B. Proposed System Feature

1. Proposed system provide advantage of FPGA implementation of design like reconfigurable, less complexity & require less power.
2. Also the realization of block FIR filter using MCM scheme gives less area delay product for large order.
3. Proposed system used for both fixed & reconfigurable application.
4. For Fixed Application MCM Scheme provide less multiplication and addition for complex design.

IV. SYSTEM DESIGN AND IMPLEMENTATION

A. Proposed structure for block FIR filter

Output of FIR filter can be calculated as product of impulse response vector and an input vector.

$$y(n) = \sum_{i=0}^{N-1} h(i) \cdot x(n-i). \quad (1)$$

Where N =Length of Filter
h(n)= impulse response vector
x(n)= input vector.

The proposed structure for reconfigurable application consists of one coefficient selection unit (CSU), one register unit (RU), *M* number of inner product units (IPUs), and one pipeline adder unit (PAU).For the reconfigurable application CSU stores coefficients of all the filters. CSU consist of *N* ROM LUTs, *N* is the filter length. CSU at one clock cycle select filter coefficient at particular channel.RU receives the input signal X(n) and produces L rows in parallel. IPU performs the inner matrix vector product and gives Y(n).

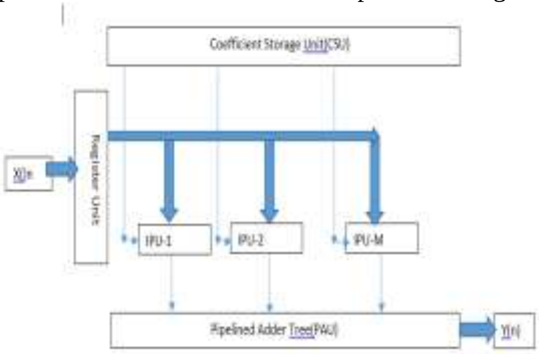

Figure 1: Proposed structure for block FIR filter for Reconfigurable Application

For Fixed Application CSU and IPUs are not required because the coefficients are fixed. Only MCM blocks are required for multiplication. For Fixed Application

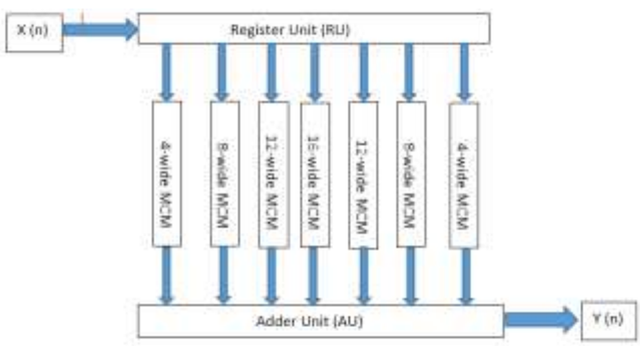

Figure 2: Proposed structure for block FIR filter for Fixed Application

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For block Filter implementation of MCM Scheme formulation input matrix uses the Common Sub expression Elimination technique. So the input matrix only contain six input samples[x(4k), x(4k-1), x(4k-2), x(4k-3), x(4k-4), x(4k-5), x(4k-6)] and it multiplies with fixed no. of coefficients.

Input Sample	Coefficient Group
x(4k)	{h(0),h(4),h(8),h(12)}
x(4k-1)	{h(0),h(4),h(8),h(12)} {h(1),h(5),h(9),h(13)} {h(),h(),h(),h(),}
x(4k-2)	{h(0),h(4),h(8),h(12)} {h(1),h(5),h(9),h(13)} {h(2),h(6),h(10),h(14)}
x(4k-3)	{h(0),h(4),h(8),h(12)} {h(1),h(5),h(9),h(13)} {h(2),h(6),h(10),h(14)} {h(3),h(7),h(11),h(15)}
x(4k-4)	{h(1),h(5),h(9),h(13)} {h(2),h(6),h(10),h(14)} {h(3),h(7),h(11),h(15)}
x(4k-5)	{h(2),h(6),h(10),h(14)} {h(3),h(7),h(11),h(15)}
x(4k-6)	{h(3),h(7),h(11),h(15)}

TABLE.1.MCM for block FIR Filter

B. Implementation Setup

XILINX ISE web pack 14.1used for design, synthesis and implementation. Verilog are used to describe the behavior and structure of system and circuit designs. The proposed structure simulated on the Xilinx System Generator.

V.RESULTS

A. Performance Comparison

The performance comparison table shows that proposed structure requires less number of multipliers and adders than existing algorithm.

Resources	**Proposed structure**	**Mohanty structure**
Length	16	16
Flip-Flop	834	312
Multiplier	46	64
Adder	49	60

TABLE. 2. Performance Comparison

B. Synthesis And Simulation Result:

Synthesis report shows the no of flip-flops,counters, LUTs for implementation of block FIR Filter using MCM. It also gives information about device utilization. Simulation result gives output of Filter.

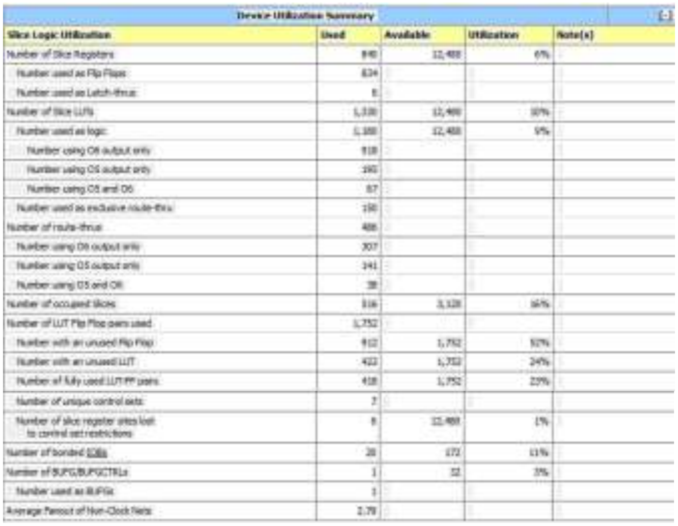

Figure 1: Proposed structure Simulation Report

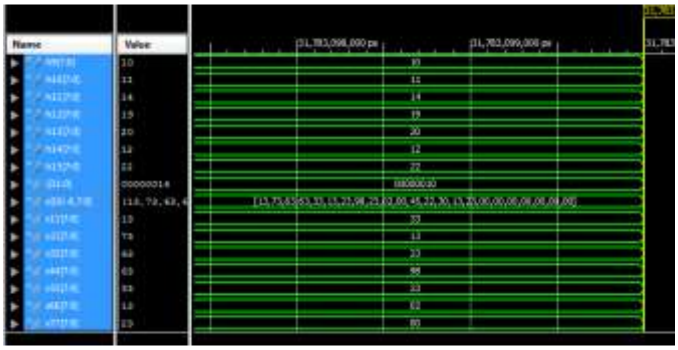

Figure 2: Proposed structure output for block FIR filter

VI. CONCLUSION

In this paper, proposed structure provide area delay efficient realization for Fixed and Reconfigurable Application. The design of block FIR Filter using MCM Scheme reduces the computational complexity of structure by reducing no. of addition and multiplication.

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REFERENCES

1] J. G. Proakis and D. G. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications. Upper Saddle River, NJ, USA: Prentice-Hall, 1996.

2] T. Hentschel and G. Fettweis, Software radio receivers, in CDMA Techniques for Third Generation Mobile Systems. Dordrecht, The Netherlands: Kluwer, 1999, pp. 257283.
3] E. Mirchandani, R. L. Zinser, Jr., and J. B. Evans, A new adaptive noise cancellation scheme in the presence of crosstalk [speech signals], IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 39, no. 10, pp. 681694, Oct. 1995.
4] D. Xu and J. Chiu, Design of a high-order FIR digital filtering and variable gain ranging seismic data acquisition system, in Proc. IEEE Southeastcon, Apr. 1993, p. 16.
5] J. Mitola, Software Radio Architecture: Object-Oriented Approaches to Wireless Systems Engineering. New York, NY, USA: Wiley, 2000.
6] A. P. Vinod and E. M. Lai, Low power and high-speed implementation of FIR filters for software defined radio receivers, IEEE Trans. Wireless Commun., vol. 7, no. 5, pp. 16691675, Jul. 2006.
7] J. Park,W. Jeong, H. Mahmoodi-Meimand, Y.Wang, H. Choo, and K. Roy, Computation sharing programmable FIR filter for low-power and high-performance applications, IEEE J. Solid State Circuits, vol. 39, no. 2, pp. 348357, Feb. 2004.
8] K.-H. Chen and T.-D. Chiueh, A low-power digit-based reconfigurable FIR filter, IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 8, pp. 617621, Aug. 2006.
9] S. Y. Park and P. K. Meher, Efficient FPGA and ASIC realizations of a DA-based reconfigurable FIR digital filter, IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 7, pp. 511515, Jul. 2014.
10] P. K. Meher, Hardware-efficient systolization of DA-based calculation of finite digital convolution, IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 8, pp. 707711, Aug. 2006.
11] P. K. Meher, S. Chandrasekaran, and A. Amira, FPGA realization of FIR filters by efficient and flexible systolization using distributed arithmetic, IEEE Trans. Signal Process., vol. 56, no. 7, pp. 30093017, Jul. 2008.
12] Nekoei,F., Kavian,Y.S., Strobel,O., “Some Schemes Of Realization Digital FIR Filter On FPGA For Communication Application” in proc. *20th International Crimean Conference on Microwave and Telecommunication Technology*, pp. 616 – 619, 2010.
13] Li,J., Zhao,M., Wang,X.,“Design and Simulation of 60-order Filter Based on FPGA”in proc. *International Conference on Intelligent Human-Machine Systems and Cybernetics (IHMSC), IEEE*, pp. 113 - 115, Oct 2011.

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