ISSN: 2278 – 1323
International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)
Volume 5, Issue 8, August 2016

A Survey Paper on Design of Voltage Level Shifter in SOC

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Abstract— ***Power dissipation of integrated circuits is the most challenging issue for very large scale integration (VLSI) design engineers, particularly for handy and portable applications. Use of multiple supply voltages systems, which employs level converter among two voltage islands, is one of the most efficient ways to reduce power consumption.***

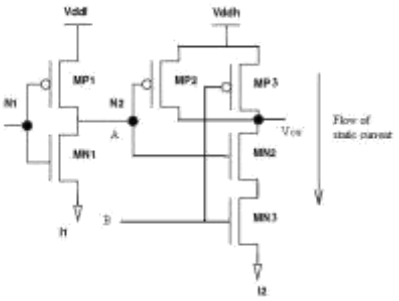
***Index Terms*—ULS,Power,ULC,DLC,CCLC.**

I. INTRODUCTION

Portable devices like cell phones, personal digital assistants (PDA), laptops, digital cameras and a variety of such other devices are highly popular among various users in the market. This requirement for portability has put forth number of restrictions on the size, weight, and battery life of such devices. Low power design is the key to meet the demands for such lightweight and longer battery life devices. Hence, power dissipation is one of the fundamental design concerns that current day very large scale intregration (VLSI) design engineers have to cope with while dealing with integrated circuit designs. Power minimization is not only essential for portable devices but also necessary for improving reliability of high-end microprocessors and data processing which include real time data processing and decoding of audio/video data . Significant research progress has been made during recent years to reduce the power dissipation of an integrated circuit.

1.2 Need for Level Converter

Multiple voltage supply systems are most efficient and commonly employed techniques for low power designs. The idea behind this technique is to use multiple supply voltages for a single chip by dividing the integrated circuit into regions, called *voltage islands*, operating at different voltages. The circuits which are on the critical path are supplied higher voltage level (V_{DDH}) and the circuits which are off the critical path are made to run at a lower voltage level (V_{DDL}) . A level converter is needed at the interface of a gate operating at V_{DDL} and a gate operating at V_{DDH}. The insertion of level converter between two voltage islands is essential to avoid the static current which might lead to undesirable power consumption . Thus a level converter can be defined as a simple circuit which converts the voltage at its input from one voltage level to another. A level converter can be fixed according to the requirement of level conversion in a circuit. Level converters which are inserted only at the interface of the cells operating at different voltage levels are synchronous level converter. The level converters which are inserted anywhere in the circuit wherever level conversion is required are known as asynchronous level converterS.



II. PREVIOUS WORK

Level converters are very important for multi-voltage supply systems. In the recent years, a lot of research has been going on which concentrate on the aspect of power reduction through multi-voltage system on chips (SoCs) and level converters. In this chapter, a review of the research work done in multi-voltage systems and level converters is presented. Section 2.1 shows various research work done for multi-voltage supply systems. Sections 2.2 and 2.3 discuss in

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brief various researches done in level up converters and level down converters

A. Multi level Voltage System

The ever growing need for low power design for various day to day, especially for mobile applications has motivated the very large scale integration (VLSI) design engineers to study and work on various techniques for power reduction. As discussed in chapter 1, the most commonly used and, importantly, efficient method for power dissipation reduction, is by using a multi-voltage supply system which make use of level converters. The key to design a multiple voltage system is to divide the integrated circuit into regions working at different voltage levels. For designing such systems algorithms like clustered voltage scaling (CVS) are widely used. CVS methods allows synchronous level conversion which means that after dividing the integrated circuit into different regions or cells working at different voltages, level converters are inserted only at the interface of two cells. Authors in [4] discuss in details about multi voltage supply systems and various algorithms followed for assignment of V_{DD} to cells.

B. Up level Converter

While designing a multiple supply voltage system, it is essential to consider the overhead caused by the level converters . To reduce this overhead, generally multiple voltage systems implement pipeline flip flops along with level converters at the end of low V_{DD} clusters [8]. The flip flops combined with level converters perform the operation of latching and level conversion at the same time. Such flip flops are called as a level converting flip flops. In [9], key properties and design metrics of a level converter for dual-V_{DD} systems are examined. The authors have studied the traditional level converter circuits like cross coupled level converter (CCLC), single supply diode voltage limited buffer level converter (SSLC), pass transistor half latch (PHL) and pre-charged circuit. Several new level converting flip flop circuits called LCFFs are also proposed and these new designs are compared to the above mentioned traditional level converting circuits in terms of level converter performance and *robustness as well as system level performance and robustness. The proposed level converting flip flops exhibit improved energy-delay product values, reduced system-level power and better immunity to supply noise without incurring significant layout are penalties. In [5],[6] and [10] the authors have studied a conventional level converter circuit known as dual cascode voltage switch (DCVS). The DCVS circuit is a small circuit which consists of a PMOS pair connected back to back which act as a differential pair. Each of the above referenced papers proposes new level converter designs considering DCVS as a baseline design. In [6], authors propose a new level converter circuit based on the keeper transistor concept in pass transistor logic Figures*

C. Down Level Converter

In [12], a distinct level down converting circuit is proposed. This circuit consists of a differential input pair circuit acting as the level converting circuit. This level converter provides stable operation for low voltage and high speed use [12]. The circuits make use of thin gate oxide MOSFETS which enable a faster level conversion. The differential input pair of this level converter offers a high immunity against power supply bouncing.Table 2.1 shows the different research works in level converters categorized on the basis of type of the level converter proposed, technology used for simulation, calculated power consumption values and the design approach followe

III. PROPOSED METHODOLOGY

Overall View of Universal Level Converter

Universal Level Shifter (ULS) can be simply define as a system which performs four different level converting operations on the input signal. These four operations contain (i) up conversion, (ii) down conversion, (iii) passing of signal and (iv) jamming of signal. Level up conversion can be stated as conversion of a low voltage signal (V_L) to a higher voltage level (V_H). While in distinguish, level down conversion can be defined as conversion of a higher voltage signal (V_H) into a low voltage (V_L). Passing of the signal indicate bypassing the signal to the former side of the network lacking doing any operation on the signal and jamming indicates completely stopping the input signal from existing at the former side. The universal level converter can be planned for all the above four mentioned functionalities depending on the type of necessity. The type of action to be performed can be selected using the two control signals.

Figure 4.1 shows a high level block diagram of the projected ULS.

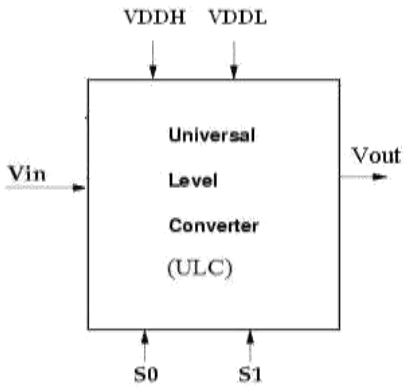

Fig. 4.1 High level view of proposed universal level converter (ULS)

As shown in the diagram, ULS has in all five input pins and one output pin. The input signal is supplied at pin *Vin* and output is taken across *Vout*. *s0* and *s1* are the pins for the control signals. The dual supply for ULS consists of V_{DDH} and V_{DDL}.

The level converter employs four break up circuits that match up to the above mentioned four discrete operations. Figure 4.2 shows the detailed view of the different blocks which constitute to the design of ULS. The *CCLC* block is used for level up conversion, while *DL* block is used for level down conversion. The passing and jamming functionality is get through the *pass circuit* and *block circuit*. The schematic details of these blocks are briefed curtly. The outputs since these four blocks are attached to the output of ULS through a multiplexer. The two control signals s0 and s1 are used to select the preferred operation of ULS.

IV. PROPOSED RESULT AND CONCLUSION

The simulation set up for 45nm technology is same as shown in Fig. 4.1. But to simulate MLC at this technology a BSIM4_45nm technology model file from PTM (predictive technology model) is used. For this schematic design, a W/L ratio of 4:1 is used, and the device parameters for PMOS are W= 360nm and L = 45nm and for NMOS are W= 180nm and L = 45nm. The values of threshold voltages (V_{TH}) for PMOS and NMOS are -0.22V and 0.22V, respectively. The typical values for the dual voltage supplies are used as V_{DDH} = 0.7V and V_{DDL} = 0.595 (85% V_{DDH}). The dual voltage supplies at pins V_{DDH} and V_{DDL} are connected to voltage sources. The value of load capacitance used is 15fF. The pin *Vin* represents the input pin where a piecewise voltage signal is applied as input. *s0* and *s1* are the control signal pins which decide the type of output of MLC. The circuit is simulated in the LTspice and a transient analysis for 100nsec is performed during simulation. The output of MLC is observed in its different modes of operation as discussed Table 2. The Fig. 5.1 shows the output of the universal level converter in all of its four modes of operation.

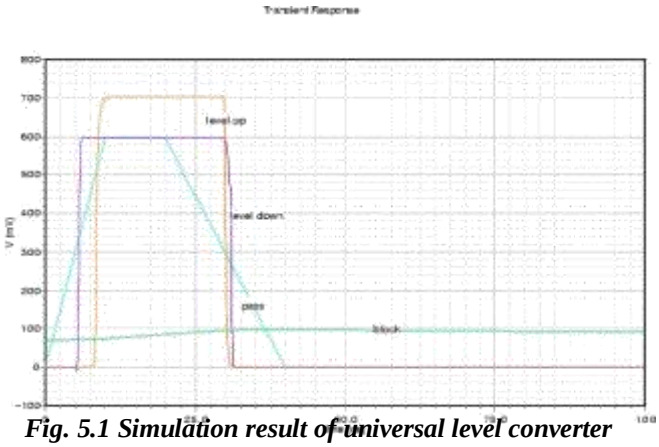

Fig. 5.1 Simulation result of universal level converter showing the outputs for all the four modes of operation.

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