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Performance Comparison of Carry Save Adder at 180nm, 90nm and 45nm CMOS Technology

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***Abstract*- In today's world designing low power and low voltage circuit is a promising field in VLSI Design. Addition is the most basic and often used arithmetic operation in microprocessor, digital signal processor. The Processor speed highly depends on the speed of the adder circuit. Carry Save Adder (CSA) is one of the fastest adders with penalty of area. The comparative analysis is done on the basis of performance parameters like leakage current, power dissipation and Time delay with 180nm, 90nm and 45nm CMOS technology.**

***Keywords*- Carry Save Adder, 17T Full Adder, CMOS-180nm, 90nm and 45nm Technology.**

I. INTRODUCTION

The carry-save adder reduces the addition of 3 numbers to the addition of 2 numbers. The propagation delay is 3 gates regardless of the number of bits. The carry-save unit consists of n full adders, each of which computes a single sum and carries bit based on the corresponding bits of the three input numbers. The entire sum can then be computed by shifting the carry sequence left by one place and appending a 0 to the MSB of the partial sum sequence and adding this sequence with RCA produces the resulting n+ 1-bit value. This process can be continued indefinitely, adding an input for each stage of full adders, without any intermediate carry propagation. These stages can be arranged in a binary tree structure, with cumulative delay logarithmic in the number of inputs to be added, and invariant of the number of bits per input. The main application of carry save algorithm is, well known for multiplier architecture is used for efficient CMOS implementation of much wider variety of algorithms for high speed digital signal processing. CSA applied in the partial product line of array multipliers will speed up the carry propagation in the array [2].

II. WORKING OF CARRY SAVE ADDER (CSA)

1) *BASIC WORKING OF CSA*

Carry Save Adder can be used to add multiple operands. In an example given bellow three operands are added. The sum & carry generated is similar to other Full Adders but the carry is added to the sum at the next level. At the last stage a ripple carry adder(RCA) is used to generate the sum & carry.

X:	1011
Y:	+0001
Z:	+1011
S:	0111
C:	1011
Sum:	11001

As shown in above example three operands X, Y and Z of four bits are added. The partial sum is calculated and the carry is given to next higher bit and added to

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the partial sum in the next stage. Final sum is available after two stages of successive additions.

2) CSA USING RIPPLE CARRY ADDER USING 17T 1-BIT FULL ADDER CELL

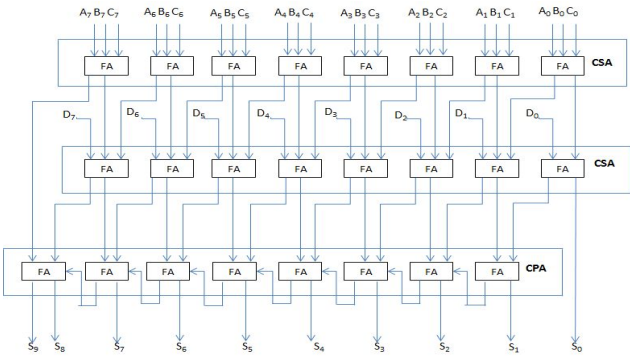

Fig.1: 8-Bit 4-Operand CSA using 17T FA Cell

Fig.1 shows schematic of conventional Carry Save Adder in which any 1-bit Full Adder Cell is used as a FA Cell.

III. RELATED WORK

Carry save adder is being used in multipliers, signal processing, FFT etc. The Carry Save Adder reduces the addition of 3 numbers to the addition of 2 numbers so that propagation delay is 3 gates regardless of the number of bits. Here in this paper 17T 1-bit FA Cell is taken as FA unit. The 17T FA has no short circuit power and lower dynamic power (compared to other adder cells), because of less number of transistor and magnitude of circuit capacitances. It consumes 10% to 15% less power than the other two (16T and 14T) cells[1]. A comparative analysis (using Magic and Hspice) for 8–bit ripple carry and carry select adders shows that the adders based on the new cell can save up to 25% of power consumption [1].

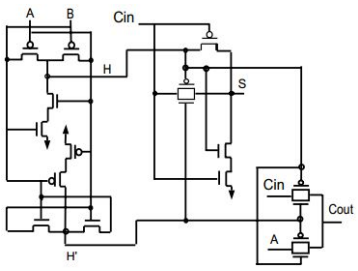

Fig.2: 17 Transistors Adder Cell [1]

IV. SIMULATION RESULTS

Simulation of proposed circuit is done in NGSPICE TOOL and graphs are obtained from ORIGINPRO Tool.

1) SIMULATION OF 17T FULL ADDER CELL

Simulation results of 17T Full Adder cell in 180nm and 90nm CMOS Technology is shown below.

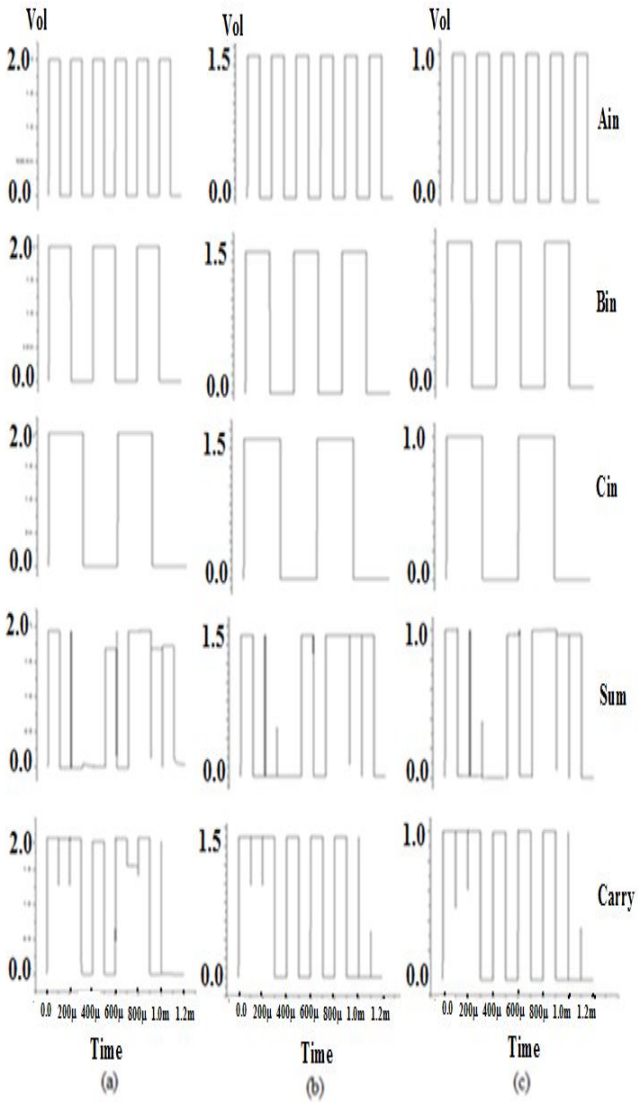

Fig.3: Inputs and Outputs of 17T FA in (a) 180nm, (b) 90nm and (c) 45nm CMOS Technology

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2) SIMULATION OF 8-BIT 4-OPERAND CSA

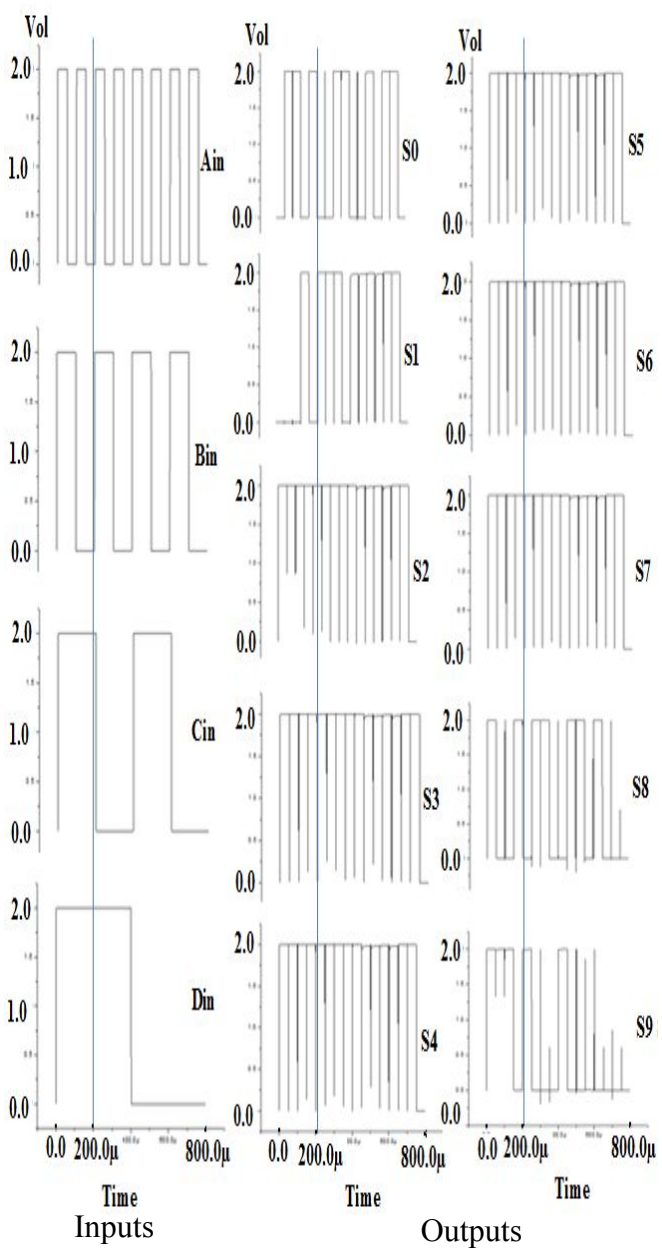

Fig.4: Inputs and Outputs of CSA in 180nm CMOS Technology

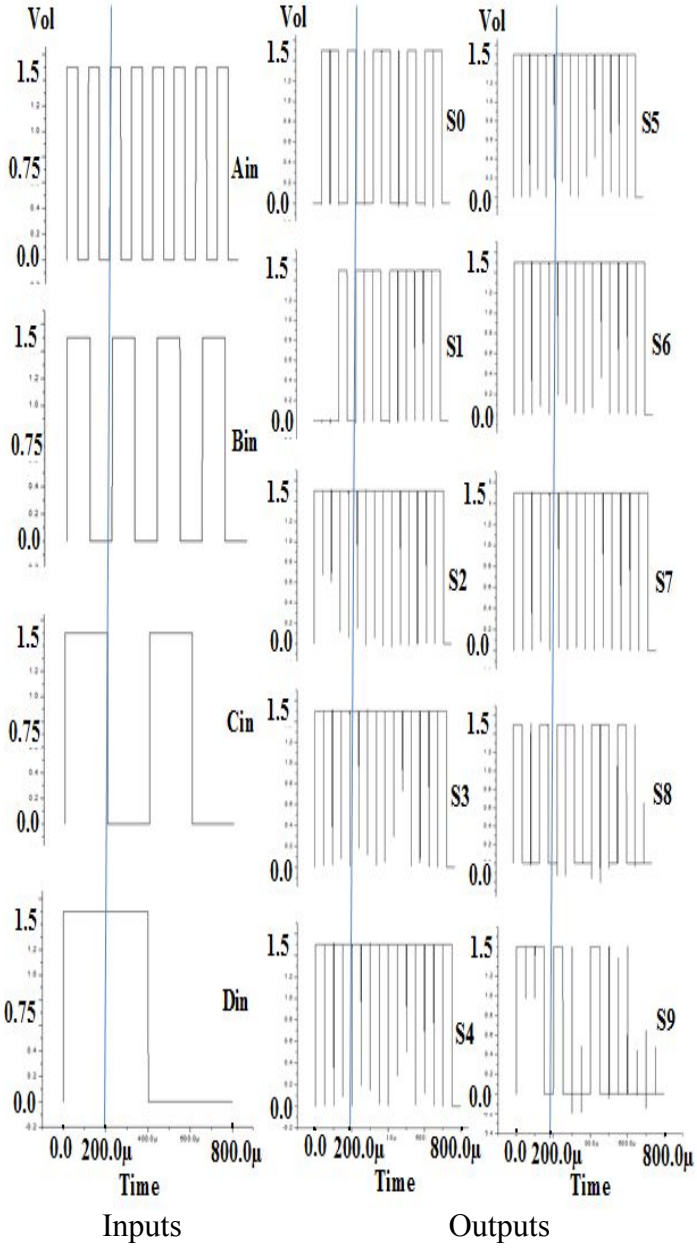

Fig.5: Inputs and Outputs of CSA in 90nm CMOS Technology

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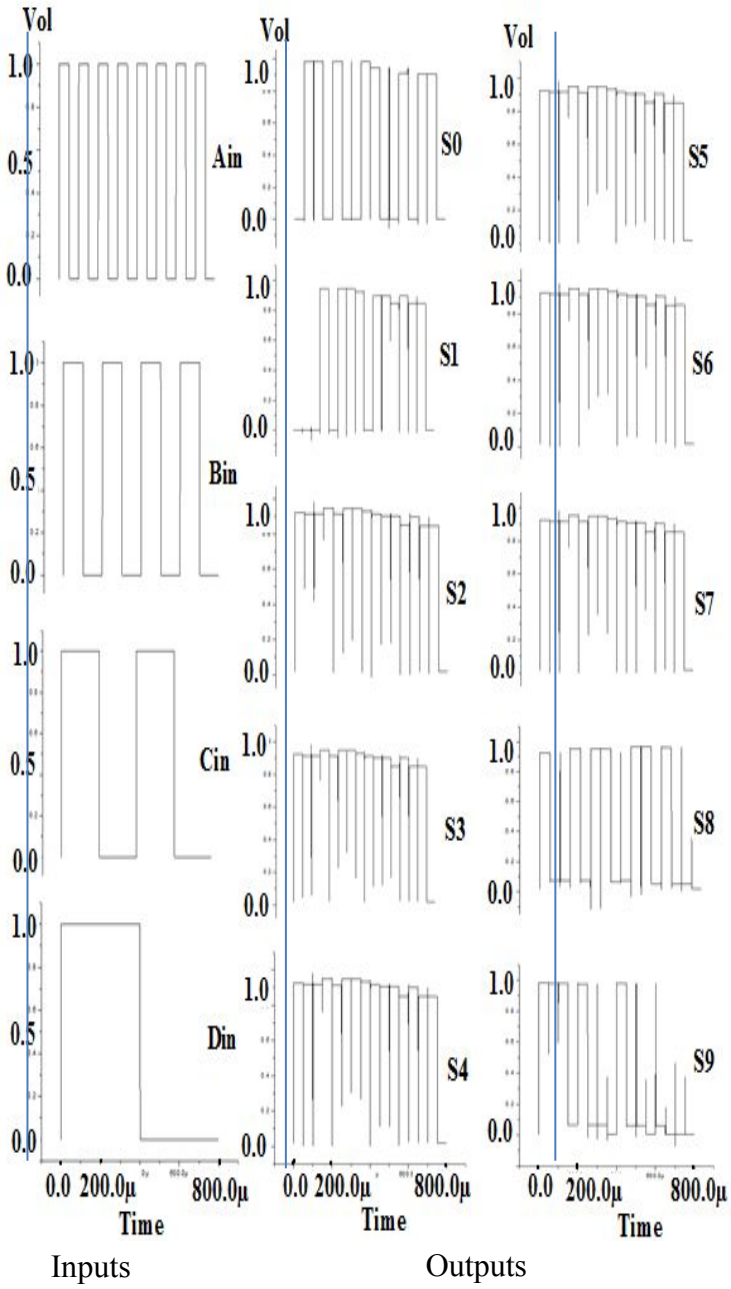

Fig.6: Inputs and Outputs of CSA in 45nm CMOS Technology

V. COMPARISON TABLES

Table I: 17T FA cell in 180nm and 90nm CMOS Technology

Techno-logy	Leakage Current	Power Dissipation	Delay
180nm	7.73E-20 A	15.46E-20 W	0.91187 µs
90nm	1.85E-25 A	2.775E-25 W	0.42248 µs
45nm	3.92E-25 A	3.92E-25 W	0.28048 µs

Table II: CSA in 180nm and 90nm CMOS Technology

Techno-logy	Leakage Current	Power Dissipation	Delay
180nm	2.25E-23 A	4.5E-23 W	0.01612 µs
90nm	5.40E-24 A	8.10E-24 W	0.00324 µs
45nm	3.15E-23 A	3.15E-23 W	0.00189 µs

VI. CONCLUSION

After comparing the leakage current, power dissipation and delay timing results of 17T FA Cell and Carry Save Adder in 180nm and 90nm CMOS Technology we can conclude that as we shrink the Technology i.e. gate length we get more efficient and faster circuits so that when it is used in Digital Signal Processing (DSP), Fast Fourier Transform (FFT) and other applications where timing constraints are crucial, we will be able to meet timing requirements and performance is improvement defiantly with lesser area.

VII. FUTURE SCOPE

The proposed design further can be modified by replacing each full adder with 10T or 7T FA Cell so that the speed can be further but all this is possible at the cost of some tradeoff between leakage current & power dissipation.

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