Circuit Design of Low Area 4-bit Static CMOS based DADDA Multiplier with low Power Consumption

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Abstract— **Multiplier has vast applications, so designers are competing with each other if one comes up with high Speed then other one might come up with low Area like that mix of VLSI design constraints is the concern here. Till now most of the persons who has name on Multipliers had their own approach. In this paper we are intended to introduce Conditional approach in which Circuit can be designed for Logic0 Conditions or for Logic1 Conditions. Here we are not curious to get the expression and then convert that into a Cmos Circuit based on de-morgan's theorem. Transistors will be the leaf level cells in our approach in which we try to utilize each and every Demarcation line and each line gives unique Logic. We want Disadvantage of more Transistor count in CMOS to turn into somewhat less Transistor count by our Conditional approach. DADDA multiplier has been designed by using carry save adder method . The proposed approach implemented on above multiplier has been designed and simulated by using TANNER EDA Software.**

IndexTerms—staticcmos,24Tcircuit,xor,xnor.

I. INTRODUCTION

Multiplication is one of the arithmetic operations performed by multiplier in the various analog and digital circuits. The Area and power dissipation are the important parameters which should be taken into consideration in digital circuits.Binary multiplication can be achieved by several approaches. A combinational circuits of tree multiplier, with a one-sided reduction tree and a ripple-carry adder as the final stage is called an array multiplier [1]. But it has worst case delay. Then fastest Wallace tree multiplier has been introduced for minimum propagation delay. However, the Wallace multiplier has complex structure which will be difficult to layout. Hence an attempt has been made to develop DADDA multiplier which is designed by using 1-bit full adders with Carry Save Adder (CSA).

Now we need to design a multiplier by following our own technique such that functionality mismatch should never occur but design constraints like power and area should be achieved. We have designed multiplier by using STATIC CMOS logic style, it has advantage of low power consumption but dis-advantage of area with respect to number of transistors, so here we will have the challenge to design the

multiplier with less number of transistors. Logic style like PTL(Pass Transistor Logic) has advantage of less number of transistors it has the problem of logic level degradation.

II. MULTIPLIER

Multiplier is going to multiply 4 bits of A(A3 to A0) and 4 bits of B(B0 to B3) and results in eight bit output named P(P8 to P1).we have taken the Base as DADDA Multiplier by using carry save adder method which has used Full Adders and off course they also need 16 two input AND gates for the product terms which are given as the inputs to the Full Adders[9].

The idea was why we require 16 two input AND gates why can't we use NAND gates and then totally redesign the logic such that huge reduction in Transistor count can be achieved. For the product term P1 in the Base design requirement was two input AND gate as inputs A0 and B3 and no way we could able to achieve optimization here , now we have started investigating product term P2 which needed product terms A1B3 and A0B2 but we have replaced that entire section with two 2-input NAND gates with one output and 2-input XOR gate with two outputs and the first output is our product term P2. now we have started investigating product term P3 which needed product terms A0B1 , A1B2 and A2B3 but we have replaced that entire section with three 2-input NAND gates with one output and 3-input 24T Circuit with two outputs and the first output and second output of XOR gate given to nand gate and also OAI 21 circuit with inputs as nand output , XOR second output and 24T Circuit first output, finally OAI 21 followed by an inverter is product term P3.

Now let us see the product term P4 which is the XOR gate first output but that XOR gate has two inputs one input coming from the NAND2 output which required for us to achieve product term P3 and the other input coming from the 24T Circuit first output but 24T Circuit has three inputs , one coming from the AND of A3 and B3, other coming from the 24T Circuit first output and other coming from the second output of 24T Circuit which used to achieve product term P3.

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Product term P5 requires three NAND2 gates , three not gates, two 24T Circuits and one XNOR gate.Product term P6 requires two NAND2 gates, one XOR gate, one XNOR gate and one 24T Circuit.Product term P7 requires one NAND2 gate, one XOR gate and one 24T Circuit. Product term P8 is the second output of the XOR gate which used for achieving P7.

There are 6 cells in this Multiplier named n2, X, N, I, 24T and inverter where n2 corresponds to NAND2 gate which requires 4 transistors, X corresponds to two input XOR gate which requires 10 transistors and it consists of two outputs, N corresponds to two input XNOR gate which requires 10 transistors and it consists of two outputs, I corresponds to three input OAI21 which requires 6 transistors and 24T corresponds to 24 Transistor circuit.

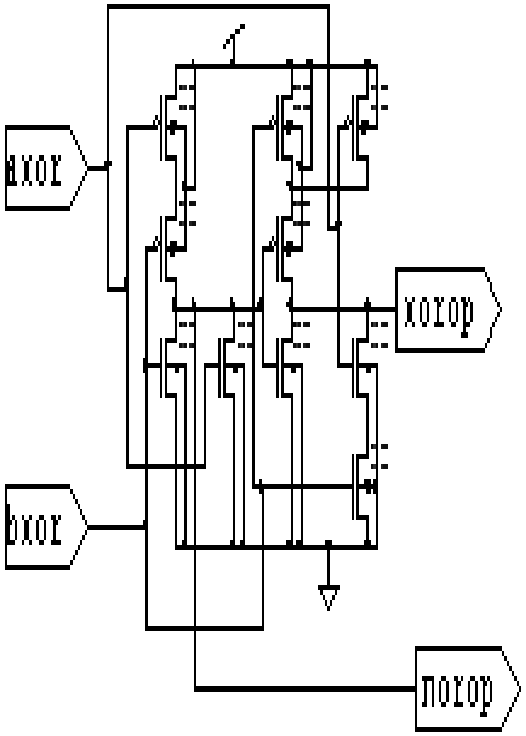

Fig. 1 Two input – Two output XOR gate

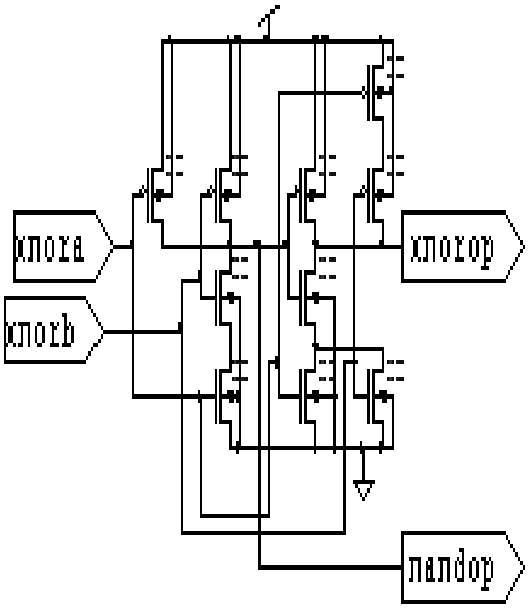

Fig. 2 Two input – Two output XNOR gate

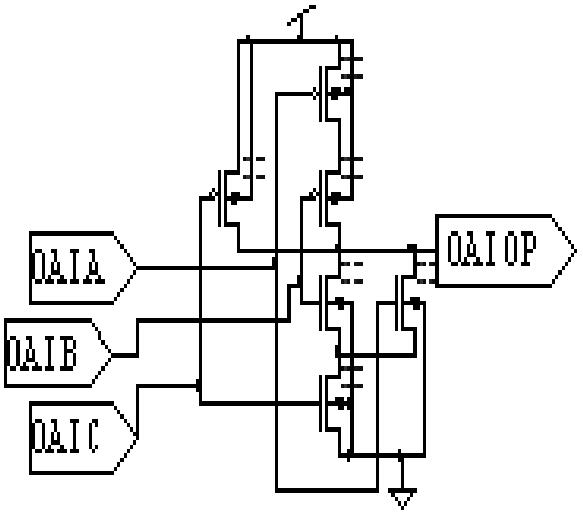

Fig. 3 OAI21 Circuit

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Below figure consists of two outputs and they are just complements of SUM and CARRY outputs of FULL ADDER this cell was needed for us to achieve optimization as DADDA Multiplier was based on FULL ADDER cell and Transistor count for this cell is twenty four , so here itself we have started optimization .

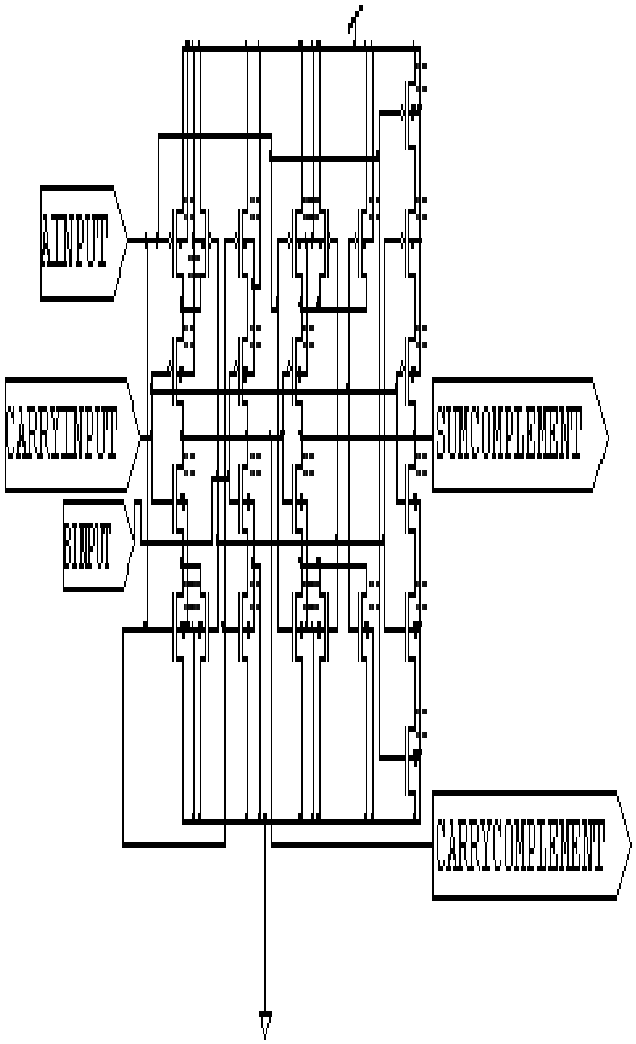

Fig. 4 24T Circuit

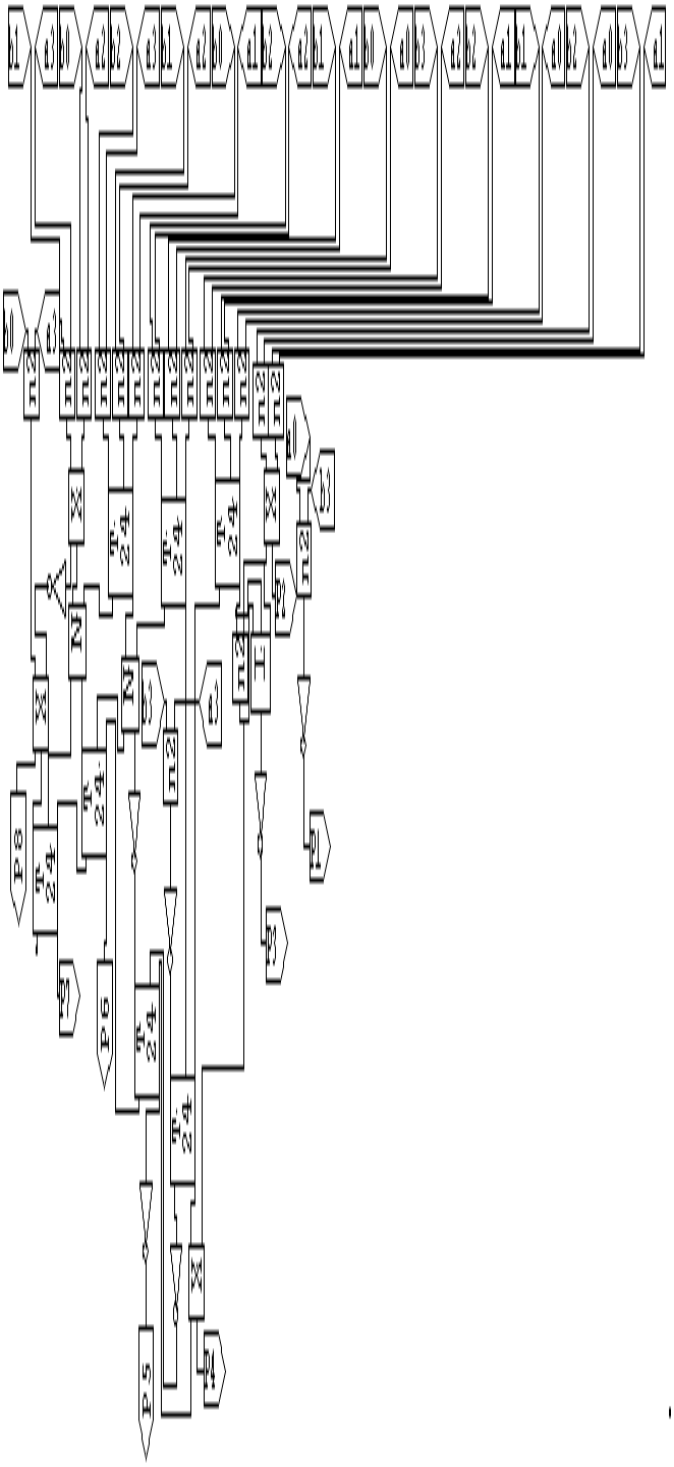

Fig. 5 Proposed 4x4 DADDA Multiplier using CSA

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III. STATIC CMOS

STATIC CMOS has the advantage of Robustness , low power consumption as well as Full output voltage swing if P-MOSFET is on then corresponding N-MOSFET is OFF.STATIC CMOS needs more number of transistors because if we require T-number of TRANSISTORS in the PULL-UP network also needed T-number of TRANSISTORS in the PULL-DOWN network. STATIC CMOS has advantage of full output voltage swing, so these full voltage levels can make sure in the upcoming section's N-MOSFET'S and P-MOSFET'S fully on or off.

We can just design when the output is Logic '1' and then we can just arrange for Logic '0' or vice versa. We can easily differentiate between output voltage high logic level and output voltage low logic level and this will be even more beneficial when the technology is scaled down that is when supply voltage is less then Logic '1' range and Logic '0' range will come down. Even though it is recommended that not more than 4 number of transistors should be in series either in PULL-UP or PULL-DOWN region as delay is going to be worse. Our Design has only 3 number of Transistors in series.

IV. PERFORMANCE ANALYSIS

Implementation of 4-bit Multiplier has been done using STATIC CMOS logic style. Table1 shows AREA comparison of 4x4 DADDA Multiplier using CSA, Proposed 4x4 Multiplier using CSA, Array Multiplier using CSL, CPL and DPL and Tree Multiplier using CSL,CPL and DPL. power dissipation comparison for 4-bit Multiplier using DADDA Multiplier and Proposed Multiplier are shown in TABLE2. This table clearly shows that Proposed DADDA Multiplier has very less power dissipation than DADDA Multiplier using CSA. The Multiplier which we designed using STATIC CMOS logic style uses less number of transistors. It uses 16% less area(number of transistors) than DADDA Multiplier (9) using CSA, 25% less area when compared to CSL of Array and Tree Multiplier (1), 17% less area when compared to CPL of Array and Tree Multiplier (1) and 40% less area when compared to DPL of Array and Tree Multiplier (1).

TABLE1 COMPARISION OF AREA IN FOUR DESIGNS

TOTAL	Design in DADDA Multiplier	Proposed Design (Static cmos)	Array Multiplier CSL CPL DPL	Tree Multiplier CSL CPL DPL
Area (number of transistors)	376	316	432 384 528	432 388 532

TABLE2 COMPARISION OF POWER IN TWO DESIGNS

Parameter	DADDA Multiplier	Proposed Multiplier
Power(mw)	1.85mw	0.07mw

Even though the logic style like CPL by default takes less number of Transistors when compared to Static Cmos which default takes more number of Transistors, we were able to Design with Low Area. The worst case active Transistor count is 50% of total number of Transistors and in our Design it will be 158, in DADDA it is 188 and in CSL of Array and Tree it is 216 and shown in TABLE 3.

TABLE3 COMPARISION OF ACTIVE TRANSISTORS IN FOUR DESIGNS

ACTIVE	Design in DADDA Multiplier	Proposed Design (Static cmos)	Array Multiplier CSL	Tree Multiplier CSL
(number of transistors)	188	158	216	216

V.CONCLUSION

Power is becoming an important design constraint these days especially because of the battery operated devices as well as Area which in turn directly proportional to Cost of the Design one would always wants to buy a product with low cost and we can also incorporate additional functions with in the prescribed Area.we came with our own Design it was possible because of the FULL-CUSTOM Design which allows us to Design our own circuit by taking the leaf level cells as gates or may be Transistors since our Design is implemented in Transistors we have been able to acheive area and power constraints, even though we want Speed also to be more it is also possible because we have optimized the logic and it is not like sacrificing one Design constraint to achieve another constraint. we have designed our Multiplier by using STATIC CMOS logic style which generally requires more number of transistors.

we are able to design the multiplier by using less number of transistors than DADDA Multiplier by using CSA. It shows an 4-bit Multiplier of the proposed technique only needs 316 transistors.

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