Comparative Analysis of VLSI circuits using multigate devices.

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Abstract- **The enhancement in the scaling technology has increased the need of low power based circuits. In nanometer regime, CMOS based circuit may not be used due to problem in its fundamental material, short channel effect and high leakage. There is need of better technologies for handling the various consequences of MOSFET technology. FinFET technology presents an alternative to classical MOSFET to achieve low power applications. Today the need to design logic circuits with low power, small area and lower power dissipation with high reliability is increasing. All the logic circuits like Inverter and NAND2 gate in this paper are designed and simulated using HSPICE by Synopsis. This paper presents comparative analysis of MOSFET and FinFET based logic circuits using 32nm technology . It is found that amongst all the designs FinFET based circuits are more suitable for low power applications in nanometer regime. The power dissipation is also found to be 0.247µW for inverter and 0.131 µW and 0.096 µW for NAND2 gate in SG and IG mode which is low.**

Index Terms—**Multigate (MG), FinFET, HSPICE, low power device, power dissipation, Inverter,NAND2 gate.**

I. INTRODUCTION

The dynamic and fast evolution of electronics and communications industry has been actually possible by enhancing progress in CMOS technology. This progress is based on dimensional scaling, that results in exponential growth in both device density and performance. The reduction in the costing is also decreasing as the new technologies emerge. The other factors such as high input resistance, self isolation, zero static power dissipation, simple layout and process steps have made CMOS transistors as the main components of the current integrated circuits (ICs). MOSFETs brought great development in developing the VLSI domain through its various features.

The improved circuit performance and density made essential more transistors to be integrated on one single chip which gave rise to complicated functionality. It was also observed that when higher electric fields were generated the transistor device worsened. This affected the reliability of circuits. As the requirements of more number of transistors increased it resulted in higher doping which caused challenges
like mobility degradation and random dopants induced threshold voltage fluctuations. Power is also a limiting factor in VLSI integration. The resulting heat dissipation also limits the performance of VLSI chip. Reduction of power consumption is an issue in CMOS circuit design. As the requirement of low power devices increases, it is essential to reduce the power dissipation. By lowering the supply voltage (VDD), the power consumption can be reduced. As VDD is lowered, gate delay is increased and hence it is observed that low operating frequency is present. Low power devices can be achieved by using an alternative solution instead of CMOS based design like Double Gate FETs or FinFETs. All this consequences lead to the evolution of multigate devices as that leads to the path of evolution era in the VLSI technology.[1][2]

A multigate device refers to MOSFET semiconductor which consists of more than one gate. Single gate electrode is used for controlling multiple gates of the transistor. Whereas the multiple gate surfaces act electrically as a single gate, or by independent gate electrodes. A multigate device employing independent gate electrodes is sometimes called a Multiple Independent Gate Field Effect Transistor (MIGFET).There are different types of multigate devices such as Planar double-gate transistor, Flexfet,FinFET,Tri-gate transistor,Gate-all-around (GAA) FET.Here emphasis is on FINFETs.In this paper we design and analyze different designs of FinFET based logic circuits to work efficiently and with low power, size and power dissipation.

This paper is organized as follows. Sections II describes about the FinFET structure. The circuit descriptions and simulation results are presented in sections III and IV respectively followed by performance comparison of the different designs in section V. Finally section VI concludes the whole work.

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II. FINFET STRUCTURE

Steady miniaturization of transistor with each new generation of bulk CMOS technology has yielded continual improvement in performance of circuits. But scaling of bulk CMOS faces challenges due to fundamental material and process technology limits. The primary obstacles to the scaling of bulk CMOS to 32nm gate lengths include short channel effects, Sub-threshold leakage, gate-dielectric leakage and device to device variations. But FinFET based designs offers the better control over short channel effects, low leakage and better yield [3, 6] below 45nm helps to overcome the obstacles in scaling. Double Gate devices have been used in a variety of innovative ways in digital and analog circuit designs.

FinFET are non planar double gate transistor built on Silicon on Insulator (SOI) substrate. The important characteristic of the FinFET is that the conducting channel is enfolding by the thin silicon "fin", which creates the gate device [4]. The thickness of the fin which is measured in the direction from source to drain, determines the effective channel length of the device. A parallel transistor pair consists of two transistors with their source and drain terminals tied together. In Double-Gate (DG) FinFETs, the second gate is added opposite to the traditional gate, which has been recognized for their potential to better control short channel effects, as well as to control leakage current. Fig. 1. shows the schematic diagram of FinFET structure

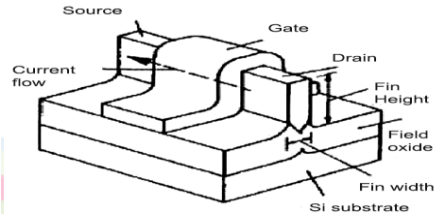


Fig.1 FinFET structure [4]

There are basically 4 types of FinFET configuration/modes as follows:- The operations of FinFETs is identified as Short Gate (SG) mode with transistor gates tied together, the Independent Gate (IG) mode where independent digital signals are used to drive the two device gates, the Low-Power (LP) mode where the back gate is tied to a reverse-bias voltage to reduce leakage power and the hybrid (IG/LP) mode, which employs a combination of low power and independent gate modes [5].

Fabrication of FinFETs is compatible with that of conventional CMOS, thus making possible very rapid deployment to manufacturing. The major advantages of FinFET include the following:

(1) Nearly ideal subthreshold slope.
(2) Small intrinsic gate capacitance.
(3) Smaller junction capacitances.
(4) Better immunity to SCEs.
(5) Design flexibility at circuit level with shorted gate (SG) and independent gate (IG) options.

In this paper two configurations namely: SG-mode FinFETs and IG-mode FinFETs are considered

III CIRCUIT DESCRIPTION

A. FinFET based Inverter

Fig.2 shows schematics of FinFET based Inverter using FinFET in SG mode. Vin and Vout serves as the inputs and output respectively.

SG mode inverter gates take lesser delay than other modes of inverter gates. Thus, the SG mode is conductive in high performance design.

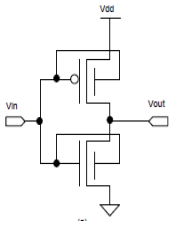
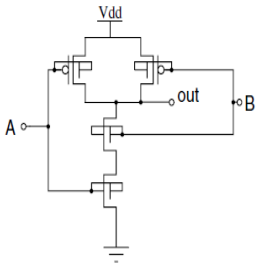


Fig.2 Inverter using FinFET in SGmode

B.FinFET based NAND2

a) SG mode NAND2

In SG mode NAND2, both p-type FinFET and n-type FinFET transistors back gates are connected to their front gates; this composition is best suitable for high performance application.



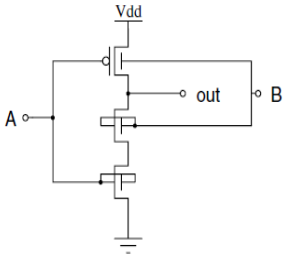


Fig.3 Fig.4

Fig.3: NAND2 using FinFET (SGmode) ,Fig.4 : NAND2 using FinFET (IGmode)

In IG mode NAND2 gate ; in which single p-type FinFET transistor has connected to two input signals (one input at the front gate and other at the back) and the rest of the two n-type FinFET transistors connected in SG mode. This design result in a reduction of one p-type FinFET and is conductive in area significant designs.

III. SIMULATION RESULTS

All the MOSFET and FinFET based logic circuits like inverter and NAND2 gate are simulated on the circuit simulator HSPICE by Synopsis using 32nm Predictive Technology Model. Simulation is carried out with signals having equal rise and fall time with 50% duty cycle. The length and width of the MOSFETs and FinFETs are optimized precisely such that simulation results are with minimum error.The power supply for MOSFET based circuits using 32nm technology is 1V and that for FinFET based circuits is 0.8V

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i) MOSFET based Inverter

The waveforms shown below in Fig.5 describes the operation of MOSFET based inverter circuit using 32nm

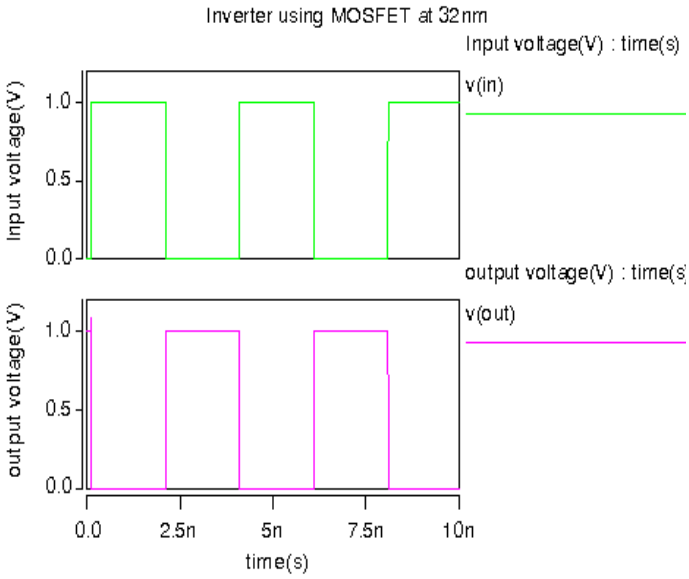

Fig.5 Waveforms for MOSFET based Inverter using 32nm

ii) MOSFET based NAND2 gate

The waveforms shown below in Fig.6 describes the operation of MOSFET based NAND2 gate circuit using 32nm.

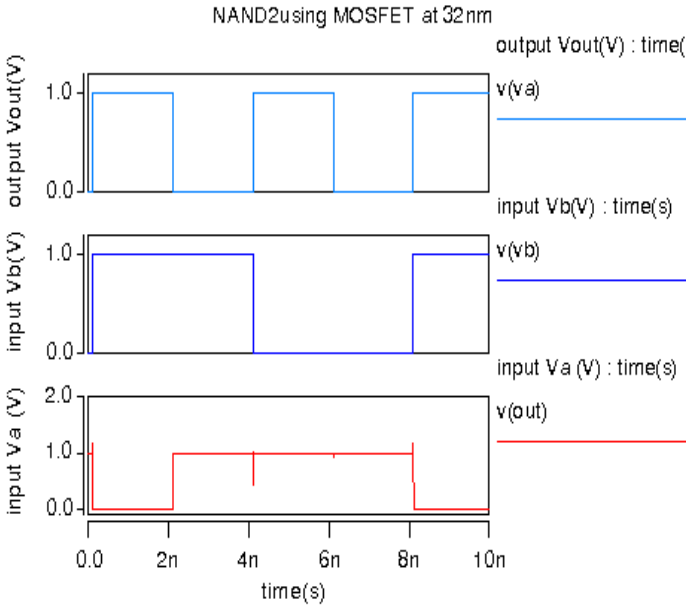

Fig.6 Waveforms for MOSFET based NAND2 using 32nm

iii) FinFET based Inverter

The waveform shown below in Fig.7 describes the operation of FinFET based inverter circuit using 32nm where FinFET is in SG mode.

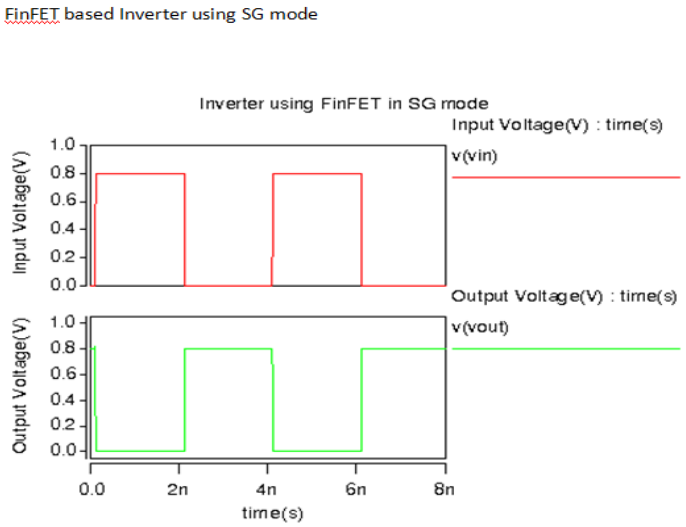

Fig.7 Waveforms for NAND2 using FinFET (SGmode)

iv) FinFET based NAND2 gate

The waveform shown below in Fig.8 a Fig.9 describes the operation of FinFET based NAND2 for SG mode an IG mode using 32nmFinFET technology.

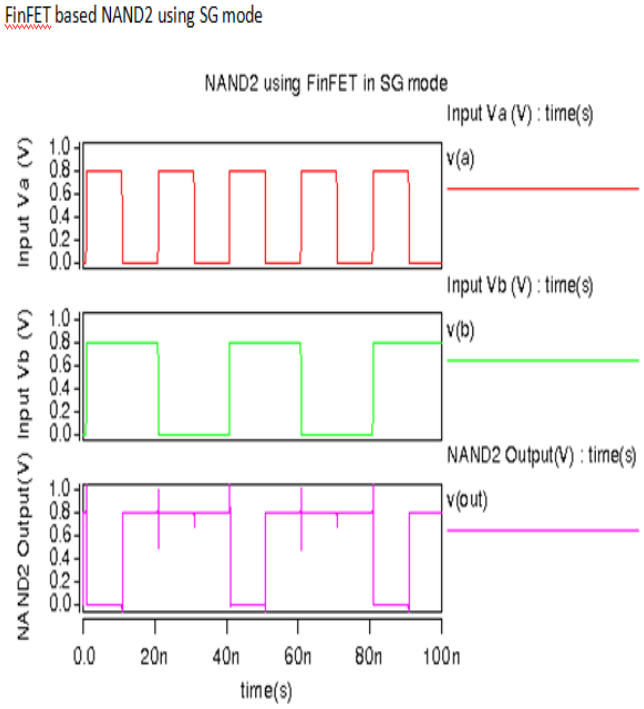

Fig.8 Waveforms for NAND2 using FinFET (SGmode)

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FinFET based NAND2 using IG mode

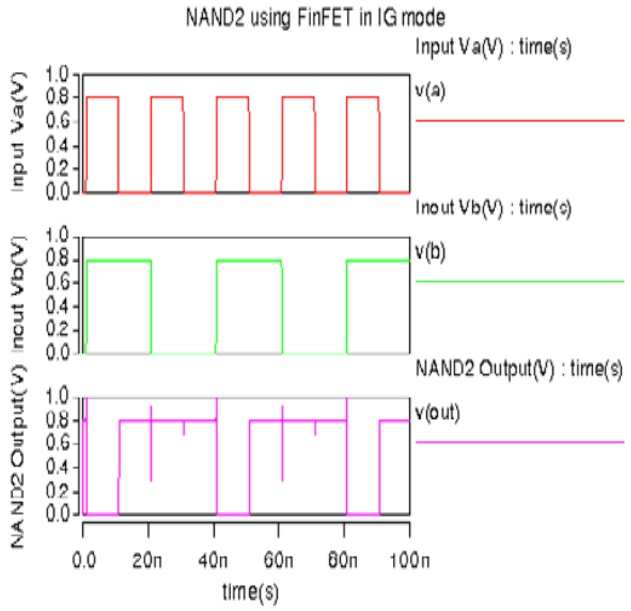

Fig.9 Waveforms for NAND2 using FinFET (IGmode)

V. PERFORMANCE COMPARISON

Table I depicts comparison of various performance parameters for the FinFET and MOSFET based Inverter circuit. It is seen that FinFET based inverter operates at lower supply voltage i.e 0.8V , has lowest power dissipation of 0.247µW and smaller area.

TABLE I. COMPARATIVE ANALYSIS OF Inverter using MOSFET and FinFET technology

Parameter	FinFET based Inverter	MOSFET based Inverter
Technology	32nm	32nm
Tool	Hspice	Hspice
Supply voltage	0.8	1V
Average power dissipation(µW)	0.247µW	0.349mW
Transistor count	2FinFETs	2MOSFETs

Table II depicts comparison of various performance parameters for the FinFET and MOSFET based NAND2 circuit. It is seen that FinFET based NAND2 circuit operates at lower supply voltage i.e 0.8V , has lowest power dissipation of 0.096µW in IG mode and smaller area.

TABLE II. COMPARATIVE ANALYSIS OF NAND2 gate using MOSFET and FinFET technology

Parameter	Finfet based NAND2 SG mode	Finfet based NAND2 IG mode	MOSFET Based NAND2
Technology	32nm	32nm	32nm
Tool	Hspice	Hspice	Hspice
Supply voltage	0.8	0.8	1V
Average power dissipation(µW)	0.131µW	0.096 µW	0.328mW
Transistor count	4 FinFETs	3FinFETs	4MOSFETs

VI.CONCLUSION

In VLSI systems power consumption should be minimum for high performance and reliablity . In this paper we compare the performance of different designs of logic circuits like inverter and NAND2 gate designed using MOSFET and FinFET technlogy. Operating frequency remains same for all the circuits. Amongst all the FinFET based logic circuits not only operates at low supply voltage but also has low power consumption and smaller area. Thus FinFET technology is a good alternative to planar CMOS for scaling beyond 32nm and having superior performance for low power applications.

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