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Carry Select Adder Pipelined Architecture for FFT

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Abstract
Fast Fourier Transform (FFT) is commonly used essential tool in digital signal processing applications. The adder plays a very important role in it. To obtain optimized adder design in terms of delay and area, several works have been proposed earlier. In this paper, performance targeted carry select adder (CSLA) with D-latch is proposed. An FFT application will be performed by using the proposed work to showcase the performance improvement. It is observed that a 34% improvement is observed when compared against conventional adders.

I. INTRODUCTION

Fast Fourier transform (FFT) is one of the most widely used operation in digital signal processing algorithms. The FFT is an efficient class of computational algorithms of the DFT. The fast Fourier Transform analysis is to convert the original signal to a frequency domain signal and vice versa. FFT involves the mathematics such as multiplier, adders and subtractions. In an *N*-point DFT, to evaluate each DFT sample value, we have to perform *N* multiplications and *N-1* additions using complex numbers. *N* such computations are required in all, therefore there will be N^2 complex multiplications and *N(N-1)* complex additions. The FFT procedure for synthesizing and analyzing the Fourier series was given by Cooley and Tukey. These methods provide a divide and conquer approach to the computation of DFT. This is based on the decomposition of N point DFT into successively smaller DFTs. In an *N*-point sequence if *N* can be expressed as $N = r^m$, then the sequence can be designated into *r* point sequences where *m* denotes the number of stages of computation and *r* denotes radix of the FFT algorithm. Here the decimation can be performed *m* times where $m = \log_2 N$. The total number of complex additions are reduced to $N\log_r N$ and total number of complex multiplications are reduced to $(N/2)\log_r N$. The two different Radix-2 algorithms are Decimation-In-Time (DIT) and Decimation-in-Frequency (DIF) algorithms. In both these algorithms *N* inputs are divided into two *N/2* sequences.

In this paper we make use of DIF algorithm because of its improved accuracy. For DIF algorithm the output point's frequency is subdivided. The output obtained by this method will be in bit reversed order. Radix-2 algorithm is an efficient algorithm that multiplies two signed numbers using 2's compliment form. The number of partial products is reduced by half for this algorithm.The speed depends on addition of partial products. The critical path for the multiplier is on the number of partial products. The partial products generated are added using conventional adders which uses high amount of logic resources, delay & power. Many fast adder exits, but adding fast with low delay and power is still challenging. To overcome this we proposed carry select adder with D-latch instead of Regular CSLA and BEC to achieve lower area, delay and power consumption. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. Carry Select Adder is a logic element that computes (n+1) bit sum of two n-bit numbers. Carry select method is having a good compromise between cost and performance in carry propagation method.

The rest of this paper is organized as follows. Chapter II provides earlier work generated on CLA used for implementation of FFT. Chapter III describes architecture to optimize computational time. Our proposed FFT architecture using carry select adders is discussed in Chapter IV. Chapter V depicts experimental analysis for obtained results followed by conclusion.

II. RELATED WORK

The adder used in butterfly computation is the carry select Adder (CSLA) which is one of the fastest adder .The main advantage is that the arithmetic operations follows pipelining operation and addition is done using CSLA, so it reduces the overall computation time& power consumption. Different carry select (CS) methods have been suggested to reduce the delay and power.

In 1962, O.J.Bedrij [1] proposed a conventional carry select adder (CSLA).It is an RCA-RCA configuration that generates a pair of sum words and output-carry bits corresponding to carry inputs (C_{in} =0 and C_{in} = 1) and selects one out of each pair for

final-sum and final-output-carry using the control signal C_{in}. A conventional CSLA has less CPD than an RCA, but the design is not attractive since it uses a dual RCA.

Later in 1998, to obtain a lower transistor count, an add-one circuit was proposed by T.Y. Chang [2]. One group of RCA is replaced by an add-one circuit to achieve a 29.2% area reduction at the expense of 5.9% speed penalty for a 64-bit CSL over the conventional dual RCA design.

In 2001, Youngjoon Kim and Lee-Sup Kim [3] introduces a multiplexer based add-one circuit is proposed to reduce the area with negligible speed penalty. A carry-select adder can be implemented by using a single ripple carry adder and add-one circuits instead of using dual ripple carry adders. A multiplexer-based add-one circuit is proposed to reduce the area with negligible speed penalty.

For bit length n=64, this new carry select adder requires 42 % fewer transistors than the conventional carry select adder and 29% fewer transistors than Chang'scarryselectadderusingsingleripplecarryadder. Fewer transistors results less area and less power

He et al. [5] proposed a square-root (SQRT)-CSLA to implement large bit-width adders with less delay. In a SQRT CSLA, CSLA's with increasing size are connected in a cascading structure. The main objective of SQRT-CSLA design is to provide a parallel path for carry propagation that helps to reduce the overall adder delay.

A CSLA based on common Boolean logic (CBL) is also proposed in [6] and [7]. The CBL-based CSLA of [6] involves significantly less logic resource than the conventional CSLA but it has longer CPD, which is almost equal to that of the RCA. To overcome this problem, a SQRT-CSLA based on CBL was proposed in [7]. However, the CBL-based SQRT-CSLA design of [7] requires more logic resource and delay than the BEC-based SQRT-CSLA of [5].

In all the above techniques area and power is reduced greatly up to some extent but the delay is not reduced. Delay affects the speed of addition. In order to increase the speed of addition i.e., less delay a unique approach is proposed. This method replaces the BEC by D-latch with enable signal. Carry selection unit is used for the selection of carry bits. The proposed 32 bit CSLA using D latch involves nearly 34% less delay compared to regular CSLA and modified BEC based CSLA& the power is reduced to nearly 33% when compared to regular CSLA and 21% compared to modified BEC based CSLA. Experimental analysis shows that the proposed architecture achieves the three folded advantages in terms of area, delay and power.

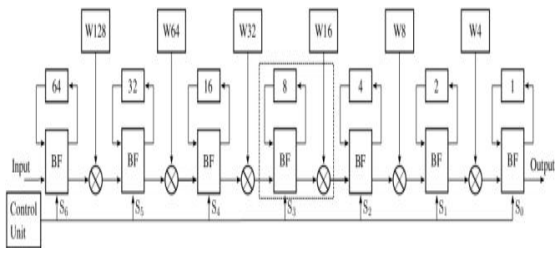
III. METHODOLOGY

Before the development of FFT architecture it was difficult to process the data for digital signal processing circuits. The different architectures were developed to improve the performance of DFT in terms of FFT. But each FFT architecture has a drawback that it needs more ROM to store the twiddle. For each cycle of operation the number of hardware components increased. To overcome this pipelined FFT architectures have been introduced.

A. Pipeline architecture:

These architectures can achieve a high throughput and low latency which are suitable for real time applications. These pipelined FFT architectures can be classified as a Single path delay feedback (SDF) and Multi-path delay commutator (MDC), according to the dataflow scheme.

To improve hardware efficiency, the SDF architecture is used to share the same delay elements between butterfly inputs and outputs, but the architecture operates at a low throughput due to the single path. The single-path delay feedback (SDF) pipeline FFT is good in its requiring less memory space (about *N-1* delay elements) and its multiplication computation utilization being less than 50%, as well as its control unit being easy to design. Such implementations are advantageous to low-power design, especially for applications in portable DSP devices. Based on these reasons, mostly SDF pipeline FFT is adopted. However, the FFT computation often needs to multiply input signals with different twiddle factors for an outcome, which results in higher hardware cost because a large size of ROM is needed to store the wanted twiddle factors. The complex multipliers used in the processor are realized with shift-and-add operations. Hence, the processor uses only a two-input digital multiplier and does not need any ROM for internal storage of



coefficients. However, low speed and higher

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hardware cost caused by the proposed complex multiplier are the pay-off. An example 128-point radix-2 FFT architecture is shown in Fig. 1.

Fig. 1 Architecture of a 128-point radix-2 FFT architecture [10].

B. Adder in butterfly unit:

The adder circuit used in the butterfly structure is the carry select adder which consists of two Ripple Carry Adders (RCA) with C_{in}=0 and C_{in}=1 and a Multiplexer. The problem in CSLA design is that it is not area efficient because it uses multiple pairs of RCA to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the MUX which is shown in the Fig. 2.

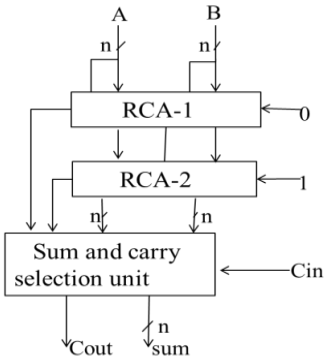

Fig. 2 Conventional CSLA

In order to improve the shortcomings of CSLA, we use Binary to Excess-1 Converter (BEC) instead of RCA with C_{in}=1 in the regular CSLA. The structure of proposed adder is shown in the Fig. 3. The main advantage of this BEC logic comes from the lesser number of logic gates than the *n*-bit Full Adder (FA) structure.

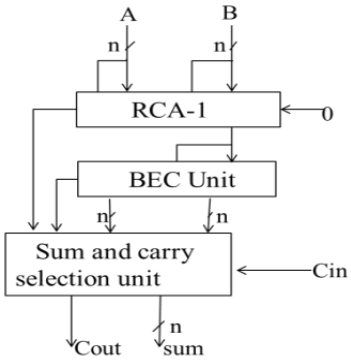

Fig. 3 BEC based CSLA

The logic for BEC unit is shown in Fig. 4 and the corresponding logic equations are as follows.

$$X0 = \sim B0 \quad (1)$$
$$X1 = B0 \wedge B1 \quad (2)$$
$$X2 = B2 \wedge (B0 \,\&\, B1) \quad (3)$$
$$X3 = B3 \wedge (B0 \,\&\, B1 \,\&\, B2) \quad (4)$$

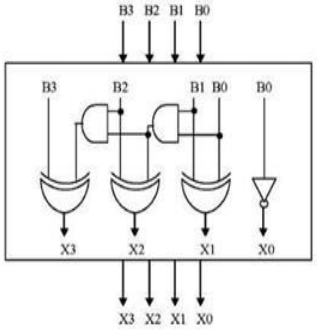

Fig. 4 BEC logic

IV. PROPOSED ADDER

When the modified CSLA is simulated and synthesized, the area and power is less in the CSLA with BEC but the delay is not reduced. Speed of addition is crucial for FFT implementation. So we can improve the above structure in terms of less delay and higher speed by replacing the BEC with a D-Latch. The improved carry select adder using D-latch is shown below.

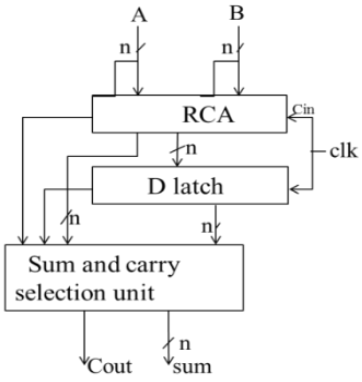

Fig. 5 CSLA using D latch

Latches are used to store one bit information. Their outputs are constantly affected by their inputs. In other words, when they are enabled, their content changes immediately according to their inputs. In

other words, when they are enabled, their content changes immediately according to their inputs. The architecture of proposed 32-bit CSLA is shown in Fig. 6.

It has different eight groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used to reduce the area, delay & power consumption. Each of the two additions is performed in one clock cycle. This is 32-bit adder in which Least Significant Bit (LSB) adder is ripple carry adder, which is 2 bit wide.

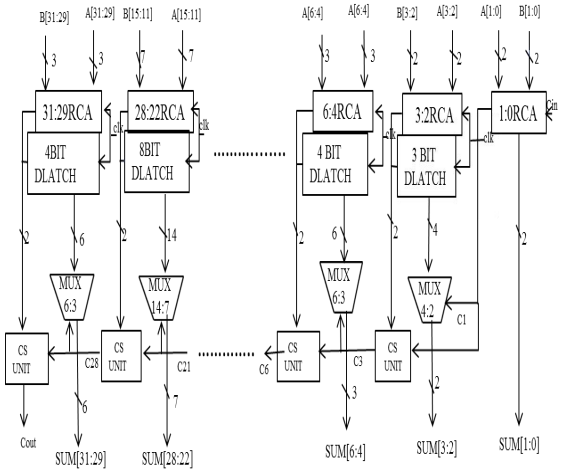

Fig. 6 32-bit CSLA using D latch

The upper half of the adder, i.e., most significant part is 30-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. From the figure it can understand that latch is used to store the sum and carry for C_{in}=1 and C_{in}=0.Carry out from the previous stage, i.e., least significant bit adder is used as control signal for multiplexer and carry selection unit to select final sum and output carry of the 32-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed is the output carry. In the D-LATCH architecture first stage is designed based on Ripple Carry adders and the second stage is designed based on the D-LATCH logic.

V. EXPERIMENTAL RESULTS

Efficient FFT implementation using carry select adders with D-latches architecture is implemented in Verilog, simulated using ModelSim and synthesized on Xilinx ISE 12.3i Spartan-3E family device XC3S500E 4FG320. Table I shows performance comparison of different carry select adders. Table II shows performance of FFT using different carry select adders. From the simulation results the delay of FFT implementation using CSLA with D-latch is reduced by 23%

Table 1 Performance comparison of CSLA

Adder Type	Delay (ns)	Power (mw)
Regular CSLA (32 bit)	25.34	163
Modified BEC based CSLA (32 bit)	25.18	139
Proposed CSLA using D latch (32 bit)	16.71	110

Table 2 Performance comparison of pre-adder & FFT using CLA

Adder Type	Delay (ns)
FFT using pre- adders (128 bit)	51
FFT using carry select adders with D-latches (128 bit)	39

Increasing in speed makes this FFT algorithm applicable for various re-configurable VLSI applications.

VI. CONCLUSION

The design of Radix-2 FFT with 128-point is done and simulated using Modelsim. The proposed structure is synthesized in Xilinx ISE 12.3i. A simple approach is proposed in this paper to increase the speed of FFT architecture. The reduced number of gates by replacing regular CSLA with modified CSLA with D-latch offers the great advantage in the reduction of area and also increases the speed.

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