Survey paper on Implementation of FPGA based Parallel Microprogrammed FIR Architecture

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ABSTRACT— In the modern world, digital signal processing (DSP) is the fundamental technology used in communication system.FIR filter is the essential element in digital signal processing application ranging from image and video processing to wireless communication. This paper presents the implementation of field programmable gate array (FPGA) based parallel microprogrammed FIR architecture. Digital FIR filter includes datapath unit and control unit. The datapath unit consists of multipliers, adders and delay elements and the control unit contains the microprogram controller to control the operation of datapath unit. In the FIR filter, multiplication is the key element required to improve the performance of FIR filter, as the multiplier is the more power consuming element. In this paper Wallace tree and Vedic multipliers are used for implementation of microprogrammed FIR filter architecture. The proposed FIR filter is coded in VHDL using modular design approach and implemented in Virtex-5 FPGA. Based on implementation result obtained through Xilinx ISE tool, performance evaluation is done.

Index Terms— FIR filter, microprogrammed, Multiplier, FPGA.

I. INTRODUCTION

The digital signal processor (DSP) applications are video processing, image processing, wireless communication. Filtering is the fundamental step used in such digital signal processing applications. Digital filters are an important type of linear time invariant (LTI) system designed for removing random noise from the signal, spectral shaping, motion estimation, noise reduction and channel equalization among many other applications. Basically, digital filters are Finite impulse response (FIR) and infinite impulse response (IIR) filters used in different application. Because of absolute stability and linear phase properties the FIR filters are extensively used. The key blocks used in the implementation of digital FIR filter are adder, multipliers and delay elements. Basically, the FIR filter performs linear convolution of N-data sample which can be mathematically expressed as:

$$y(k) = \sum_{n=0}^{N-1} w(n).x(k-n)$$

The direct form implementation of an FIR filter can be developed from the convolution sum as shown in fig. below:

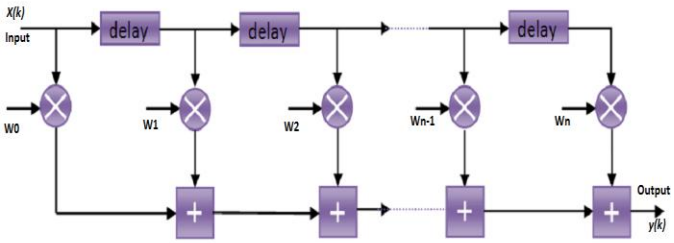

Fig. : Direct form FIR filter architecture

The objective of this paper is to implement the parallel microprogrammed FIR filter using Wallace tree and Vedic multiplier and evaluate the performance of them.

II. LITERATURE SURVEY

P. Kollig, B. M. Al-Hashimi, K. M. Abbott [1] presented the paper on "FPGA Implementation of High Performance FIR Filter". In this paper, 64-tap linear phase filter operating at 1.4 MHz is designed with 60dB attenuation at 0.28fs, 12dB attenuation at 0.25fs based on explicit multiplier. The implementation result was tested on Xilinx XC4006E device. The author concluded that,

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pipelined multiplier provides best trade-off between speed and resource requirement.

Hanho Lee, Gerald E. Sobelman [2] presented the paper on "FPGA Based FIR Filter Using Digital Serial Arithmetic". In this paper, digital-serial 5-tap FIR filter on a Xilinx XC4010 FPGA is implemented. The author concluded that, digital-serial design with digit-size of 2 bit have about 17% smaller area-time product than those of bit-serial implementations.

Lin Jieshan, Huang Shizhen [3] presented the paper on "An Design of the 16-Order FIR Digital Filter Based On FPGA". In this paper, introduces the design and simulation of FIR filter which is mainly based on FPGA, Quartus II and Matlab. The author concluded that, the use of this software significantly shortens the R& D period and it is able to greatly improve the speed of the filter by use of the pipelining structure.

Asgar Abbaszadeh, Khosrov D. Sadeghipour [4] presented the paper on "A New Hardware Efficient Reconfigurable FIR Filter Architecture Suitable For FPGA Application". In this paper, a new hardware efficient reconfigurable FIR filter architecture is proposed based on binary signed subcoefficient method. Using this method the hardware requirement for the multiplexer unit is reduced with respect to typical method. The author concluded that, the FPGA synthesis results of the designed two filters based on 3-bit and 4-bit partitioning have been shown 33% and 27% reduction in the resource usage with respect to two state of art architecture.

Bahram Rashidi, Farshad Mirzaei, Majid Pourormazd [5] presented the paper on "Low Power FPGA Implementation of Digital FIR Filter Based on Low Power Multiplexer Base Shift/Add Multiplier". In this paper, implementation of low power and low area digital Finite Impulse Response (FIR) filter is presented. The proposed FIR filter has been synthesized and implemented using Xilinx ISE V7.1 and Virtex IV FPGA. The author concluded that, the minimum power achieved is 56mw in fir filter based on shift/add multiplier in 100MHz with 8-bit input and 8-bit coefficient.

B. Mamatha, V. V. S. V. S. Ramachandram [6] presented the paper on "Design and Implementation of 120-Order FIR filter Based on FPGA". In this paper, high speed FIR filter is implemented using registered adders and hardwired shifts and modified common subexpression elimination algorithm is used to reduce the number of adders. The implementation result was tested on ALTERA devices. The author concludes that, by using this method the significant area and power is reduced as compared to Distributed Arithmetic technique.

Mrs. Pooja, S. Puri, Mr.U. A. Patil [7] presented the paper on "High Speed Vedic Multiplier in FIR Filter on FPGA". In this paper, FIR filter is designed using fast method for multiplication based on ancient Indian Vedic mathematics. Vedic multiplication is based on Urdhava Tiryakbhgyam sutra. The coding is done in VHDL and synthesis is done using Xilinx ISE series. The author concludes that, Vedic multiplier achieves high speed by reducing gate delays and the Urdhava Tiryakbhagyam method is more efficient than conventional method.

Vijender Saini, Balwinder Singh, Rekha Devi [8] presented the paper on "Area Optimization of FIR Filter and its Implementation on FPGA". In this paper, multiplication with Canonical Sign Digit (CSD) and binary number is simulated and implemented on the Spartan devices. The author concludes that, the area in terms of number of slices is optimized by 80% in Canonical Sign Digit Algorithm.

N. Jhasi, B. R. B. Jaswanth [9] presented the paper on "Design and Analysis of High Performance FIR Filter Using MAC Unit". In this paper, the better performance FIR filter using low power adder and multiplier is implemented. The carry skip adder and modified Wallace tree multiplier consumes low power among all adders and multiplier circuit. Implementation result was tested on Xilinx FPGA device. The author concludes that, the proposed FIR filter consumes less power than the conventional FIR filter.

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M. Gnanasekaran, M. Manikandan [10] presented the paper on "Low Delay-High Compact FIR Filter Using Reduced Wallace Tree Multiplier". In this paper, an area efficient and high speed multiplier is designed using Wallace multiplier and reduced carry save adder. This design is coded in Verilog HDL and is simulated by using Modelsim 6.3c and synthesis is done in Xilinx ISE 10.1. The author concluded that, the area delay product of proposed design is less than the existing design.

Sarita Chouhan, Yogesh Kumar [11] presented the paper on "Low Power Designing of FIR Filters". In this paper, the FIR filter is designed using high speed low power multiplier and this multiplier is designed using Modified Booth Algorithm which is controlled by detection unit using an AND gate and carry save adder. The author concludes that, the proposed high speed low power multiplier used in designing the FIR filter can attain 30% speed improvement and 22% power reduction in modified booth algorithm as compared to other conventional multipliers.

Syed Manzoor Qasim, Mohammed S. Bensaleh [12] presented the paper on "Design and FPGA Implementation of Sequential Digital FIR Filter Using Microprogrammed Controller". In this paper, the sequential 4-tap digital FIR filter based on microprogrammed controller is designed. The proposed FIR filter is coded in VHDL using modular design approach and implemented in Spartan-3E FPGA. The author concluded that, the maximum operating frequency of the designed FIR filter is 119.775MHz which is greater than the system clock frequency (50MHz) and consumes small area.

III. FUTURE ENHANCEMENT AND CONCLUSION

From the above literature survey it is concluded that the FIR filter is the essential element in Digital Signal Processing (DSP) applications such as video processing, image processing and wireless communication such that in this paper we basically concentrate on study of different methods for designing of efficient FIR filter. Now the future work is to concentrate on designing of an equivalent parallel architecture of the FIR filter based on microprogrammed controller using Wallace tree and Vedic multiplier, extending tap size of FIR filter architecture and comparing the performance of both architectures i.e. sequential and parallel based on microprogrammed controller.

V. REFERENCE

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