Low Power VLSI Design using Clock-Gating Technique

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Abstract— In this paper clock gating technique is presented for low power VLSI (very large scale integration) circuit design. With the scaling of technology and the need for higher performance and more functionality, power dissipation is becoming a major bottleneck for microprocessor designs. Because clock power can be significant in high-performance processors, we propose a deterministic clock-gating (DCG) technique which effectively reduces clock power. In this paper a 4-bit synchronous counter, Arithmetic and Logic unit(ALU) ,scrambler and descrambler is designed using clock gating.

Index Terms—ALU, Deterministic Clock Gating, Low Power, VLSI

I. INTRODUCTION

There are three performance parameters on which a VLSI designer have to optimize the design i.e. Area, Speed and Power. Today's consumer demands more functionality, small size, high speed and optimized power devices. Consumer demands a smaller size battery with longer life. To do so power have to be minimized at each levels . To optimize power the simplest technique is to shut down the clock supply for those blocks of the sequential circuit which remains idle or not used for long period. [1]

In small signal applications the leakage power increases power consumption during operation and reduces the availability of power which in turn affects the device performance[2,3]. Therefore some minimization techniques are necessary to improve the device performance while reducing the leakage power[4]. Power consumed in a digital circuit is of two types. (1) Static power and (2) Dynamic power. Static power consists of power dissipated due to leakage currents whereas dynamic power consists of capacitive switching power and short circuit power. In VLSI circuit clock signal is used for the synchronization of active components. Clock power is a major component of power mainly because the clock is fed to most of the circuit blocks, and the clock switches every cycle. Thus the total clock power is a substantial component of total power dissipation in a digital circuit [5]. Clock-gating is a well known technique to reduce clock power.

In a sequential circuit individual blocks usage depends on application, not all the blocks are used simultaneously, giving rise to dynamic power reduction opportunity. By clock gating technique, clock to an idle portion is disabled, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit. In clock gating clock is selectively stopped for a portion of circuit which is not performing any active computation [7].Local clocks that are conditionally enabled are called gated clocks, because a signal from the environment is used to gate the global clock signal [6].

II. CLOCK GATING TECHNIQUE

Clock-Gating [8] is the most common register transfer level (RTL) optimization for reducing dynamic power. In clock gating method, clock is applied only to those modules that are working at that instant. Clock-gating support adds additional logic to the existing synchronous circuit [9] to prune the clock tree, thus disabling the portions of the circuitry that are not in use. By adopting the clock-gating approach, power dissipation can be reduced significantly, lowering not only the switching activity at the function unit level, but also the switched capacitive load on the clock distribution network.

Here the clock gating [10] is implemented using AND gates. Fig. 1 shows the schematic of a latch element. A significant amount of power is consumed during charge/discharge cycle of the cumulative gate capacitance Cg [11] of the latch when the clock is fed directly (Fig. 1(a)) and there is no change in the clock cycle. Fig. 1(b) shows the latch with gated clock. By gating the clock, charge/discharge of Cg can be effected only when there is change in the clock cycle thus saving power.

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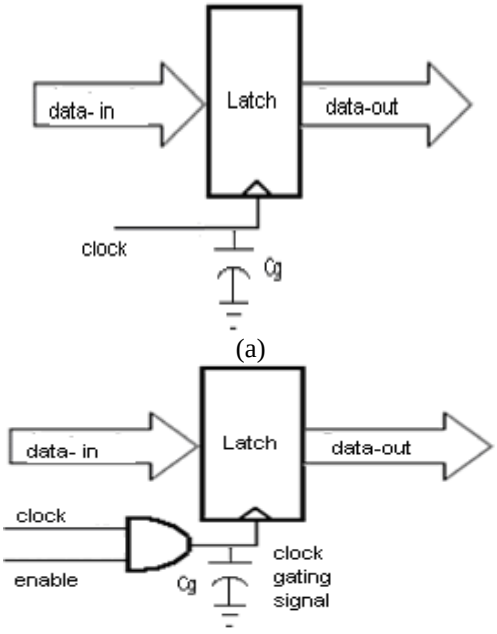

Figure 1. Schematic of Latch Element
(a) without clock gating
(b) with clock gating

III. IMPLEMENTATION OF CLOCK GATING TECHNIQUE

In this paper the above clock gating technique is used to achieve low power dissipation. The Arithmetic and Logic Unit,4-bit synchronous up counte ,scrambler and descrambler circuit are implemented using clock gating technique.

A. Arithmetic and Logic Unit

The ALU, or the arithmetic and logic unit, is the section of the processor that is involved with executing operations of an arithmetic or logical nature. The ALU is an extremely versatile and useful device since, it makes available, in single package, facility for performing many different logical and arithmetic operations.

Arithmetic Logic Unit (ALU) is a critical component of a microprocessor and is the core component of central processing unit. ALU can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. Arithmetic instructions include addition, subtraction, and shifting operations, while logic instructions include Boolean comparisons, such as AND, OR, XOR, and NOT operations[12].
Block diagram of ALU is shown in figure.2.

Arithmetic and logic unit consists of two blocks for different operations-
a. Arithmetic operations.
b. Logical operations

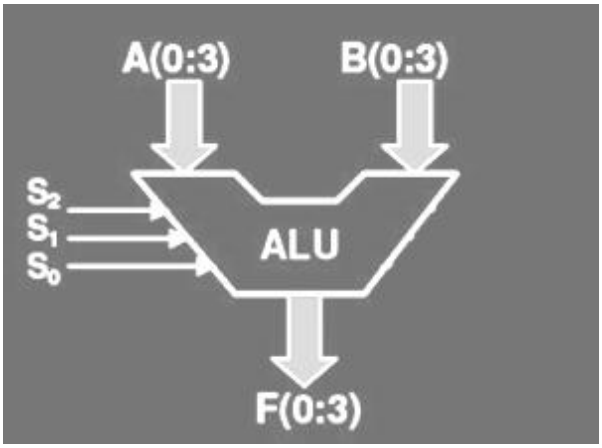

Figure 2: Block diagram of ALU

Addition and subtraction

These two tasks are performed by constructs of logic gates, such as half adders and full adders. While they may be termed 'adders', with the aid of they can also perform subtraction via use of inverters and 'two's complement' arithmetic. A binary adder-subtractor is a combinational circuit that performs the arithmetic operations of addition and subtraction with binary numbers. Connecting n full adders in cascade produces a binary adder for two n-bit numbers.

Logical operations

Further logic gate s are used within the ALU to perform a number of different logical tests, including seeing if an operation produces a result of zero. Most of these logical tests are used to then change the values stored in the flag register, so that they may be checked later by separate operations or instructions. Others produce a result which is then stored, and used later in further processing.

Functionally, the operation of typical ALU is controlled by the three function select inputs (S0 to S2), ALU can perform all the 8 possible logic operations as soon in Table 1.

Table 1: Operations Performed in The Arithmetic Unit Based On S2,S1 and S0 .

S_2	S_1	S_0	Function (F)
0	0	0	A+B
0	0	1	A-B
0	1	0	A-1
0	1	1	A+1
1	0	0	A $\wedge$ B
1	0	1	A $\vee$ B
1	1	0	NOT A
1	1	1	A $\oplus$ B

B. 4 bit binary synchronous up counter

Each of the higher-order flip-flops are made ready to toggle (both J and K inputs "high") if the Q outputs of all previous flip-flops are "high." Otherwise, the J and K inputs for that flip-flop will both be "low," placing it into the "latch" mode where it will maintain its present output state at the next clock pulse. Since the first (LSB) flip-flop needs to toggle at every clock pulse, its J and K inputs are connected to V_{cc} or V_{dd}, where they will be "high" all the time. The next flip-flop need only "recognize" that the first flip-flop's Q output is high to be made ready to toggle, so no AND gate is needed. However, the remaining flip-flops should be made ready to toggle only when *all* lower-order output bits are "high," thus the need for AND gates.

Fig.4 is the RTL schematic of counter using clock gating.

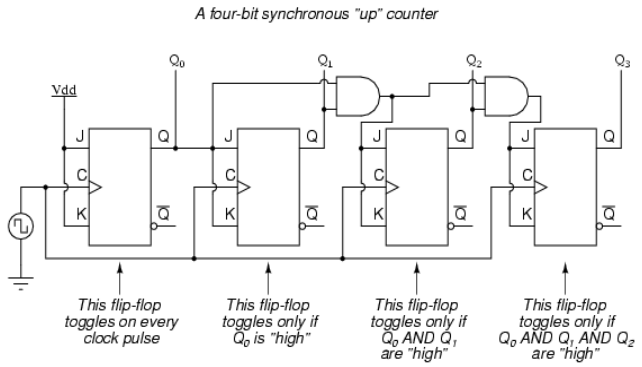

Figure 3: A four-bit synchronous up counter

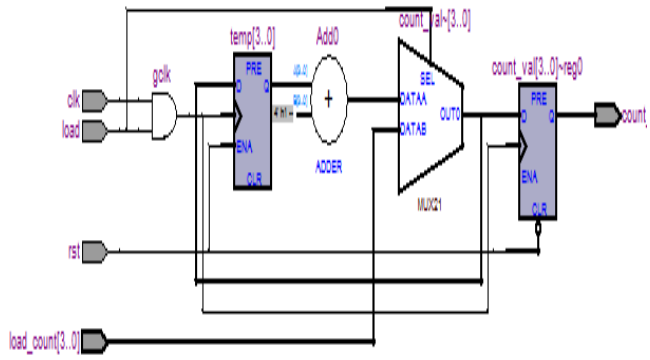

Figure 4: RTL schematic of counter using clock gating.

C. Scrambler and Descrambler

In telecommunications and recording, a *scrambler* (also referred to as a *randomizer*) is a device that manipulates a data stream before transmitting. The manipulations are reversed by a *descrambler* at the receiving side. Scrambling is widely used in satellite, radio relay communications and PSTN modems.

The performance of data transmission systems must be independent of the specific bit sequence being transmitted.If allowed to occur,repeated bit sequences can cause wide variations in the received power level as well as difficulties for adaptive equalization and clock recovery.Since all these problems are eliminated if the bit sequence is "random",many modems employ a data scrambler to produce a pseudorandom sequence for any given input bit sequence.The scrambler usually takes the form of a shift register with feedback connections,while the unscrambler is a feedforward-connnected shift register.

A data scrambler and unscrambler are shown in Fig 4. The scrambler operates in the following fashion. The initial shift register contents are arbitrary but prespecified and fixed to be the same in both the scrambler and unscrambler.The first bit in data in sequence is summed modulo-2 with the modulo-2 sum of locations 12 and 17 in the shift register.This sum becomes the first bit in output bit sequence of stsge I .As this bit is presented to the channel,the contents of shift register are shifted up one stage as follows: 17 → out,16→ 15, 15→ 14, ……..,1 →2.The first output bit is also placed in shift register stage 1.The next bit sequence data in arrives and the procedure is repeated.

The unscambler operates as follows .The initial contents of the shift register are fixed.When the first bit of input sequence arrives,this bit is summed mod-2 with the mod-2 sum of the initial values os stages 12 and 17. This sum then becomes the first bit of output sequence.At this time instant the contents of the shift register are shifted up one as follows: 17→16, 16→15, 15→14,……, 1→2.The first bit of input sequence of stage II is then put in stage I and the next bit in input sequence is presented to the unscrambler.The procedure is then repeated.

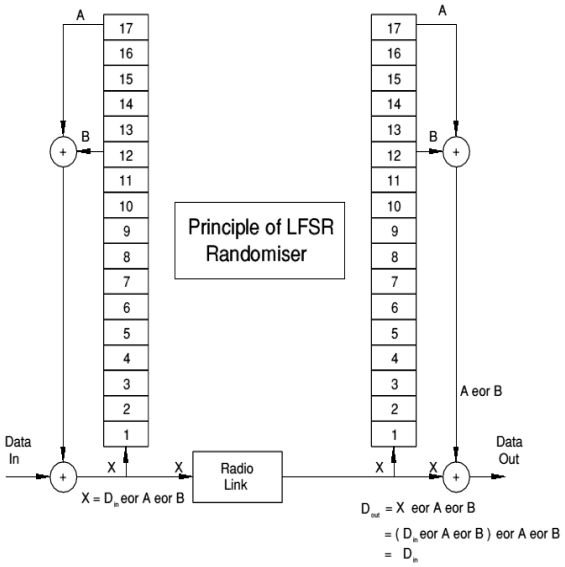

Figure 5: Data scrambler and unscrambler

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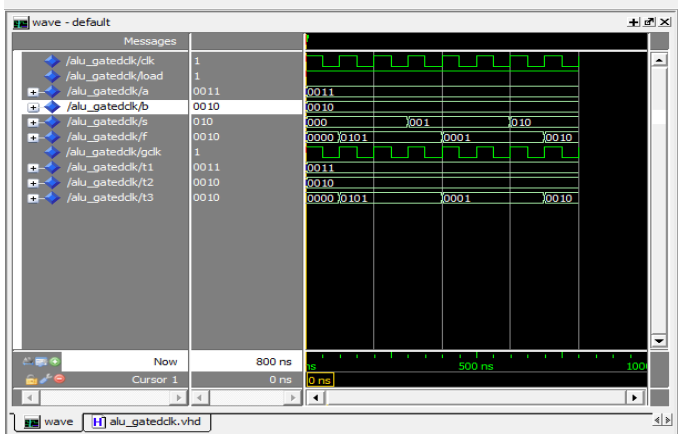
IV. RESULTS

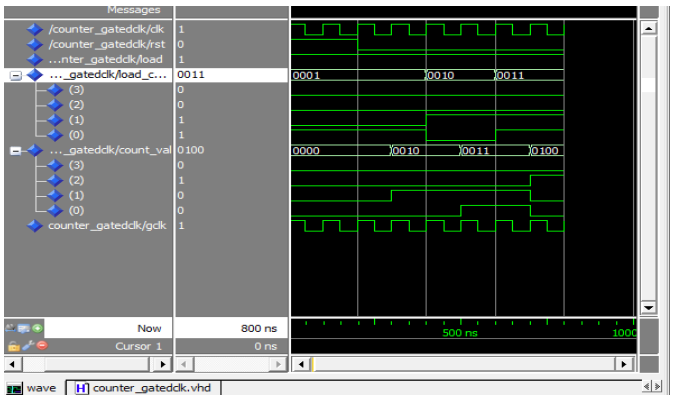
The entire design is captured in VHDL and implemented using Modelsim 6.3f and Quartus II software

A. Simulation Results

The simulation results of various circuits are shown in Figure By applying different input conditions, the outputs are observed Using Modelsim tool.



(a)



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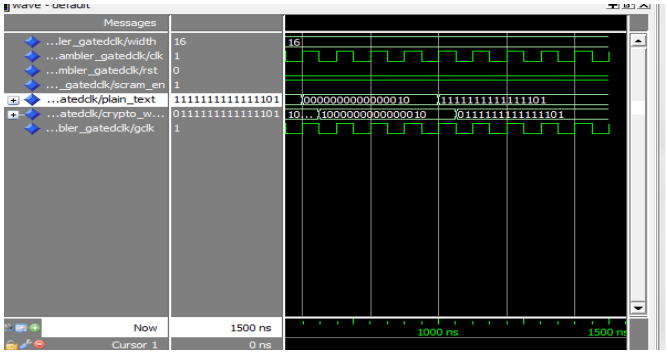
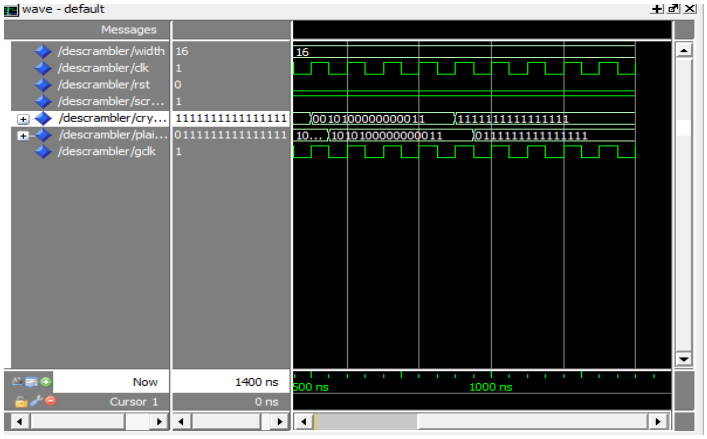


(c)



(d)

Figure 6.:Simulation Results of (a)ALU, (b)Counter, (c)scrambler,(d)descrambler using clock gating.

B. POWER ANALYSIS

Power analysis of ALU,Synchronous counter,scrambler and descrambler with and without using clock gating is given in below Table 2.

Table 2: Power Dissipation of different circuits with and without clock gating

S.No.	Circuits	Power dissipation without clock gating (mw)	Power dissipation with clock gating (mw)
1	ALU	68.71	68.68
2	Synchronous counter	67.98	67.96
3	Scrambler	70.85	70.80
4	Descrambler	70.85	70.80

V. CONCLUSION

In this paper a simple method to reduce dynamic power consumption is introduced. The proposed scheme is based on clock gating technique. And gate based clock gating is used in design example.Experimental result shows that clock gating technique significantly reduces the dynamic power consumption.

In conclusion clock gating technique significantly reduces dynamic power of circuit, but may increase number of logics, and hence area will increase.

VI. ACKNOWLEDGEMENTS

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