A WIRELESS PHYSIOLOGICAL PARAMETER MONITORING SYSTEM

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ABSTRACT

The rapid development in the field of science and technology has turned the twenty first century into a digital book. A book in which everything on everyone is being recorded exists in every field. What we have is a system that can act as a Data Book in the field of diagnosis and treatment of ailments. Here we concentrate on vitals like heart rate, temperature along with movements of a patient. The system is a combination of biosensor technology, system-on-chip design and wireless communication systems. The system when assembled will act as a single node in a in an autonomous body sensor network (BSN). It can act as a powerful tool in well-being monitoring, medical diagnostics, and personal connectivity. For that one has to go for either an FPGA or an SOC which combines all the attributes of a BSN. Here we propose an ARM based physiological parameter monitoring system equipped with physiological sensors, an ARM microcontroller, an RF module and a DAQ card which is correlated to computer system for database. The system is non-invasive in nature and monitors vital parameters such as temperature and heart rate along with the movements (including seizure movements) and keeps a record of parameters mentioned. Microsoft Visual Basic 6.0 is used as front end and Microsoft Office Access as database of the system. Thus it makes the diagnosis and treatments much easier. The system has been tested and found reliable, accurate and also supports physically challenged people.

.General Terms

BSN (Body Sensor Network), BAN(Body Area Network), ARM (Advanced RISC Machine), SOC(System-On-Chip)

Keywords

BAN, nodes,

1. INTRODUCTION

The twenty first century is the fastest one that happened in the human history. Rapid growth and developments were seen in every field of science and technology. And it led to the formation of an enhanced medical field. It is the Integration of wireless, biosensor technologies with an SOC design that results a powerful autonomous Body sensor network (BSN). BSN is also known as Body Area Network (BAN). A Body Area Network (BAN) is defined formally as a system of devices in close proximity to a person's body which is co-operated for the benefit of the user. Body Area Network(BAN) is a number of intelligent physiological sensors integrated into a wearable Body Area Network which can be used for computer assisted rehabilitation or early detection of medical condition.

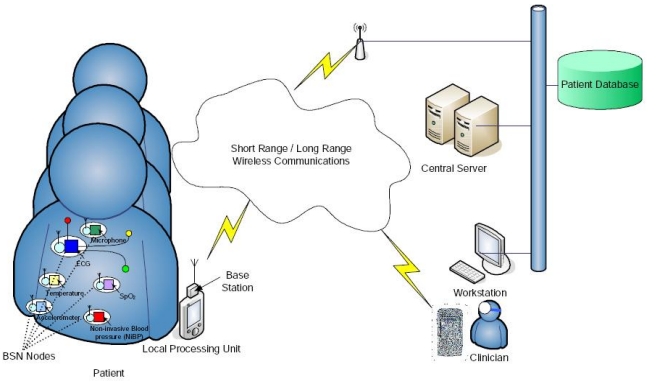

Fig.1.1: Schematic diagram Body Area network

With recent advances in biosensor technology, SOC design, Wireless technologies when applied to an autonomous BSN results a powerful tool in well-being monitoring, medical diagnosis and personal connectivity. Such miniaturized pervasive health monitoring devices have become practically feasible. In addition to providing continuous monitoring and analysis of physiological parameters, the recently proposed Body Sensor Networks (BSN) incorporates context aware sensing for increased sensitivity and specificity. More recent developments have sought to make use of recent technological developments. An SOC which combine many of the functions of the BSN microsystem is widely used for this purpose.

The design of a multifunctional SOC creates many problems increases noise budget considerably. To avoid this physical isolations are provided. This approach reduces the noise content still could do nothing in the case of sensor interfaces. Increased cost of isolations elevates the system expense. The biggest contributor of noise that reaches the analog amplifier inputs is the resonator controlled oscillator within the RF section. It generates 15 mV and 25 mV of noise at 20 MHz and 40 MHz, respectively, as measured at the operational amplifier input nodes. The on-chip RC oscillator operating at 7.1 MHz generates 13 mV of noise as measured at the operational amplifier input nodes and produces lower peak-to-peak noise in the same measurement configurations. For a mixed signal platform, the battery voltage decreases with use which results high average power consumption.

Quite often, the relative large size of these devices significantly limits the performances as well as the pervasive deployments.

1.1 OBJECTIVE

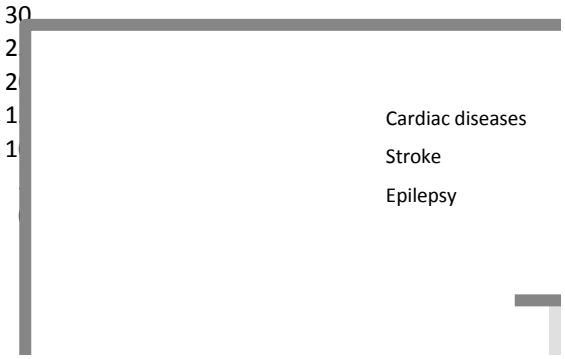

Fig.1.1 Cardiac, Epileptic and stroke cases admitted in from January to May 2015

The chart shows the number of cardiac and neuro patients cases admitted in from January to May 2015 from a reputed medical college. The cardiac disease strictly includes the Cardiac arrest cases alone. The most striking issue is the overlapping in the number of cases. Cardiac issues along with the neural issues are increasing at a large rate. Epileptic cases are on higher rate than that of stroke patients. Here the numbers of cardiac and epileptic cases are in same range. This shows the importance of having an independent system to monitor both the cardiac and neural cases continuously. It shows that the case number in neural case is next to the cardiac cases.

For that a Wireless Physiological Parameter Monitoring System that aims to combine many of the functions of the BSN Microsystems onto a single substrate is proposed. The existing mixed signal platform is replaced by a single ARM7 (Advanced RISC Machine) microcontroller. This result reduced power consumption and noise. Our design is specified for a biosensor system which measures temperature, impact movements, and Heart beat and monitors these parameters using data channels communicating via an encoded wireless interface to a remote base station. The proposed system is implemented in hardware using ARM7 microcontoller, sensors such as temperature, Impact and heart beat sensors, RF communication module, and a central processing station. The above mentioned proposed system is simulated using Proteus7 as simulation tool. Since it's a non-invasive physiological parameter monitoring system there exist no point of infection and similar problems. The system comprises sensor circuits, a microcontroller, an RF transmitter- receiver module and a monitoring base station.

The person is monitored using sensors and data is sent wirelessly from each node to the network. The proposed system acts as a single node in a Body Sensor Network (BSN).

2. LITERATURE REVIEW

The ability to integrate complete sensor systems into a very small form factor is of growing importance in a Body area network. The development of a wireless biomedical sensor interface system-on-chip (SOC) that aims to combine many of the functions of the BSN Microsystems onto a single substrate. The system comprises analog sensor interface circuit, data-conversion circuits, a microcontroller, a data encoder, and a frequency-shift keying (FSK) RF transmitter. Fig 3.1 shows the complete system diagram of the SOC we have developed.

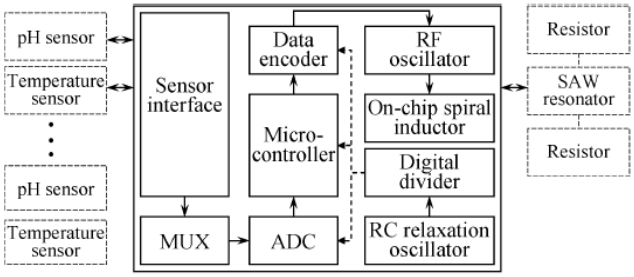

Fig.: 3.1. Schematic diagram of the system-on-chip architecture.

The design flow used to create the SOC was relatively straightforward. The analog-to-digital interface circuitry comprises seven 2-input multiplexers and a 10-b successive approximation analog-to-digital converter (ADC). Power supplies were directly connected as the reference voltages of the ADC. The microcontroller-driven multiplexers allow eight sensor channels to be presented to a single ADC for 0.3 ms each, hence, 2.4 ms is required to sample all eight channels. The RC relaxation oscillator is used to generate the input to the chip timer circuit. The first-order relaxation oscillator was based on charging or discharging an on-chip timing capacitor via a precision current source, which provided a cost-effective solution as well as design simplicity and programmable ability. The oscillation frequency of the relaxation oscillator was proportional to the value of the charging current and was inversely proportional to the value of the timing capacitor. The relaxation oscillator circuit was designated with an operational transconductance amplifier, a comparator, an inverter, the sampling switches and capacitor, and a controlled current source.

The timing precision of the oscillator is poor due to the fabrication tolerance of on-chip resistors and capacitors. The nominal frequency of the RC oscillator is set to be 8 MHz. The timer circuit contains a digital divider designed to generate different clocks for the ADC (250 kHz), the microcontroller (250 kHz), and the data encoder (32 kHz). The clock rates for these blocks are 224 kHz, 224 kHz, and 29 kHz, respectively. The timer can generate the originally intended clock frequencies when it is connected to an oscillator implemented in the RF section of the SOC, but this requires an additional off-chip surface-acoustic-wave (SAW) resonator and two resistors. However, in order to save power, the RF oscillator is not used for timing, but only when wireless transmission is required. In addition to generating the system clocks, the timer also generates a positive pulse (lasting 5 s) every two seconds to start the microcontroller. The microcontroller was designed by us to have the identical instruction set, excluding the multiply (MUL) and WAIT instructions, as a Motorola 6805 CPU. The microcontroller was designed to be fully static and was implemented with 512-B ROM, 32-B RAM(24Bfor buffers and 8 B for stack), three bidirectional 8-b input/output (I/O) ports and a 16-b capture/compare timer system. The software routines, embedded into the 512-B ROM, were used for scheduling different tasks, such as channel cycling, data sampling and

packet forming, and automatically go into a sleep mode when all tasks are finished. However every two seconds, the aforementioned positive pulse generated by the timer invokes a rising-level sensitive interrupt of the microcontroller, and forces the microcontroller to go back to an active mode. This external interrupt design enables dynamic reconfiguration of the system sample rate. All output data are represented as a serial bit-stream packet by the microcontroller. One packet has two identical data episodes with a total of 192 information bits. Each episode begins with eight start bits with a well-defined signature, eight channels (8 b each) of physiological data plus an even parity bit, two 8-b buffer contents (for ID and future expansion) and an 8-b stop sequence. There are 64 '0' b between two consecutive packets.

The microcontroller was programmed for the duration of representing each bit to be 7.81 ms. In practice, it takes 8.7 ms to represent each bit because of the shift of the clock rate from 8 MHz to 7.1 MHz. Therefore, the microcontroller's serial port data rate is approximately 115 b/s. The bitstream signal from the microcontroller is fed into a programmable transmitter for wireless transmission.

The transmitter comprises a data encoder and RF section. The multiplication process is a simple modulo-2 adder that also acts as a phase modulator. The core of the DS-SS transmitter is the pseudorandom noise (PN) code generator. The PN code generator consists of an eight-stage linear feedback shift register (LFSR) and a multiplexer. The PN code length was programmable to provide the appropriate amount of data spreading for a particular application. The transmitter also comprises a memory block for storage of data. In the LFSR implementation, the all 0 state (all 1 state if XNOR is used in the feedback path) is not allowed. In the design, this was prevented by an additional control circuit. This rearrangement also enables the generation of even length PN codes by inserting an additional 0 to give a maximal LFSR sequence. Serial bitstream data to be transmitted are coded by either the PN code if the bit is logic 0 or a 180 phase-shifted version of the PN code if the bit is logic 1. This coding is performed automatically by the EXOR operation.. The minimum data rate from the encoder is approximately 3.67 kb/s, which is 32 times the microcontroller's serial port data rate (115 b/s). The integrated RF section on the SOC could be activated.

The amplification stage of the RF session was elaborated to be a near-class-E RF power amplifier that was driven by the encoder's digital output. A two-stage driving amplifier was utilized. The gain budget of this amplifier was carefully asserted to maintain high gain and linearity while limiting the total current. The amount of amplitude and bandwidth extensions was optimized for this design in order to minimize data jitter. In the output stage, the back-termination polysilicon resistors were used to reduce reflections from output ports. A relatively low carrier frequency was selected for the on-chip RF section. The carrier frequency signal was generated directly by using an oscillator with an external SAW resonator, rather than by having a low-frequency oscillator multiplied up to the desired frequency. For exploratory purposes, the RF section had two resonator controlled oscillators, each with a frequency-shift keying (FSK) modulator and an output stage. One was a Pierce circuit and the other was a Colpitts oscillator. To achieve low phase noise, only one active transistor was used in the core circuits. Negative resistance was created by using the RF-NMOS transistor in the common source configuration for the Pierce oscillator and the common gate configuration for Colpitts oscillator. The SAW resonator was used as a frequency determination element between the drain and the gate of the NMOS transistor for the Pierce oscillator, and the source and the gate for Colpitts oscillator, respectively. A variable capacitor in series with the SAW resonator was used to generate FSK modulation. The main advantage of using the SAW resonator was relatively high quality factor and relative low power consumptions.

3. PROBLEM FORMULATION

An on-chip spiral inductor incorporated on the SOC can be used. The radiated signal from the inductor was detectable at a range of 0.5 m in air using a Winradio receiver with a conventional whip antenna at a data rate of up to 5 kb/s. Therefore, the encoder data rate is always set to be 3.67 kb/s. The signal from the SOC is detected by a data-acquisition (DAQ) device. Since the DAQ terminal uses a correlator implemented on a PC in software, the synchronization requirement between the SOC and the terminal was significantly reduced. The correlator will yield a positive peak at 0 phase, and a negative peak at 180 phase. Data can be simply recovered by thresholding the correlator output.The design of a multifunctional SOC creates many problems such as

A. Increased Noise Budget: The presence of individual components contributes the overall noise budget. The biggest contributor of noise that reaches the analog amplifier inputs is the resonator controlled oscillator within the RF section. It generates 15 mV and 25 mV of noise at 20 MHz and 40 MHz, respectively, as measured at the operational amplifier input nodes. The on-chip RC oscillator operating at 7.1 MHz generates 13 mV of noise as measured at the operational amplifier input nodes and produces lower peak-to-peak noise in the same measurement configurations. The total noise measured on an output pin from the analog circuit [before the analog-to-digital converter (ADC)] of the SOC, when powered by two batteries, is equal to 15 mVrms. In order to minimize the off chip component count, hence, the overall packaged system size, an on-chip RC relaxation oscillator is used to generate the input to the chip timer circuit.

B. Power Consumption: The battery voltage decreases with use and the average current consumption of the SOC for different battery voltages is measured. The largest power consumption is from the sensor interfaces and RF sections, which are 1.9 mA at 3 V and 1.7 mA at 3 V, respectively. With the on-chip RF section activated, the maximum measured power consumption for new batteries was 18 mW, decaying to 8 mW for batteries approaching the end of their lifetime. No significant perform deteriorations were affected by decreasing battery levels within the battery operation ranges.

C. Increased cost for physical isolations: The limiting factor on noise is on-chip substrate noise due to clock transmission rather than thermal or shot-noise sources in the sensor architecture. Therefore a great consideration is given to the chip-assembly and routing in order to minimize on-chip coupling as far as possible using conventional layout techniques. The SOC was designed to minimize the propagation of noise from the noisy 40-Hz RF oscillator (with the on-chip RF oscillator activated) to the noise-sensitive sensor interface circuitry, and particularly to the operational amplifier input nodes. These circuits were physically isolated on the silicon die, their power supplies were separated inside

the chip, and additional substrate noise barriers (guard rings) were placed around them. Moreover, the core and padring power supplies were also separated inside the chip, and the pad ring was split into analog, digital, and RF sections to inhibit noise from propagating through the power lines. Finally, approximately 20 pF of power-supply decoupling capacitance was distributed between different rails resulting an increased cost of production.

3.1 System Model

Recent years have seen the rapid development of biosensor technology, system-on-chip design, wireless technology and ubiquitous computing. When assembled into an autonomous body sensor network (BSN), the technologies become powerful tools in well-being monitoring, medical diagnostics, and personal connectivity. In this paper, we describe the first demonstration
of a fully customized mixed-signal silicon chip that has most of the attributes required for use in a wearable or implantable BSN. Our intellectual-property blocks include low-power analog
sensor interface for temperature, heart beat and impact monitoring, a data multiplexing and conversion module, a digital platform based around an 8-b microcontroller, data encoding for spread-spectrum wireless transmission, and a RF section requiring very few off-chip components. The chip has been fully evaluated and tested by connection to external sensors, and it satisfied typical system requirements.

3.1.1. WIRELESS SENSOR INTERFACE SYSTEM ON CHIP

The complete system diagram of the SOC has been developed. The design flow used to create the SOC was relatively straightforward.

Sensor Interfaces

The SOC operates with external temperature sensors. The external temperature sensor is a forward biased pn junction with a junction area of 0.6 mm. The interface circuit is a conventional structure that connects the diode in feedback across an operational amplifier with a constant bias current. An on-chip bias resistor sets the constant current to be approximately 15 A. The reverse bias saturation current of the diode is 30 pA and the ideality factor is approximately 2; therefore, the device sensitivity 22 C, but does vary from device to device due to tolerances.

The external pH-ISFET sensor forms the load of a 33- A cascade current sink. The ISFET is similar to a MOSFET device where the gate metal was replaced by a reference electrode immersed. The ISFET has an intrinsic gate referred sensitivity of a 43-mV/pH point. For circuit implementation, the cascade structure of the current source allowed a high impedance to be obtained, which reduced the variations of the drain-source current due to the fabrication, temperature, and power-supply variations. The output transistors of the cascade circuit form an active load to the ISFET that is configured as a source follower; thus, the voltage swing at the source of the ISFET responds at the 43-mV/pH point.

3.1.2. Mixed-Signal System Platform

The systems-on-chip (SoC) concept has been quite successful, particularly in the digital arena. Hundreds of designs combining numerous processors, configurable and dedicated accelerators, I/O interfaces, and on-chip networks have been designed, fabricated, and brought to market. Reduction of overall system cost, chip size, and power together with performance increase have been the main driving force behind this continuing integration of functionality onto a single die. Yet, true SoC integration requires not only the inclusion of the digital computing,
but also a seamless integration of the mixed-signal (MS) processing that embodies the periphery to the outside world and the environment. Some very complex and sophisticated mixed-signal SoCs have been designed and manufactured over the past few years. This is true in the domain of wireless and/or wireline communications, where cost considerations have led to the combination of high-frequency RF components, high-performance analog and complex digital functionality. Besides cost reductions, SoC integration has led to some additional rewards for example, lower jitter and phase noise is attainable by not having to go off chip, and large power savings can be achieved by eliminating two low-voltage differential signaling (LVDSV an interconnect standard) interfaces for high-performance analog–digital converters (ADCs), to name some. Yet, each of these mixed-signal SoCs is typically the result of a painstakingly executed and time-consuming custom design process. Most MS modules are still custom designed using tool flows that are only modestly more advanced than the ones we used over the last decades. Reuse of modules, design exploration, and the adoption of higher abstraction levels, going beyond logic synthesis techniques that have been proven to be so effective in the digital world have made little inroad. Analog building blocks are still dropped into the SoCs as hard macros, and integration of analog modules is limited to medium-performance hard-wired blocks with frozen layouts.

4. PROPOSED SYSTEM

The need of a continuous Healthcare and Wellbeing Monitoring system in the field of Body Area network is increasing daily for which, we use a multifunctional SOC which combines most of the attributes of a BAN. To overcome the above mentioned drawbacks of this existing system, we propose a new Wireless Physiological Parameter monitoring system combining the features of a BSN with an Advanced RISC Machine (ARM) microcontroller, sensors, and communication modules

4.1. SYSTEM DESIGN

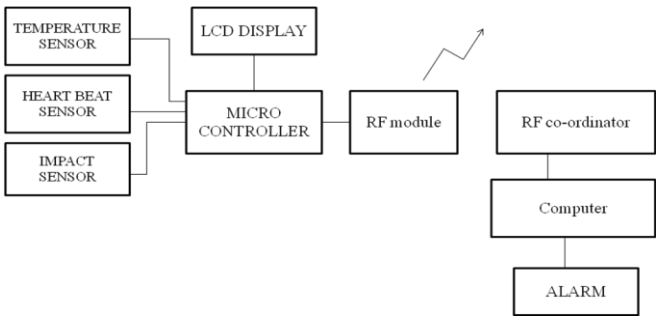

Fig.: 4.1. Proposed system block diagram

The proposed system acts as a single node in a BSN. Each patient is considered as each node in a BAN and is continuously monitored using the sensors. Vital Physiological parameters like temperature, heart beat and impact movements are continuously monitored. This data can be fed into a database system for each patient for further

observations and study. Any abnormalities in the vitals are detected at once and further actions are taken. The system is a non-invasive wearable physiological parameters monitoring system that can be used for physically challenged people. The heart beat is monitored using a pulse oximeter which gives a digital data about the heart beat for a minute. The temperature is monitored using an integrated temperature sensor which gives an analog output voltage. The impact movements are measured in 3-dimensional axis using an accelerometer which detects the static and dynamic acceleration. The accelerometer gives a digital output which varies its duty cycle depending upon the positional movements of the subject under observation. The output voltages of the three sensors are given into the input of ARM7 microcontroller. The received data is converted into ASCII characters and is send to the main processing unit with the help of an RF module as shown in the diagram. The low power, low cost RF module transmits the received data from the microcontroller to the base station system were the data is displayed, monitored and stored in data base for each patient nodes. The replacement of mixed signal platform with a single ARM microcontroller will reduce the noise content considerably. Thus this elevates the system performance. The low power performance of the microcontroller leads to improved energy consumption. The system can work in 3v and 5v input supply. The process of replacing SOC with a single microcontroller gives a more compact system which is less bulky than the original system. The designed system comprises sensor circuits, a microcontroller, an RF transmitter- receiver module and a monitoring base station. The output from the sensor interfaces are processed and send to the remote central station by the microcontroller using an RF communication module. The continuously receiving signals are monitored by the base station and in the case of any abnormalities, further alarm is sounded and medical aid is provided. In short the proposed system is a biosensor system which measures temperature, impact movements, and Heart beat and monitors these parameters using data channels communicating via an encoded wireless interface to a remote base station

The data received from the patient is displayed in the VB front end designed. No matter whatever the incoming data is, it is being recorded into the individual database Microsoft Access database based on the patient id in the received data. In the case of abnormalities, the front end will display message boxes which with only answering will disappear. In case of parameter value change from the given threshold value front end will keep on giving message boxes showing abnormalities. Everything along with date and time are recorded in the database for further study. This in turn can act as a real time case sheet for the subject under observation

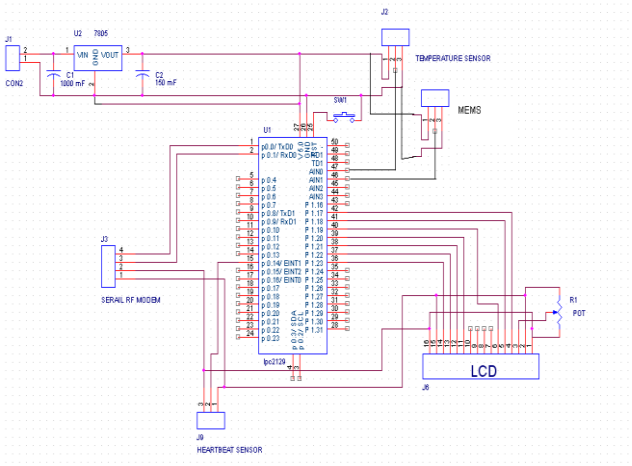

Fig.4.2. Circuit diagram

The complete circuit diagram of wireless physiological parameter monitoring system is shown below The circuit consists of power supply section, three sensor interfacing sections, an LCD interfacing section and a RF modem interfacing section. The CC2500 is used in RF section which is a low-cost 2.4 GHz transceiver designed for very low-power wireless applications. LPC2129 microcontroller has 3 VDD pins (23 & 43 & 54) for 3.3v supply and 5 VSS pins (6,18,25,42 & 50) for ground. 57TH pin is RESETpin , when this pin is grounded or active low LPC2129 get reset. So for making IC in working mode, P1.26 pin is pulled DOWN through resister 10K. For working , a 10MHZ crystal is used. The capacitors c14 & c15 connected to the crystal is the stabilizing capacitors which stabilizes oscillations from the crystal.

The power supply section consists of a 7805 IC which is used as voltage regulator. It gives power of regulated 5v to the microcontroller section and sensors. The power supply is given to Vss and GND pins of the microcontroller. A switch attached to it acts as a RESET pin. Serial Communication port is connected to port0.0 and port0.1 pins tor data reception and transmission. The port R1 attached to the LCD helps to vary its brightness. The entire circuit is done in the common board of ARM microcontroller. The sensor inputs are fed into the microcontroller and then to the LCD display. The data out from the controller is fed into the Serial RF modem input. The ARM microcontroller is placed on a header circuit which consists of a crystal oscillator and an extra power supply unit which produces a 3.3V from the given 5V supply to the microcontroller alone. Two zener diodes are place in the hardware section to the controller to make the IS pins high. Additional to that an rs232 is added to the header board for connection to the computer system. Normally in TTL logic 0 is 0v and logic 1 is +5V but when connected to lap for burning purpose this voltage level changes such that logic 1 is taken as voltage between +3 to +24V and logic 0 as -3 to -24 V. To meet this issue four clamped capacitors are used in the common board. The RF module is connected vertically to the board. It consists of a transceiver. The sensors used are Heart beat sensor model 1157 for measuring heart rate, Acceleration/vibration/tilt sensor – 3 axis and an LM35 IC for temperature measurements. LM35 is used with single power supplies, or with plus and minus supplies. Accelerometer sensor can measure static(earth gravity) or dynamic acceleration in all three axis.

5. EVALUATION AND PERFORMANCE

Completed the literature survey, proposed a new Physiological parameter monitoring system and that was tested OK. The system appears to be an efficient patient monitoring system in hospitals, rehabilitation centers and also among aged people since it is a non-invasive physiological parameter monitoring system. The system was found to be working as per the design and was found to be reliable as well as accurate. Integration of wireless, biosensor technologies with SOC design results powerful tools in an autonomous Body sensor network (BSN). The wireless physiological parameter monitoring system successfully functions as a node in a WBAN/WBSN.

6. ACKNOWLEDGMENTS

We would like to thank Nehru College Of Engineering And Research Center, Pampady for providing the technical support.

7. CONCLUSION

Conducted a detailed study on existing system, proposed system design and identified the tools and components needed in the software and hardware implementation. Both hardware and software implementations were done successfully. The system was tested and found accurate and reliable. Thus the design and implementation was successfully completed.

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[7] **Jan M. Rabaey, Fellow IEEE, Fernando De Bernardinis, Ali M. Niknejad, Borivoje Nikolic´, Senior Member IEEE, and Alberto Sangiovanni-Vincentelli, Fellow IEEE** Embedding Mixed-Signal Design in Systems-on-Chip Innovative approaches and new design methodologies are needed to integrate digital, analog and RF components in CMOS systems-on-a-chip smaller than 100 nm.

