

Implementation and Design of Low Power Carry Select Adder using Different Technologies

Rajwinder Kaur, Amit Grover

Abstract— Carry select adder is one of the key hardware block in most of arithmetic logic unit and arithmetic logic is the essential unit of the microprocessors, DSPs and FIR filters etc. In the world of technology it has become necessary to develop several innovative design approaches to decrease the area and power consumption. In this paper TG has been used to develop the proposed 64-bits CSA using AND, XOR and OR gates. The main objective of this paper is to design a new CSA which gives better results in terms of delay and power dissipation than the conventional CSA designs. The proposed 64-bits CSA has been designed using 45nm, 90nm and 180nm CMOS technologies and we use TANNER tool version 7 for circuit implementation. The developed adder has shown the improvement in delay and average power consumption in order to implement CSA adder proficiently in digital signal processors.

Index Terms— Carry select adder(CSA), Ripple Carry Adder (RCA), Transmission Gate (TG), Low Power design.

I. INTRODUCTION

The most important area of research in VLSI system design is to design the high speed digital adders having effective area, delay and power. Addition is indeed the most fundamental arithmetic operation in digital circuits. The speed of addition in digital adder circuits is limited by the time mandatory for a carry to propagate through the adder [1]. So to solve the problem of carry propagation the CSA is used in several arithmetic logic systems, digital signal processing systems like FIR filters by independently creating the multiple carries and then chooses an accurate carry to create the final sum [4],[7]. CSA provides the comparisons between RCA and CLA adder where RCA is area efficient and simple and having slow speed and CLA provides fast speed but it consumes large area [2]. But CSA having high speed and occupied less area than CLA. Conventionally, CSA is implemented with dual ripple carry adder with carry in of 0 and 1 correspondingly depending on the configuration of block length [13]. CSA is furthermore classified as either linear or square root.

This paper represents CSA having less delay and low power consumption than the conventional CSAs. The related circuit is made up of NMOS and PMOS transistors using TG technology having simple structure than that proposed in other CSAs. The transmission gate comprises of n-channel transistor as well as p-channel transistor with distinct gate connections, common source and drain connection. The control signal is applied to a gate of n-channel transistor and its complement is applied to the gate of p-channel transistor. By combining the characteristics of p-channel and n-channel

transistors, it is able to pass logic 1 and logic 0 efficiently without any distortion.

To design a low power and high speed circuits can be addressed at various levels like algorithm layout, architecture, process technology and circuit levels.

There are three types of power that is:

- 1) Static power consumption
- 2) Dynamic power consumption
- 3) Short circuit power dissipation

Static power is associated with leakage current and can be improved with the advancement of fabrication technology. Static power consumption is that which mainly affect a system at rest.

$$P_s = I_{\text{leakage}} V_{dd}$$

The dynamic power consumption is that which affects a system in active mode. Dynamic power is attributed by two causes:

1. Load capacitance charging discharging
2. Short circuit

$$P_{\text{total}} = P_{\text{switching}} + P_{\text{short-circuit}} + P_{\text{leakage}} \\ = (\alpha_{0 \rightarrow 1} \times C_L \times V_{dd}^2 \times f_{\text{clk}}) + (I_{sc} V_{dd}) + (I_{\text{leakage}} V_{dd})$$

The term $(\alpha_{0 \rightarrow 1} \times C_L \times V_{dd}^2 \times f_{\text{clk}})$ indicates the power consumed by the capacitor charging discharging during circuit switching where C is load capacitance, $\alpha_{0 \rightarrow 1}$ is node transition and f_{clk} represents the frequency of the clock. The $(I_{sc} V_{dd})$ term is short circuit power dissipation. It arises when direct current flows from V_{dd} to G_{nd} , it depends on rise time, full time because it is only during transition that transistor between V_{dd} and G_{nd} remains on and Short circuit power dissipation comes into play. The term $(I_{\text{leakage}} V_{dd})$ indicates the static power when the circuit is at rest. Basically the static power is zero but due to the leakage current there is little bit static power is available. Thus the voltage which supplied is the effectual way to decrease the three types of power. Such reduction necessitates innovative design approaches for low power and less voltage ICs [5],[14].

In 2012, Ramkumar and Kittur are suggested a CSA which uses a simple and effective gate level modification to significantly decrease the area and power of the CSA [10]. In 2012, I.C. Wey, C.C. Ho, C.C. Pong and Y.S. Lin are suggested an area proficient CSA by sharing the common Boolean logic term to achieve the lower area, less power consumption and power product delay [6]. In 2014, Basant Kumar Mohanty suggested a new CSA which was presented by the logic operations involved in conventional CSA and binary to excess-1 convertor based CSA are analyzed to study the data dependence and to identify the redundant logic operations [12].

This paper is systematized as follows. The section I describes the introduction. In section II, there is carry select adder is defined. In section III, there is the description of

design style. In section IV, final result is shown. In section V conclusion is summarized. In section VI future scope is described.

II. CARRY SELECT ADDER

Carry Select Adders (CSAs) have been considered as a compromise solution between RCAs and CLAs ($O(n)$ time and $O(2n)$ area) because they offer a good trade-off between the compact area of RCAs and the short delay of CLAs [3]. The carry select adder comes in the category of conditional sum adder. Conditional sum adder works on some condition. Sum and carry are calculated by assuming input carry as 1 and 0 prior the input carry comes [4]. When actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer. The CSA is used in many systems to overcome the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. But the CSA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input $c_{in} = 0$ and $c_{in} = 1$, then the multiplexers are used to get final sum and carry are used [8].

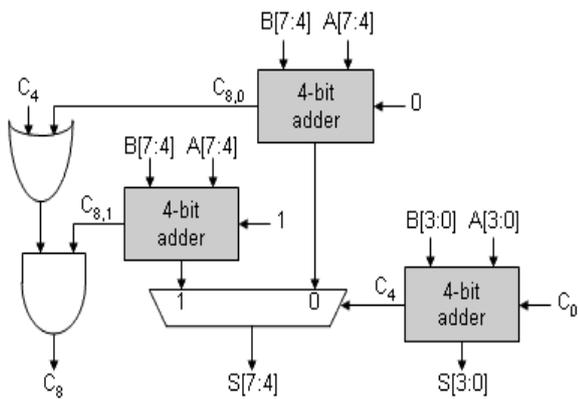


Fig.1: 8-bit CSA with multiplexer unit

III. DESIGN STYLE

The 64-bits CSA is made by 1920 transistors by using the transmission gate (TG) design style. In this circuit design, the simulation is run by 45nm, 90nm and 180nm technologies at different gate width of NMOS and PMOS transistors. The minimum length used for both transistors is $0.18\mu\text{m}$ and power supply used to run the circuit is 1.7v. With the help of below 1-bit CSA circuit, 64-bits CSA is developed.

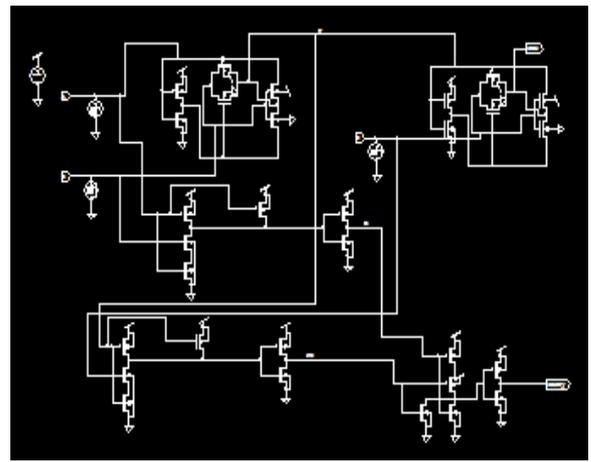


Fig.2: Circuit diagram of 1-bit CSA using TG technology

The proposed carry select adder design uses a XOR gate, two AND gates and one OR gate. The schematic diagram for that gates are respectively shown below.

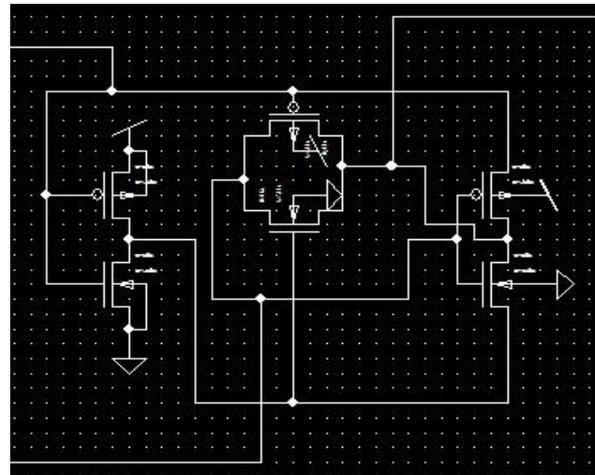


Fig.3: XOR Gate

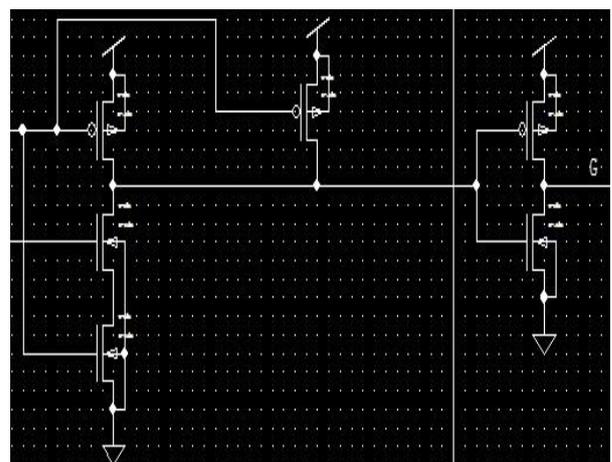


Fig.4: AND Gate

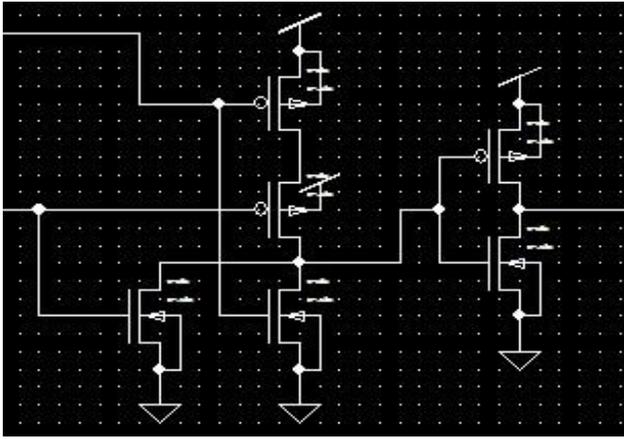


Fig.5: OR Gate

IV. FINAL RESULT

The performance parameters of 64-bits CSA as given below:-
The below tables shown the results of 64-bits Carry select adder using 45nm, 90nm and 180nm technologies are carried at different gate widths.

TABLE I

Design Style	No. of transistors	Supply Voltage (V)	Minimum Length (µm)	Width of NMOS(µm)	Width of PMOS (µm)	Avg. Power Consum. (watts)	Prop. Delay at carry(sec)
CSA	1920	1.7	0.18	0.64	1.7	1.094x10 ⁻³	1.2378x10 ⁻⁹
CSA	1920	1.7	0.18	1.28	3.4	1.139x10 ⁻³	6.845x10 ⁻¹⁰
CSA	1920	1.7	0.18	2.56	6.8	1.232x10 ⁻³	3.6207x10 ⁻¹⁰

Table.1. Specifications of 64 Bits CSA adder at 45 nm technology

TABLE II

Design Style	No. of transistors	Supply Voltage (V)	Minimum Length (µm)	Width of NMOS(µm)	Width of PMOS (µm)	Avg. Power Consum. (watts)	Prop. Delay at carry(sec)
CSA	30	1.7	0.18	0.64	1.7	1.118x10 ⁻⁵	1.2465x10 ⁻⁹
CSA	30	1.7	0.18	1.28	3.4	9.056x10 ⁻³	6.227x10 ⁻¹⁰
CSA	30	1.7	0.18	2.56	6.8	9.883x10 ⁻³	3.478x10 ⁻¹⁰

Table.2. Specifications of 64 Bits CSA adder at 90 nm technology

TABLE III

Design Style	No. of transistors	Supply Voltage (V)	Minimum Length (µm)	Width of NMOS(µm)	Width of PMOS (µm)	Avg. Power Consum. (watts)	Prop. Delay at carry(sec)
CSA	1920	1.7	0.18	0.64	1.7	1.316x10 ⁻³	1.147x10 ⁻⁹
CSA	1920	1.7	0.18	1.28	3.4	1.411x10 ⁻³	6.5099x10 ⁻¹⁰
CSA	1920	1.7	0.18	2.56	6.8	1.572x10 ⁻³	3.6029x10 ⁻¹⁰

Table.3. Specifications of 64 Bits CSA adder at 180 nm technology

V. CONCLUSION

The TG is an effective and widely recognized design methodology to construct CSA adders. In this paper, CSA has been compared using 45nm, 90nm and 180nm technologies. It is concluded that, the results are calculated with different widths of NMOS & PMOS. By doing this, a proficient design is achieved for the CSA. This CSA design includes less delay, area and less power consumes than in recent times proposed CSAs designs. The suggested design technique has been applied for the implementation of 64-bit CSA adder and simulation results verified its proficiency. From the above tables it is conclude that when width of NMOS is 0.64µm & width of PMOS is 1.7µm then CSA consume less power and lesser delay and when width of NMOS is 1.28 µm, 2.56µm and width of PMOS is 3.4 µm, 6.8µm then CSA consume more power and more delay.

VI. FUTURE SCOPE

The TG based advanced CSA circuit decreases the transistor count, power consumption and carry delay of the circuit. The work of this project may be extended to higher bits of adders and to modification the technology file. The research steps may be taken further to optimize the parameters like using the length, frequency, capacitance and width etc. The area and delay of the adders may be decreased as the numbers of bits increases simultaneously.

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