Demystifying the Inward FPGA Communication Stack of USRP

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***Abstract*—USRP (Universal Software Radio Peripheral) is a modest and adaptable radio that turns a PC into wireless prototyping platform. USRP is widely used as RF transceiver, cognitive radio application, physical layer prototyping etc. USRP is a hardware used for digitizing the incoming RF signal and transmitting the RF version of data generated by the computer. USRP provides a gigabit Ethernet interface between the host PC and the high speed ADC-DAC as well as the FPGA (Field Programmable Gate Array). This paper provides a complete overview of internal component of the FPGA. The FPGA is the main signal processing platform for the RF signal of the USRP. The primary role of the FPGA is to provide interface between the ADC and DAC and the gigabit Ethernet. FPGA consists of the DUC (Digital Up Conversion)-DDC (Digital Down Conversion) unit used for frequency up-down conversion of the RF signal.**

***Keywords*—USRP, VRT (VITA Radio Transport), DUC-DDC, CIC(Cascaded Integrator Comb) Filter.**

I. INTRODUCTION

USRP is an open source device used for various wireless communication applications. It is the cheapest and easiest mode for implementing a system on a single platform [1]. It is also a flexible platform and can be used for real time application. It is a bridge between the software world and the RF world. The USRP and on-board FPGA provide engineers and developers a method for prototyping the wireless communication systems such as satellite channels/links.

The FPGA in USRP performs the high bandwidth computation and provides a sampling rate compatible with transfer rate over the gigabit Ethernet. The main function of the FPGA in USRP is to interface the daughter board (ADC-DAC) to the Ethernet. To do this FPGA logic implements transmit and receive digital signal processing paths, an Ethernet Media Access Control (MAC), a microprocessor to control the Ethernet MAC and a large memory to transfer data between various components.

The USRP is connected to the PC via a Gigabit Ethernet cable, which provides high speed data transfers. The received data is processed by the FPGA and passed to the host PC. DSP Block of the FPGA is used for signal filtering and processing. The received signal after processing by the FPGA is passed to daughterboard having DAC and ADC, which convert the digital signal to analog and vice-versa.

RF front end module has TX and RX antenna which respectively transmit and receive the signal of USRP. RF signal input and output terminals are used RX and TX which have SMA connectors of impedance 50Ω and configured as single ended channel [2].

The paper is structured as follows. Section II of this paper provides the details of the system; Section III contains the internal components of the FPGA; Section IV-VIII provides the details of each component of FPGA followed by conclusions.

II. OVERVIEW

A. USRP

The main advantage of using USRP is its ability to interface the software with the hardware in real time. The general architecture of the USRP consists of an RF front end panel, Motherboard and a Daughterboard. There are various daughterboard's which can interface with USRP having frequency range from DC to GHz. It works as a digital baseband and IF (Intermediate Frequency) section of a radio communication system. The introductory design ideology behind the USRP has been doing all signals processing like modulation and demodulation on the host PC. The FPGA performs all the high speed operations such as frequency up down shifting etc. The basic block diagram of USRP is shown in Fig.1 [3].

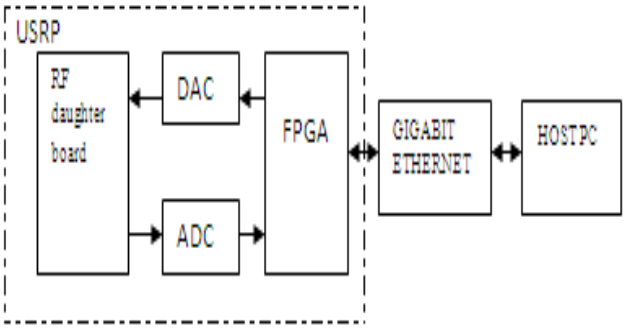


Fig.1. USRP and Host PC

B. USRP FPGA

FPGA is a large resource of logic blocks and RAM blocks which provide high speed digital computation [4]. Real time application system can be implemented using FPGA. USRP contains an on-board FPGA, which provides all signals filtering of the RF signal. FPGA consists of reconfigurable

logic elements and switch matrix to route signal between them.

III. INTERNAL COMPONENTS OF USRP FPGA

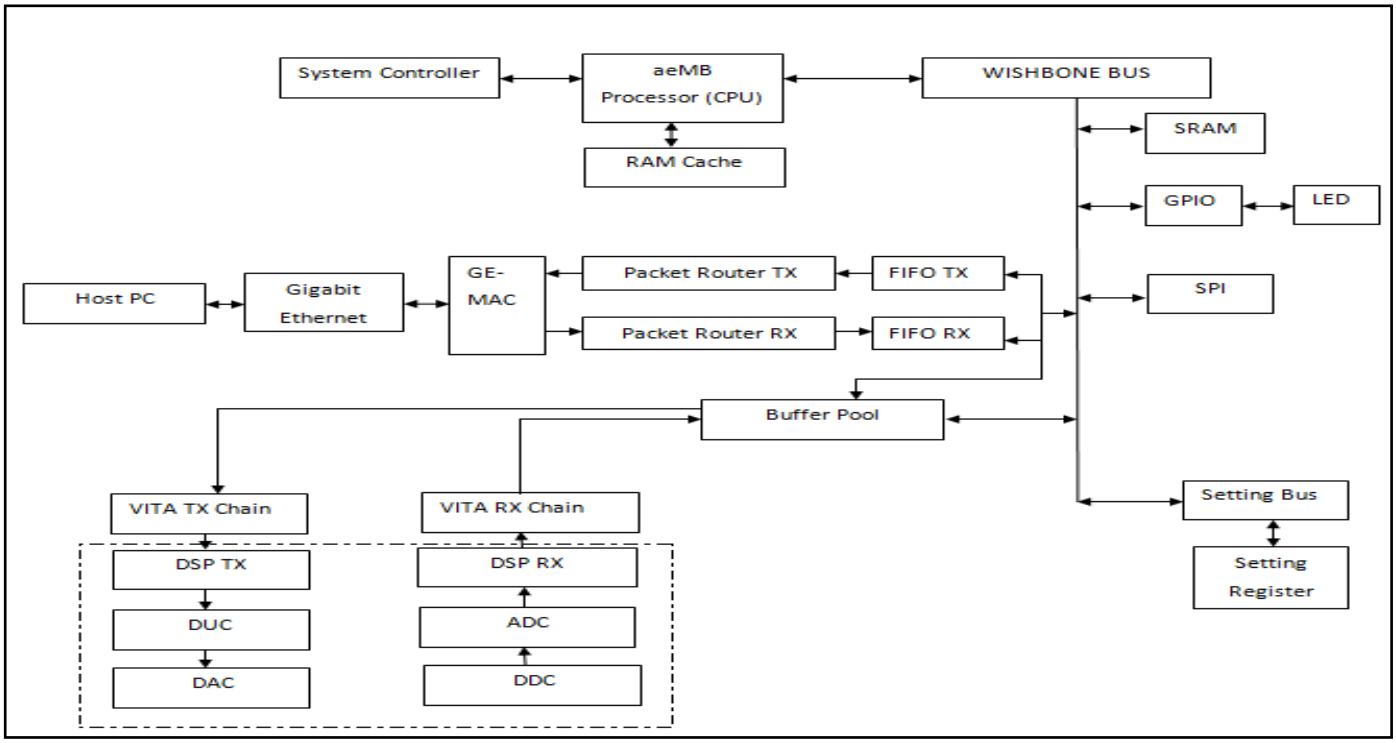


Fig.2 Internal Components of USRP FPGA

The FPGA of the USRP can be divided into various communication layer stacks. The block diagram containing the internal components of the FPGA is shown in Fig.2. Various components of the FPGA are Gigabit Ethernet at the physical layer interface, followed by the MAC layer having GEMAC, a packet router at the network layer, VITA protocol in the Transport layer and DSP chain at the application layer. The received RF signal from the RF front end panel is passed to the MAC layer through Gigabit Ethernet.

In the MAC layer, the MAC address of the data is removed and the packet is passed to the network layer for routing. The packet router at the network layer removes its IP address and routes the packet to CPU, DSP chain and to the external controller. FPGA consists of an aeMB processor having a wishbone bus interface for controlling. All signal and packet handling is carried out by the CPU.

The external component interface to FPGA such as LED is done through the GPIO (General Purpose Input/output). The status of all 6 LEDs provides the information about transmitting, receiving, firmware and CPLD loaded, reference clock and MIMO (Multiple Input Multiple Output) cable line status. The Daughterboard is connected to the FPGA through the SPI (Serial Peripheral Interface). The FPGA has an inbuilt SRAM for the data storage. External memory module may be connected to the USRP supporting up to 1GB memory. The soft-core processor of USRP FPGA has a wishbone bus interface to fetch the data from the memory. Quick access of memory is possible without any delay to simultaneous data fetching from the memory through a wishbone bus interface.

DSP chain of the FPGA performs all the signal filtering and processing in digital and analog domains. It consists of a DUC-DDC unit of the frequency up-down conversion of the RF signal. The frequency shifted signal is passed to the daughterboard having DAC-ADC unit.

IV. DSP UNIT OF USRP FPGA

DSP unit of the FPGA in divided into transmit and receive path. The transmit path carries out the three tasks: 1)provides for proper mount of outgoing data, 2) mixes the signal to an IF and, 3) provides the necessary interpolation to run the DAC at the system clock frequency [5]. The receiver path provides the necessary decimation rate to run the ADC.

A. Transmit Path

Transmit path of the FPGA DSP unit shown in Fig.3 gets the data from the VITA chain at the transport layer which is up converted by the DUC chain. The data received is a 32 bit value which is stored in the buffer module. This module decouples the data to be transmitted into I (In phase) and Q (Quadrature) signals. The upper 16 bits represent Q data and lower 16 bits represent I data. Then each complex signal is interpolated by the different cos and sine signal. This interpolated signal is then up converted in the DUC unit of the

FPGA. The DAC unit transmits it by converting the signal into analog form.

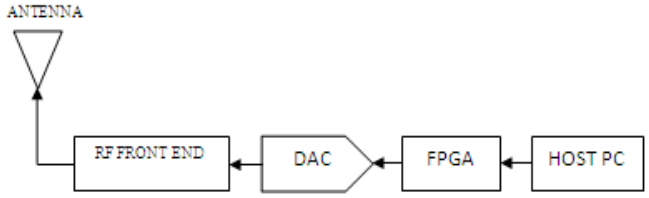


Fig.3 USRP Transmit path

B. Receive path

The received signal from the daughter board is first converted to a 12 bits value which the resolution of the DAC. The signal, then interfaces with the DUC module which routes them to a proper digital down converter. Then the RX chain module in FPGA takes care of digital down conversion to baseband and decimation. And finally, the signals go through the RX buffer module, where they get interleaved into 16 bits values by adding extra 4 bits. That value is sent to the PC through Ethernet cable. Fig.4 shows the USRP receive path.

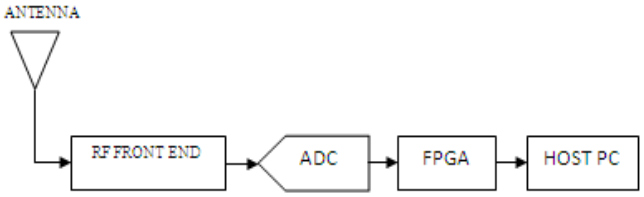


Fig.4 USRP Receive path

C. Digital Converters

Digital converters are the fundamental part of the communication system. They are used for frequency translation of the RF signal. Digital up converter are required when frequency is to up sampled whereas digital down converter are used when the frequency is to be down sampled.

1. DUC

Digital up conversion consist of two steps:

- Up sampling
- Frequency shifting

Block diagram of digital up converter is shown in the Fig:5

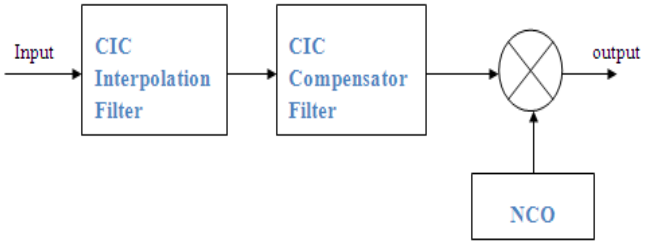


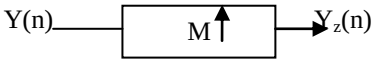
Fig:5 Block diagram of DUC

Interpolation include insertion of zero ,where for the given sequence Y(n) inserting (M-1) zero-values samples result in a sequence $Y_z(n)$ given by

$$Y_z(n) = \begin{cases} Y\left(\frac{n}{M}\right) & if\ n = integer\ multiple\ of\ M \end{cases}$$

$$Y_z(e^{jw}) = \sum_{n=-\infty}^{\infty} Y\left(\frac{n}{M}\right) e^{-j\omega}$$

$$Y_z(e^{jw}) = Y(e^{j(M\omega)})$$



CIC interpolation filter are used fo the up sampling of the input signal. Disadvanatge of CIC filter is it does not have flat passband response. Thus CIC compensartor filter is used having inverse frequency response then the CIC filter.The up sampled signal is multiplied with carrier frequency genearted by the NCO (Numerically Controlled Oscillator) based on DDS(Direct Digital Synthesizer). The final output signal is the up converted signal.

2. DDC

DDC is used for frequency down conversion in the receiver side of the communication filter.DDC process consist of two steps:

- Down sampling
- Frequency down shifting

Block diagram of DDC is shown in the Fig:6

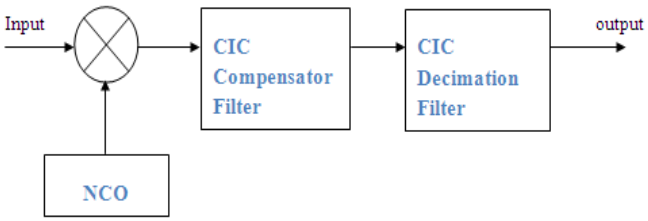


Fig:6 block diagram of DDC

Decimation means to decimate the (M-1) samples from the received signal. To distinguish between original sequence g(n), its decimated version is denoted by $g_D(n)$. The relation between the two sequences is given by

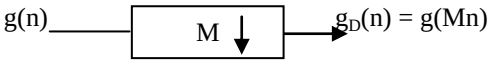
$$g_D(n) = g(M_N)$$

Where,

$$g(n) = \sum_{k=0}^{N-1} h(k)\,\hat{x}(n-k)$$

$$g_D = g(M_n) = \sum_{k=0}^{N-1} h(k)\,\hat{x}(M_n - k)$$

$$g_D = h(0)\hat{x}(M_n) + h(1)\hat{x}(M_n - 1) + h(2)\hat{x}(M_n - 2) + \ldots$$



DDC works exactly opposite to the DUC. The incoming signal is first multiplied with the carrier generated by the NCO which brings it back to the 0Hz frequency. This signal is then pass to compensator for pulse shaping followed by the CIC decimator to down sample the signal.

3. Maximum and minimum sample rate

The input and output frequencies of USRP depend on the DAC-ADC rate and decimation –interpolation factor. For any given USRP, the ADC-DAC sample rates are constant. Thus output/input frequency can be varied by changing the interpolation or decimation factor and no. of incoming samples. FPGA input clock rate is equal to the ADC sample rate and at the transmitter side, the incoming rate has been interpolated to meet the sampling rate of DAC. The input/output sample rate and frequency can be given as:

$$Input\ sample\ rate = \frac{ADC\ rate}{Decimation\ factor}$$

$$Input\ frequency = \frac{input\ sample\ rate}{no\ of\ samples}$$

$$Output\ sample\ rate = \frac{DAC\ rate}{Interpolation\ factor}$$

$$Output\ frequency = \frac{output\ sample\ rate}{no\ of\ samples}$$

D. Filters used in DDC and DUC

CIC filters are used for the interpolation and decimation of the incoming signal in the DSP unit of USRP FPGA. CIC filter consists of two stages, one having integrator filters and another stage having comb filters. Both stages have equal number of filters. Main advantage of using this filter is that it does not contain any multiplier and uses only adder, subtractor and register. Thus it can be implemented for the application having large range of sample rate. The interpolating CIC filter is used for up sampling the incoming signal and decimating CIC is used for down sampling the incoming signal.

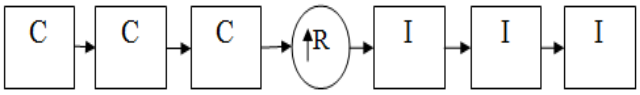


Fig.7 Interpolating CIC filter

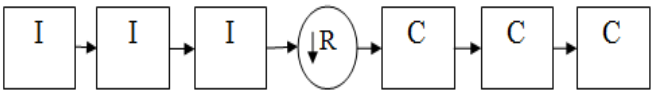


Fig.8 decimating CIC filter

CIC interpolating filter is used for up sampling the incoming signal in the digital up converter. The interpolator section have comb filter first followed by the up sampler and the integrator. CIC decimating filter is used for down sampling the incoming signal. In the decimating process integrator is at first stage followed by the down sampler and at last the comb filter.CIC decimating filter is shown in Fig.6. Interpolating and decimating CIC filter structures are shown in Fig.7 & 8 respectively. The comb section consists of a delay element and a subtractor. Structure of comb filter is shown in Fig.9.

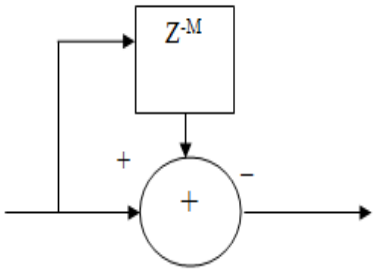


Fig .9 Comb filter

Comb filter having sampling rate fs/R and rate change R can be described by the equation as follows:

$$Y(n) = X(n) + X(n - RM)$$

where M is differential delay
After taking Z transform

$$Y(z) = X(z) + Z^{-RM}X(z)$$

$$Y(z) = X(z)[1 - Z^{-RM}]$$

Then the transforn function at fs is given by

$$HC(z) = \frac{X(z)}{Y(z)} = [1 - Z^{-RM}]$$

Integrator of the CIC filter consists of delay element and adder. Detailed structure of CIC filter is shown in Fig.10

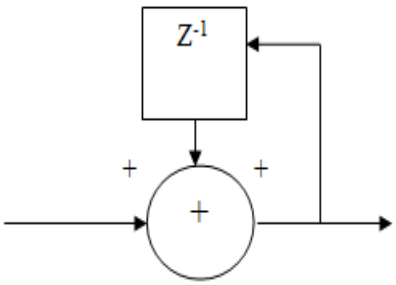


Fig.1**0** Integrator

Here,

$$Y(n) = Y(n-1) + X(n)$$

After taking Z transform

$$Y(n) = Z^{-1}Y(z) + X(z)$$

$$X(z) = Y(z)(1 + Z^{-1})$$

The transfer function for the integrator is given by

$$HI(z) = \frac{Y(z)}{X(z)} = 1/(1 - Z^{-1})$$

Then the transfer function of CIC filter is given as

$$H(z) = (1 - Z^{-RM})/(1 - Z^{-1})$$

V. PROCESSOR & ASSOCIATED ELEMENTS

A. Processor

The Soft Core Processor of the USRP FPGA is an aeMB Microblaze compatible processor. This is a CPU core that is capable of moving and manipulating data to and from memory. It does not have any peripheral nor interrupt controller but supports external interrupt. It uses wishbone bus interface [7]. All the functioning of DSP chain, Packet routing and other peripheral is control by on-board CPU [8]. It has an access to board devices through GPIO and SPI bus. CPU does not have direct access to the DSP chain data path. It communicates with host PC through UDP packets. It can directly access 512 bytes packet spaced in CPU FIFO. As shown in Fig.2 the CPU have a wishbone bus interface to all the component of the FPGA. aeMB features, which make it popular are as under:

- Harvard architecture with separate data and instruction buses.
- Pipeline architecture which provide quick access of data per clock.
- Small core with excellent performance

B. Internal Memory

USRP2 has an internal 1MB RAM for the data storage. There are eight sets of FIFO likes buffer used as arranging area, coupling the high turnout component of the FPGA such as Ethernet MAC, RX and TX DSP paths. The buffer is implemented as a dual port RAM within the FPGA. Each of the buffers is interfaced to the system processor. Four of the buffers are used as read-only operation from the FIFO on the transmit side of MAC and DSP unit and the remaining four buffers are used for write-only operation at the receiver side [5].

C. Wishbone Bus

Wishbone is a two wire, bidirectional serial bus interface that provides a simple and efficient method for data exchange between devices. It is most suitable for the application requiring occasional short distance communication between any devices. Wishbone is a true bus standard having collision and arbitration control when two masters opt to control the bus simultaneously to avoid corruption of data. The wishbone bus interface provides three transmission speeds: 100kbps, 400kbps and 3.5Mbps [6]. Features of wishbone bus are as under:

- Multi master operation
- Software programmable clock frequency
- Static synchronous design
- Bus busy detection
- Interrupt or bit-polling driven byte by byte data transfer
- Provide high speed data transfer

FPGA of USRP has a wishbone master bus for all device interfaces with the processor. As shown in earlier wishbone bus is a common bus interface between the all components of USRP. This bus an interface with SRAM which provide high speed data transfer between the memory and CPU. Various addresses of the devices are stored in the memory, from which wishbone provides the interface as per requirement. Wishbone bus has a direct interface to the GEMAC, which provides the address resolution of the received packet device. Buffer pool having dual port RAM has one port directly connected to the Wishbone bus. By having a common bus interface, several IP cores are able to work together with minimal efforts.

D. Vita Chain

The VITA is a transport layer protocol designed to provide interoperability between RF receivers and signal processing equipments. It provides interoperability by standardization of signal data transport, metadata transport and metadata types. The aim of VITA is to link logistic protocol format for the transmittal of digital IF data between one or more sources or destination [9]. This protocol enables necessary communication system requirements such as time stamping, oscillator and transmit receive control. This protocol enables all interface such as gigabit link and switch fabrics. VRT (VITA Radio Transport) is designed to be independent of physical and data link layer, therefore it may be carried over common protocols such as TCP, UDP, PCI Express and Gigabit Ethernet. Across the digital link or networks, VITA enables context and data information to be conveyed together efficiently. VRT specifies the packet based data stream where signal metadata is encoded in the packet header.

VRT supports four types of information: IF Data, IF Context, Extension Data and Extension Context. Correspondingly, there are four types of VITA packet streams as shown in Table I.

TABLE I

Contents	***Standard Formats***	***Custom Formats***
Data	IF Data Packet Stream Conveys IF Signals Real/Complex Data Fixed/Floting-point Formats Flexible packing schemes	Extension Data Packet Stream Conveys all signals or data derived from signal Any Type of Data Custom Packet Format
Context	IF Context Packet Stream Conveys Common Context for IF Data Frequency Power Timing Geolocation	Extension Context Packet Stream Conveys additional context for IF Data or Extension Data Any kind of Context Custom packet Format

Transmit path of VITA Chain gets the Data from the Buffer pool. This data received is 36-byte value, from which VITA header is removed from the VITA de-framer and then sent for processing to DSP unit. The context packet sets all the DSP parameters for the DSP unit. VITA provides a proper sampling rate and frequency compatible with the DAC and ADC of the Daughter board. Flow control and Error control are carried out in the TX path of VITA.

In the receiving path, VITA adds timing information for the controlling operation. It gets the received RF signal which is down-converted in DSP unit. VITA RX adds additional information and passes the packets to the router. This packet format data are more portable and flexible.

VI. CONCLUSIONS

USRP have become a well known platform for hardware based testing for wireless application. The system set up using the USRP has been cheaper than the conventional mode of testing the wireless application. In this paper, the entire communication path of the in-built FPGA is studied, which provide the testing platform for the complete communication over the USRP. The full integration of message passing infrastructure and adopting of VRT protocol will be a revolutionary change in developing radio system. This paper concludes that the on-board FPGA has been the heart of the system implemented using USRP. With the study of the USRP and its inward stack, one can design the desire a system for wireless testing or emulating a wireless network. This can be achieved by interfacing the target device such as PC with the USRP.

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