A low-power and high-speed Wallace 10x10 Multiplier based on 4-2 Compressors

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Abstract - **In this paper, a power and performance efficient 10x10 Wallace Tree Multiplier based on 4-2 Compressors is presented; especially for use in Digital Signal Processors and in Microprocessors. This Wallace multiplier uses 4-2 Compressors in the partial-product reduction phase which consecutively reduces the maximum output delay and also lowers power consumption. The 4-2 Compressor used in the design of multiplier is made from high-speed and low-power XOR-XNOR module and Multiplexer with transmission gates. On using these Compressors in the multiplier, the number of interconnections gets reduced, which further produces quick results, along with consuming lesser power. The power, delay and power-delay product (PDP) are compared with normal Wallace Multipliers, implemented without compressors, and is proven to have minimum delay, power consumption and PDP. The Simulation results were obtained at 0.18µm standard CMOS technology by using HSPICE tool.**

Keywords- 4-2 Compressors, Wallace Tree Multipliers, XOR-XNOR module, Multiplexers, low power-delay product PDP.

I. INTRODUCTION

With the advent of portable devices, there is a continuous demand for low power and high speed multipliers with the rising need for having power and speed efficient VLSI implementations. Multipliers are the key elements in several Computer Arithmetic circuit applications like Image and video Processing, Multimedia like in Oscillators and Microprocessors like in ALUs, Multiplier and accumulator units, Digital Signal Processors like in Filter designing, convolutors etc., . In most of the VLSI systems, multiplier lies in the critical path directly. The performance of multipliers helps in influencing the performance of several DSP algorithms and processor's running speed. So, for these reasons, the designers are now focussing on multipliers of high speed and at the same time maintaining low power consumption and further to have low power delay product.

In a tree multiplier architecture there are generally three phases, which are firstly partial product generation phase, then the partial product reduction phase and finally the addition phase to obtain the final result by adding the resulted two rows. Among these three phases, the second phase, which is partial product reduction phase typically consumes most of the power and this is responsible for overall critical path delay. Therefore in order to optimize this reduction phase, Compressors can be used for partial product accumulation [1]. Column Compression (CC) is the technique used to reduce the power consumption and delay in multiplier design, in which the compressors used in multipliers are accumulated with partial products column–wise [2].

Compressors are used for performing addition operation and they contribute towards reduction in critical path delay, which is important for maintaining circuit's performance. This can be accomplished with usage of 3-2 Compressors and 4-2 Compressors. 3-2 Compressors are also called Full Adder Cells. The Compressors are internally composed of XOR-XNOR and multiplexer modules and the improved design of these modules will contribute a lot towards improving overall system performance.

In the present work, 4-2 Compressor used in the design of Wallace 10x10 multiplier is made from high-speed and low-power XOR-XNOR module and Multiplexer using transmission gates. Usage of Compressors helps to give minimum number of partial-product reduction stages, with reduction in delay, power consumption and in addition, PDP of multiplier gets reduced.

This paper is organised as follows: Section 2 explains elements in 4-2 Compressor and its design. In section 3, Wallace tree multipliers are discussed. In section 4, 10x10 Wallace scheme based on 4-2 compressors is introduced. Experimental results and evaluation of Wallace scheme against normal Wallace multiplier are presented in section 5. And finally, we conclude the work of paper in Section 6.

II. COMPRESSORS

Compressors are generally used for performing addition operations. Higher order Compressors can be designed by interconnecting lower order compressors, like a 4-2 compressor can be made from two full adders. In designing a multiplier, 4-2 Compressor is optimal for constructing regularly structured Wallace tree with less complexity. Usage of compressors will help to have less number of interconnections.

A. Elements present in Compressors

Compressors are made out of XOR - XNOR and Multiplexer modules. There are larger number of XOR-XNOR gates and Multiplexer (MUX) modules reported in the literature. Apart from compressors, XOR-XNOR gates are also used as building blocks in Comparators, Parity Checkers, Pulse generators, Oscillators, etc.

Static CMOS type of XOR-XNOR module uses both pMOS and nMOS transistors and it consumes large amount of power and many transistors and so larger area [3]. Static XNOR-XOR also uses Complementary CMOS style of pull-up and pull-down transistors, but it also has large power consumption and not used at low voltages [4]. A XOR-XNOR gate with feedback transistors is suitable at low voltages but the input load is doubled, and this causes

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slow response if cascaded [5], and area increased. To have high speed performance than the earlier three types of XOR-XNOR gates, it is convenient to use the XOR-XNOR module as shown in Fig. 1 [1]. It can operate well at low supply voltages and it uses only 8 transistors. It also provides good driving capability.

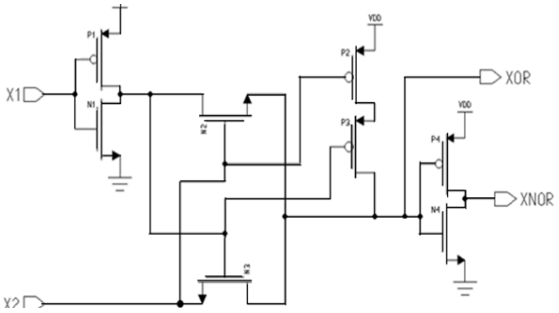

Fig. 1: Circuit diagram of XOR-XNOR

The Multiplexer (MUX) module is used in Compressors for Carry generation. The Multiplexer output is based on Select lines (S). If there are 2 data inputs, it is called 2 to 1 MUX. Static MUX using Complementary CMOS style transistors [3] and MUX with transmission gates and output buffer both consume larger area and delay. So, in Compressors, MUX using transmission gates consuming 6 transistors [6] as shown in Figure 2 can be used, in low power cells for faster results within low area.

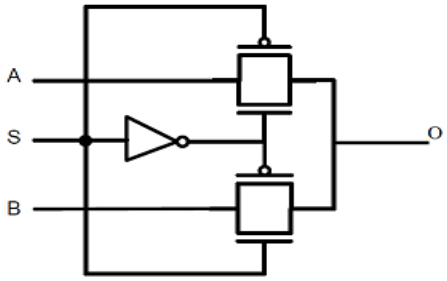

Fig. 2: MUX using transmission gates

B. Design of a 4-2 Compressor

In general 3-2, 4-2 Compressors are mostly used. A 3-2 Compressor is also known as a Full Adder Cell with three equal weighted inputs and outputs as Sum, Carry. A 4-2 Compressor have 5 inputs called X1, X2, X3, X4 and Cin (Carry-in) and it produces 3 outputs Sum, Carry and Cout. Here, the Carry and Cout bits have one bit higher weight than other bits. In this, the Cin and Cout bits are independent to each other. By connecting two full adders serially, a 4-2 Compressor can be implemented. The Block diagram of a 4-2 compressor is shown in Fig. 3 [7].

A 4-2 Compressor designed with the above mentioned XOR-XNOR and MUX modules, requires fewer transistors and so occupy low area and moreover the power consumption is minimal. The resulting output's delay can be still minimized if instead of XOR-XNOR when MUX block is used at Sum output because the select bit Cin is applied prior to the inputs that results in transistor switching before inputs arrive. The equations governing the outputs of 4-2 Compressor are,

$$\text{Sum}= (X1\oplus X2)\bullet\overline{X3\oplus X4}+\overline{(X1\oplus X2)}\bullet(X3\oplus X4)\bullet\overline{Cin}+\overline{(X1\oplus X2)}\bullet\overline{X3\oplus X4}+\overline{(X1\oplus X2)}\bullet(X3\oplus X4)\bullet Cin$$

$$\text{Carry}=(X1\oplus X2\oplus X3\oplus X4)\bullet Cin+\overline{(X1\oplus X2\oplus X3\oplus X4)}\bullet X4$$

$$\text{Cout}= (X1\oplus X2)\bullet X3+\overline{(X1\oplus X2)}\bullet X1$$

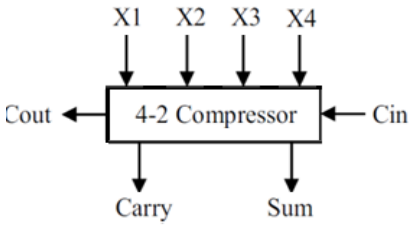

Fig. 3: Block diagram of 4-2 Compressor

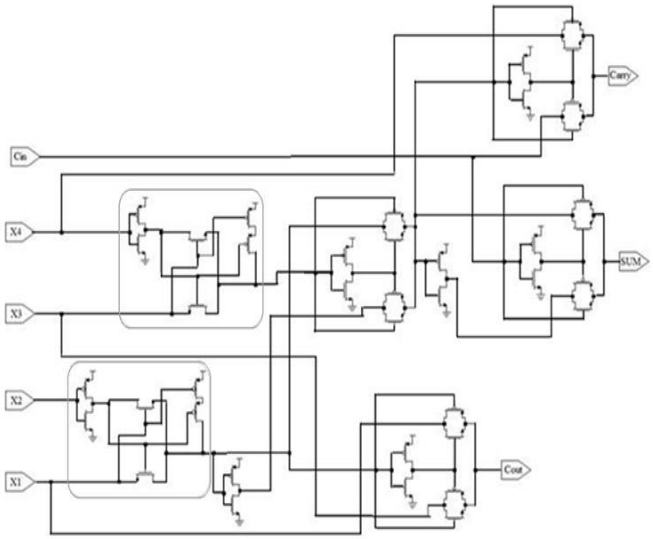

Fig. 4: Transistor model of 4-2 Compressor

The transistor model of 4-2 compressor shown in Fig. 4 has only 40 transistors. The critical path delay of the above mentioned 4-2 compressor is reduced to one XOR and two MUX delays.

III. BASIC WALLACE MULTIPLIERS

The tree multipliers are also called parallel multipliers. They are performance efficient in general. Their first phase called partial product generation is implemented by multiplying each multiplicand and multiplier bits by performing AND operation. Tree multipliers are meant for adding a number of partial products at a time and so further reducing the number of steps needed to reduce the partial products into 2 rows of final intermediate results. The Tree multipliers differ mainly in the Partial product reduction phase based on the mode of partial product reduction algorithm used. The last phase of addition performs addition of the reduced 2 row bits using Carry Propagate Adder (CPA) to produce the final result.

A. Normal 10x10 Wallace Tree Multiplier

Wallace Tree multiplier is a fast process for multiplying two numbers that was introduced by Wallace. In general, Wallace Tree multiplier will accumulate the generated partial products column-wise into three and two bits and

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gives them appropriately to Full-Adders and Half Adders respectively to reduce them as Sum and Carry bits. The bits that does not belong to these adders are bypassed to next stage. Sum bit is given to next stage of same weight and carry is propagated to a column of one-bit higher order in next stage.

Wallace accumulates as many bits as possible into adders [8]. At each stage, this process is continued until the stage height is reduced to 2 rows. The Wallace tree 10x10 multiplier along with its reduction stage is shown in Fig. 5, with six stages. The partial products are reduced in 5 stages and the Stage six uses Carry Propagate Adder. In Wallace 10x10 multiplier, 76 Full-adders and 36 Half-adders are used.

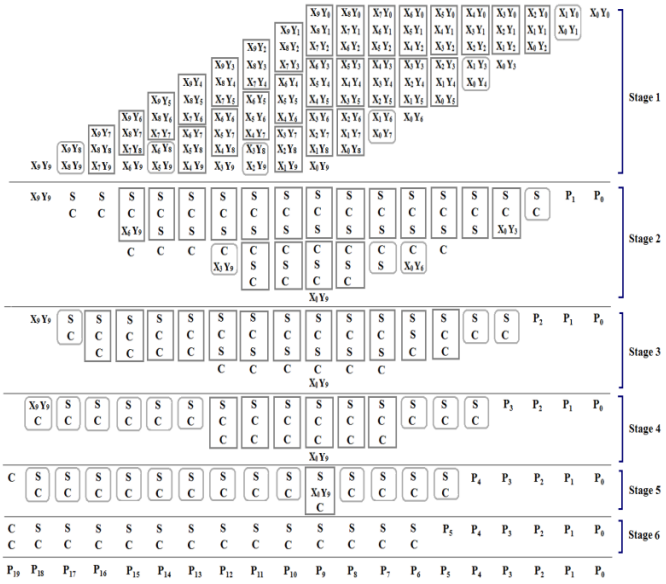

Fig. 5: Normal 10x10 Wallace Tree Multiplier

IV. WALLACE MULTIPLIER BASED ON 4-2 COMPRESSORS

Compressors when used in partial product reduction phase in multipliers will help in having lesser number of interconnections and adder cells. In high speed multipliers, usage of compressors instead of conventional full and half adders lead to quick output generation and as well the number of reduction stages gets reduced. Compressors of higher order can be used in multiplier design. When compared to two full adders, a 4-2 Compressor has lesser delay and power consumption as the interconnections are reduced. A CC multiplier, with equal size multiplicand and multiplier bits and built with compressors have considerable flexibility in allocating the number of cells to different partial product reduction stages [2]. The 4-2 compressor shown as transistor model in Fig. 4 is well suitable in Multiplier's design as that require fewer transistor count and it also provides better performance.

A. Design of 10x10 Wallace Tree Multiplier using 4-2 Compressors

On using compressors the number of reduction stages in Wallace 10x10 multiplier gets reduced to 3, instead of 5 stages when only half and full adders are used. A 10x10 Wallace Tree Multiplier based on 4-2 compressors is shown in Fig. 6. 4-2 Compressor inputs are represented by rounded rectangles. On using compressors in partial product reduction [9], the number of reduction stages gets reduced to 3, rather than 5 stages when only half adders and full adders are used. After stage3, the result is given to a Carry Propagate Adder (CPA). The power, delay and in addition the PDP also gets reduced. The 10x10 Multiplier uses 31 no. of 4-2 Compressors, 24 full adders and 20 half adders. This Wallace tree has lesser delay compared to the one which does not use 4-2 compressors.

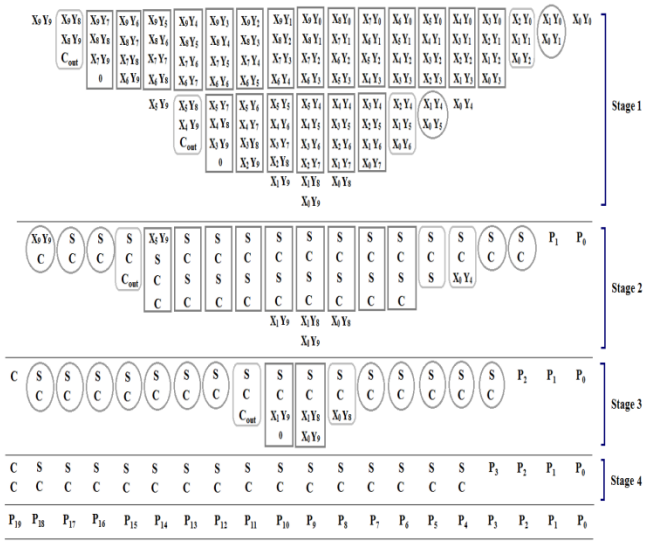

Fig. 6: 10x10 Wallace Tree Multiplier based on 4-2 Compressors

V. ASSESSMENT AND EXPERIMENTAL RESULTS

With the usage of 4-2 Compressor shown in Figure 4 in the design of 10x10 Wallace Tree Multiplier, the reduction stages gets reduced and this leads to lower power consumption and minimal output delay and further leads to have lower power delay product (PDP). As 4-2 Compressors provides quick outputs and has less number of interconnections than multipliers with full adder cells. This present Wallace Multiplier exhibits better speed and power performance than normal Wallace tree Multiplier which uses only full and half adders (of Figure 5). This can be easily noticed from the comparison Table 1 between Proposed Wallace multiplier using 4-2 Compressors and Multiplier format. At a supply voltage of 3.3V, the Inputs(X, Y) and Simulation results (P_0 –P_{19}) of the proposed 10x10 multiplier using 4-2 Compressors is shown in Figure 7(A) and 7(B)

Table 1: Comparison of Proposed 10x10 Wallace Multiplier using 4-2 Compressors against normal Wallace Multiplier

10x10 Wallace Multiplier	Power (mW)	Delay (nS)	PDP (pJ)
Normal	0.743	14.14	10.51
With 4-2 Compressors	0.735	11.47	8.43

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Fig. 7(A) Inputs X, Y of Proposed 10x10 multiplier

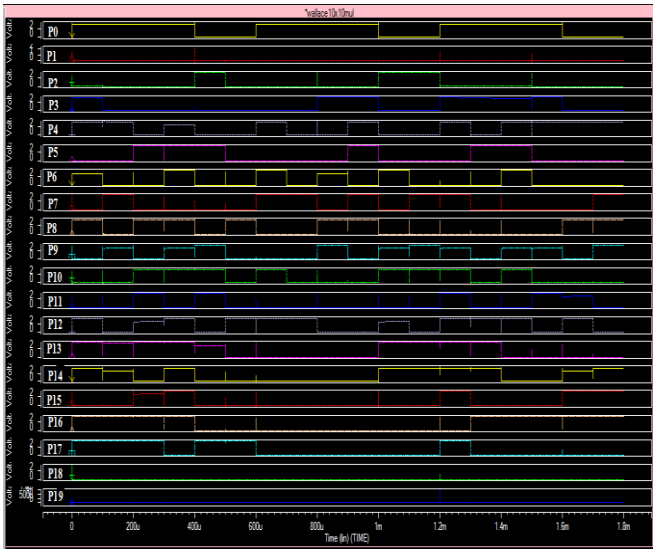

Fig. 7(B) Simulation results (P_0 –P_{19}) of the proposed 10x10 multiplier

VI. CONCLUSION

A low power and high speed 10x10 Wallace Tree multiplier has been presented for having high performance, which uses 4-2 compressors made from an XOR-XNOR gate of good driving capability, high speed and low power and Multiplexer made of transmission gates. This proposed Wallace multiplier produces quick results with less power consumption and further minimum power delay product (PDP).This present Wallace 10x10 multiplier shows optimal power and performance against normal Wallace multiplier implemented without compressors, when the Simulation results were performed using Synopsys HSPICE at 0.18µm CMOS technology.

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