MODELING OF INTERFACE FOR FPGA AND EXTERNAL SRAM USING VHDL

Supreetha M, Kiran Kumar V.G, Kanhu Charan Padhy

Abstract— With the envisage of many of the DSP applications, there is a requirement of large storage capacity. Even though the FPGAs provide the on chip memories, these memories may not be sufficient for some applications. In order to overcome this problem, the external memory can be used and can be interfaced with FPGAs. The Model is the image of the circuits This paper brings out the interfacing of FPGA-XC6SLX45 on Spartan6 of Xilinx platform and external sram IS61C256AH using VHDL code. The complexity of digital system design has been reduced with the use model concept using hardware languages like VHDL/or Verilog.

Index Terms—External SRAM, FPGA, Xilinx 10.1.VHDL (VSIC Hardware Description Language)

I. INTRODUCTION

Complexity of today's system designs are growing, requiring larger amounts of memory for high performance buffers and local data storage. Logic gates and memory required for some system designs are implemented on the single FPGA device containing embedded SRAM. Easy solution to the memory is provided by FPGAs with on-chip RAM. But, for the external storage requirements, external memory becomes necessary. Hence, for many data/program storage applications, an FPGA with an external memory device can meet the functionality requirements and it is more cost effectively. This paper brings out a solution to such exercise of interfacing an external memory ***IS61C256AH*** and FPGA on board Spartan 6 of Xilinx Platform. The circuit design mapping has been done with help of an hardware description language , VHDL . The program has been loaded on the FPGA XC6SLX45 to enable the data & control transfer to take place to and fro between the external memory ***IS61C256AH***, and XC6SLX45. Now a days, the programs are made easy with the help of programming tools. In this paper, it has been made with use Xilinx ISE core generator tools. This helps in configuration building and generating codes for the memory interface. The platform, it has been used is Xilinx Spartan6 in CSG324 package, which is built in with 512 Mbit LPDDR memory with many GPIOs for external interface. It has a SPI flash memory for configuration storage and a crystal Oscillator of 100 MHz as a clock source.

II. INTERFACE ELEMENTS

a. **External Memory, *IS61C256AH*:** A primary distinction in memory types is volatility. Volatile memories can hold their contents only while the power is available to the memory device. The memories lose their contents as soon as power is removed. Non- Volatile memories retain their contents when power is switched off also. However, it usually guarantees to be erasable a given number of times, after which it may fail. Memories can be either on-chip or external to FPGA. The choice of memory depends on the following factors: Bandwidth and speed, Storage area and Capacity, Cost , Latency, Power consumption. The use of external memory has its own advantages and disadvantages. External SRAM devices provide larger storage capacities

ISSN: 2278 – 1323

than on-chip memories, hence it is easy to interface, can also share external SRAM buses with other external SRAM devices. Interfacing the external SRAM to FPGA is very helpful for DSP applications. There are several types of external SRAM devices. The selection of SRAM depends on the type of applications.

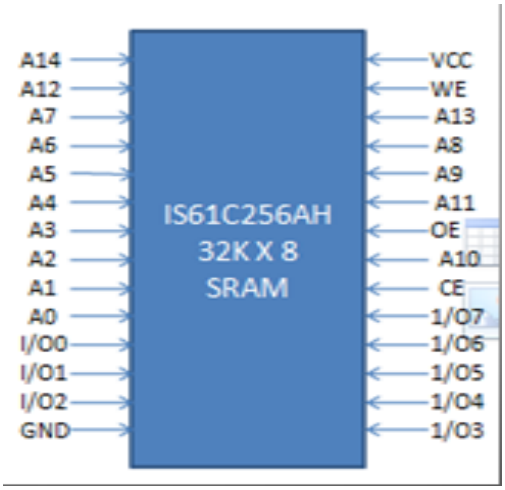

Figure1: Pin diagram

Mode	WE	CE	OE	I/O operation
Not selected	X	H	X	High Z
Output disabled	H	L	H	High Z
read	H	L	L	Dout
write	L	L	X	Din

Figure 2: Truth table of IS61C256AH

b. **Seven segment display:** A seven segment display is a type of electronic display for displaying decimal numbers. The segments in 7 segment display are represented by the letters A to G and also an decimal point (DP) is used for the display of non-integer numbers. SSD may use a LCD (liquid crystal display) or a LED (liquid crystal display) for each segment. In a simple LED package, all the cathodes or all the anodes f the segment LEDs are connected and brought out to a common pin and is referred to as common cathode or common anode device.

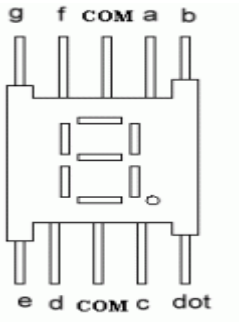

Figure 3: Seven Segment Display

c. **FPGA:** FPGAs are the reprogrammable silicon chips containing 2 dimensional arrays of logic blocks and interconnections between logic blocks. We can configure these chips to implement custom hardware functionality using prebuilt logic blocks and programmable routing resources. Once the digital computing tasks are developed in software, it is compiled down to a configuration file or bitstream that contains information on how the components should be wired together. FPGAs can be reconfigured completely.

II. INTERFACING FPGA AND SRAM

The SRAM used here is 32K x8 high speed CMOS static RAM with high speed access time of about 10,12,15,20ns, low active power of 400mW,single 5V power supply. It has 15 address lines, 8 bidirectional data input/ output ports and 3 control lines such as $\overline{CE}$,$\overline{OE}$, $\overline{WE}$. When $\overline{CE}$ is high, the device assumes a standby mode at which the power dissipation can be reduced. With active low chip enable $\overline{CE}$ input and an active low output enable $\overline{OE}$ input the easy memory expansion is provided. The active low write enable $\overline{WE}$controls both writing and reading of the memory.

ISSN: 2278 – 1323

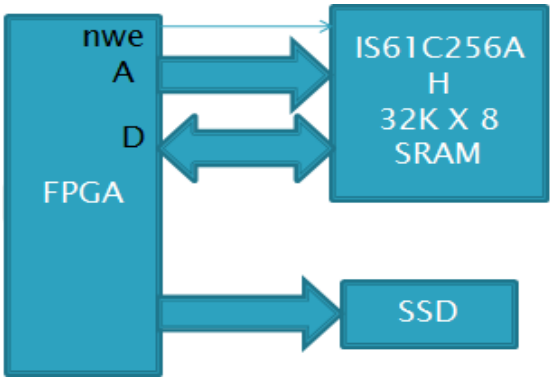

Figure 4: Interface diagram

The above interfacing diagram consists of the FPGA to which IS61C256AH, 32K X8 SRAM is interfaced. The application circuit used to check the successfulness of interface are LEDs. Here the 8 bit vector passed to the SRAM from FPGA through the bi-directional data bus, which is displayed through LEDs. The clock frequency should be reduced since the external SRAM cannot be accessed with the high frequency clock. The code also includes the bi directional bus between the FPGA and the memory, and output bus between the FPGA and the test circuit.

III. RESULT AND ANALYSIS

The simulation is carried out using Xilinx 13.1 using Spartan 6 FPGA. The write and read operation to and from the memory can be seen in the simulation shown in the figure 5.

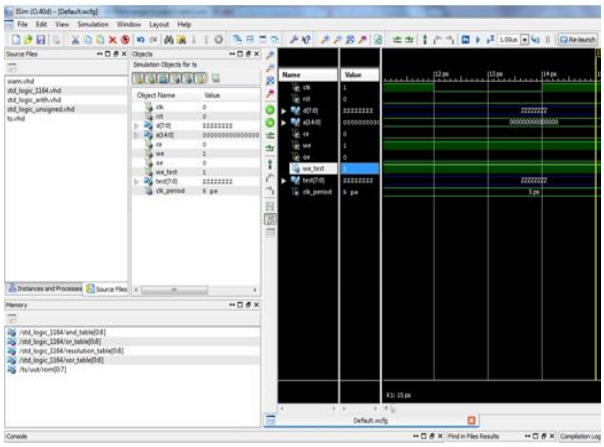

Figure 5: Simulation result

REFERENCES

[1] Digital design using VHDL by Charles H Roth.

[2] HDL programming VHDL and verilog by Nazeih M Botros.

[3]VHDL basics to programming by Gaganpreet Kaur.

[4] UG416 June 22, 2011-Memory interface Solution guide with Spartan6, by Xilinx.pdf

[5] IS61C256AH, 32K X8 SRAM.pdf

Ms. Supreetha M, received her B.E degree in Electronics and Communication Engineering from Srinivas Institute of Technology in 2013 and currently pursuing her M.Tech in VLSI & Embedded systems in Sahyadri College of Engineering & Management. Presently, she is engaged in the proto-type Design & Development of Digital System in KCTRONICS Innovative Consultancy Services on internship.

Mr.Kiran Kumar.V.G has done his B.E and M.Tech in Microelectronics from NMAMIT, Nitte. He had secured 3rd rank in M.Tech (Microelectronics & control systems) in V.T.U. he has got 11 years of experience in teaching profession.

Shri Kanhu Charan Padhy, has been graduated from UVCE, B.U, Bangalore (Electronics) .He has done his PGDBA in HRM&Finance. He has served in DGAQA,Govt. Of India as a Group 'A' Officer. He has published some articles like 'Quality in Design and Reliability through Repair' in the Quality Focus Journal of ADE,DRDO. He has published one paper in the National Conference on Ground and Flight Test of Systems Used in Military aircraft. At NaSMAC-2004.20-21 August 2004,, Bangalore & another paper in the International Conference on Quality & Reliability in Aerospace Systems, Jan15-17, 2006. Organized by RCI, DRDO, Hyderabad .He has been declared as the Best Citizen of India during 2003.He has been awarded with Commendation by the Gp Capt. P.Kamraju. He has served as a guide for the management students in the field of finance. Presently he is the M.D of Kctronics innovative consultancy services private limited, Professional Membership: SAQR (The Society for Aerospace Quality & Reliability) : Life Membership #LM192.

ISSN: 2278 – 1323