LOW POWER MODELING OF HIGH SPEED CAM WITH CONTROLLED SENSING DELAY.

S SALMAN, KUPPAM N CHANDRA SEKHAR, R MALLIKARJUNA REDDY

***Abstract* — the growing technology trends of extremely low power operated handy applications like PC, note book, smart phones and other electronic gadgets requires microelectronic devices with low power consumption. It is obvious that the transistor dimensions goes on to shrink and as require for more complex chips to increases and as a consequence power organization of such deep sub-micron based chip is one of the major issue in VLSI industry. The manufacturers are always concentrated for low power designs to provide adequate physical resources to withstand against design hurdles and this lead to increases the cost and restrict the functionality of the device. This power reduction ratio is the highest among FFs and their related designs like RAM, ROM and CAM that have been reported so far. Therefore power reduction is the critical issue at design level. It is familiar that Content addressable memory (CAM) offers high-speed search function in a single clock cycle. Due to its parallel match-line contrast, CAM is more power dissipative unit. Accordingly, strong, high-speed and low-power sense amplifiers are extremely required in CAM designs. In this document, we proposed a new CAM structure which drastically reduces more than 40% sensing delay and overall power consumption is stagnant with gating technique. The performance of this paper is evaluated on the design simulation using Microwind 3.1 simulator with 32nM CMOS design.**

***Index Terms* — Low power systems, CAM, Sensing Delay, Gating Technique, 32 nm CMOS Technology.**

I. INTRODUCTION

Power dissipation has become a major and more critical design parameter for VLSI circuits particularly at deep sub-micron technology. The new obligation for portable operations of all types of electronic designs has invited for decrease in the burden and size of the device which is compressed by the number of power sources used and their lifetime. With the active propensity of reducing the transistor size, reducing the supply voltage and making more complex designs at chip level has resulted in large power dissipation. The disparity of power dissipation with technology trends has predicted in figure1. This gives rise to rise in temperature of the chip thereby increasing need for cooling and packaging. But the system cost is also one of the key- maker in the IC market diffusion. Therefore, there has been an augmented order for low power CMOS designs. When target is a low power circuit design, the search for the most beneficial clarification must be done at each level of the design process. Decrease of power consumption makes a device more consistent. The necessitate for devices that consume a least amount of power was a major powerful force behind the development of CMOS technologies. At the circuit design level, there are many alternative to power savings exists for implementing combinational circuits. This is because all the important parameters leading power dissipation are identified to be of switching capacitance, transition activity, and short-circuit currents are strongly predisposed by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different presentation aspects become more significant.

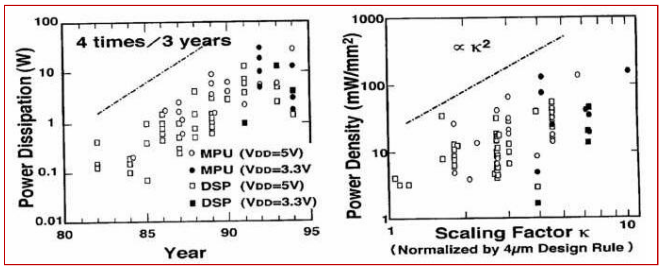

Figure1: Power Dissipation Vs Technology Trends

DESIGN DEVELOPMENT

Content addressable memory (CAM) is a kind of solid-state memory in which data are accessed by their contents somewhat than substantial locations. It receives input search data known as a search word [1], and returns the address of a analogous word that is stored in its data-bank. In broad, a CAM has three operation modes: READ, WRITE, and COMPARE, among which "COMPARE" is the main operation as CAM rarely reads or writes. Fig2 shows a basic block diagram of a CAM core with a built-in search data register and an output encoder. It begins with a compare operation by loading a predefined bit input search word into the search data register[5]. The search data are then transmit into the memory banks through finite pairs of complementary search-lines [8] and thereby directly verified with every bit of the stored words using comparison circuits. Each stored word

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has a Sense Line that is shared between its bits to suggest the verified result.

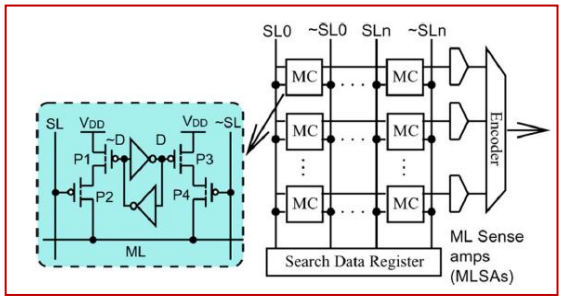

Figure2: Traditional CAM Circuit

While all accessible words in the CAMs are compared in parallel, result can be obtained in a single clock cycle. For this reason, CAMs are faster than other hardware- and software-based search systems [1][2]. Hence the CAM circuits are suggested for high-yield applications such as network routers and data compressors. On the other hand, the full parallel search operation gives rise to significant challenges in designing a low-power system for high-speed and high-capacity CAMs, the various problems or design hurdles identified and they are 1. More power hunger as the switching activity between Search Line (SL) and Matched Line (ML). 2. A sudden current flow known as surge current at the time of beginning of Search operation which leads to serious IR drop and leads to un controllable power dissipation. Therefore the existed CAM designs need to be altered to overcome afore mentioned issues. And this article suggests the CAM design to overcome unnecessary power dissipation and also included with power-gating technique to limit the unwanted IR drops.

II. MODELING OF POWER GATED CAM

In Large Scale Integration usually more than 50% of the power is dissipated in random logic of and thereby in almost all sequential design half of the power is dissipated by flip-flops (FFs). During the past research, several low-power FFs have been swift into logic development. However, in actual chip design, the conventional FF is still used most often as a ideal FF because of its well-balanced power, performance and cell area. The intention of this paper is to present a clarification to attain all of the goals of power reduction without any degradation of timing performance and the target area of the CAM cells

Proposed design:

The anticipated CAM architecture is shown in Fig3. The CAM cells are prearranged into rows (word) and columns (bit). Each cell has the identical number of transistors as the conservative P-type NOR based CAM and uses a related Matched Line structure. Though, the "COMPARISON" unit, the relevant transistors as shown in figurre3, and the "SRAM" module, i.e., the cross-coupled inverters, are powered by two disconnect metal rails, known as V_{DDML} and V_{DD}. The V_{DDML} is independently guarded by a power transistor and a feedback loop that can auto turn-off the Matched Line current to save power. The reason of having two disconnect power rails of is to completely segregate the SRAM cell from any opportunity of power disorder during COMPARE cycle [6][7].

The power-gated transistor as shown in figure3, is guarded by a feedback loop, denoted as "Power Control" which will mechanically turn off the Matched Line Current if once the voltage on the Matched Line reaches a certain threshold. At the beginning of each and every clock cycle [3][4], the Matched Line is first initiated by a global control signal. When this happened and enable signal will be automatically is set to low and the power transistor is turned to off state. As a result the Matched Line signal grounded. Immediately the enable signal turns to high state and initiates the COMPARE phase. If one or more mismatches happen in the CAM cells, the Matched Line will be charged up. Fascinatingly, all the cells of a row will contribute to the limited current accessible by the transistor, in spite of any number of mismatches. The technique will acts as a guard to the unnecessary IR drops across the Matched Line for all the ROWs of the CAM structure. And the relevant layout is shown in figure4 and the proposed 4 X 4 CAM matrix layout is shown in figure5.

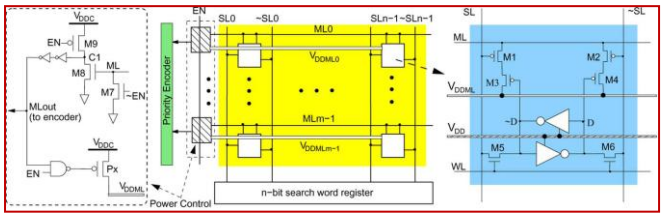

Figure3: Proposed CAM Structure

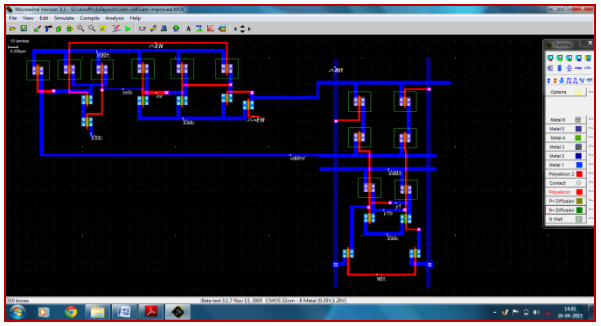

Figure4: Layout of Proposed CAM cell

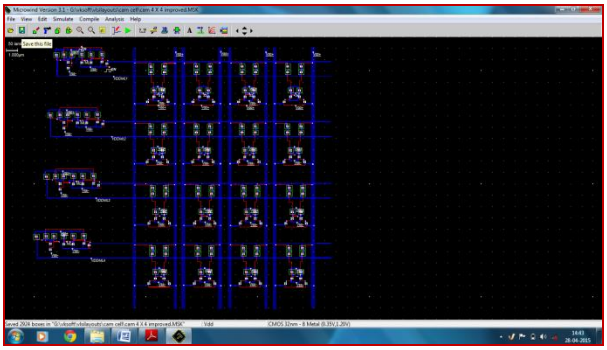

Figure5: Layout of Proposed 4 X 4 CAM Matrix

III. SIMULATION RESULTS

All the layout design description of the above article is simulated and analyzed using Microwind 3.1 Layout design tool and physical design layout results are observed separately with the help of 32nm technology, it is noticed that at some instance of simulation time the power and time delays are greatly improved with the implementation of proposed architecture, the various results are shown below. The figure6 and figure7 shows the simulation output of proposed CAM and its 4 X 4 matrix arrangement and figure8 predicts the current graph of the proposed design.

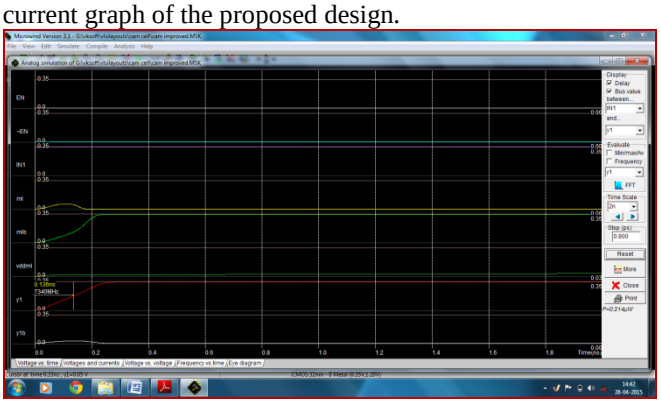

Figure6: Simulation output of proposed CAM

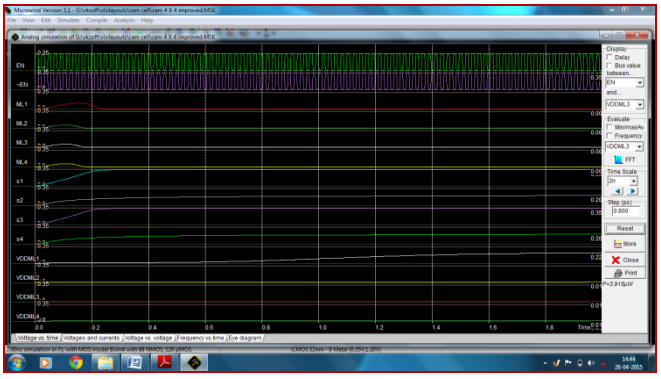

Figure7: Simulation output of proposed CAM 4 X 4 matrix

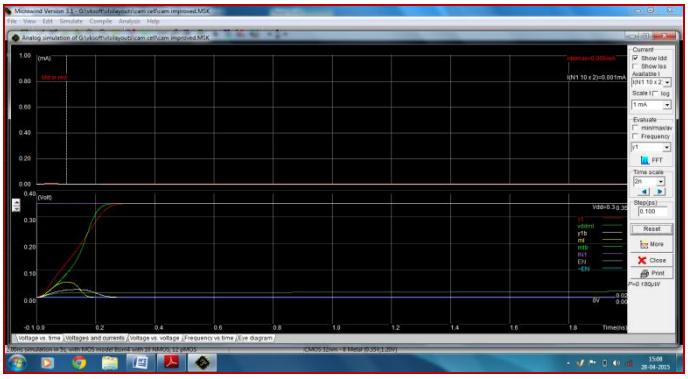

Figure8: Current graph of Proposed Design

The performance metrics at various nm are summarized in the following Table1.

TABLE 1

SUMMARY OF PERFORMANCE REPORT

parameter	90 nm	65 nm	45 nm	32 nm
Power	7.822µW	1.489 µW	0.278µW	0.180µW
Delay	892 pS	538 pS	521 pS	320 pS
I_{dd} Max.	0.092mA	0.026mA	0.006mA	0.005mA
V_{dd} Max.	1.20 V	0.7 V	0.40 V	0.35 V
W/L	1/0.1	1/0.07	1/0.05	1/0.04

IV. CONCLUSION

This paper analyzes the existed CAM topologies and suggested a comprehensive CAM structure to overcome unnecessary power dissipations occurred in the CAM due to their large switching activity and IR Drops. The proposed work may eliminate the problem of CMOS total power dissipation between logic transitions occurred in CAMs. And suggested design improves the area utilization also this paper has realized with Layout design tools and the relevant layouts are analyzed and various physical parameters are studied at 32 nm Technology. Such designs are suggested to exhibits a competitive performance with current work.

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