

Quantum Cost efficient Reversible Multiplier

Mandeep Kaur, Chakshu Goel

Abstract — Increasing demand for reducing power dissipation in digital multipliers has led to new mode of computation for multiplier design is reversible logic computation model. Reversible logic is a term originating from quantum computing. Reversible multiplier circuits have extensive application in futuristic technologies such as DSP, Fast Fourier transform, Convolution and Discrete Cosine transform. This paper propounds a novel 4×4 bit reversible multiplier circuit. This proposed reversible multiplier is faster, having less number of primitive reversible gates (Quantum cost) as compare to the existing designs. The proposed reversible multiplier circuit constructed using Peres Gate and MTSG Gate and can multiply two 4 bit binary numbers.

Index Terms— Quantum Computing, Reversible logic circuits, Nanotechnology.

I. INTRODUCTION

One of the major problem in the conventional irreversible circuit is the wastage of large amount of internal energy in the form of heat. A main goal in the VLSI circuit design is to reduce the energy wastage. Landauer [1] illustrates that irreversible hardware calculations causes a lot of internal energy wastage. According to Landauer's principle, in an irreversible operation, losing one information bit dissipates $kT \ln 2$ Joules of energy, where T is the absolute temperature and k is Boltzmann's constant ($k = 1.3806505 \times 10^{-23} m^2 K^{-1} kg^{-2}$). In the reversible logic circuits, the internal power consumption is approximately equal to zero, because these reversible circuits do not have the wastage of internal energy. Bennett [2] proved that the reversible circuits would not lose energy because they do not loss the information. In reversible circuit, the number of inputs are equal to number of outputs. So, the outputs can be used to drive the inputs in the reversible circuits [2], [3]. In the recent years, reversible logic is emerging as an intensive research topic, having extensive applications in diverse fields, such as low-power VLSI design, DNA computing, Quantum computing, nanotechnology and data security. Designing the quantum circuits needs reversible logic gates. The basic reversible gate parameters are quantum cost, total logical calculations, the total number of gates used, number of ancillary inputs and number of garbage outputs.

Quantum Cost refers to the cost of the circuits in terms of the cost of primitive gates (NOT, V and V^+ gates). Each reversible logic gate has a specific quantum cost. Total logical

calculations are the count of the NOT (δ), AND (β) and XOR (α) in the output expressions. [12] The Garbage outputs are the outputs that are not used in the calculation. The Ancillary inputs are added to the reversible circuit to make the circuit reversible. In designing a reversible circuit, these mentioned features tries to improve. Thus, in designing the new reversible circuit, it is tried to minimize the quantum cost.

In the arithmetic computational unit, the multiplication is one of the most effective operations. This arithmetic operation is performed in ALU, Fast Fourier transform, Discrete Cosine transform through the use of multiplier. In reversible operations, the information loss creates heat. To minimize the heat loss, design and implementation of digital circuits using reversible logic is adopted into the future computing technology [2]. In this paper, we have propounded 4×4 reversible multiplier circuit by Peres Gate (PG) and MTSG gate. Multiplier circuit has basically two subsections: first is partial product generation and second is the addition of partial product. In the first part partial product generation, we have used 16 Peres gate (PG) and in the second part addition subsection, 8 MTSG and 4 Peres gates are used to produce least quantum cost.

II. BASIC REVERSIBLE LOGIC

The n-input and k-output Boolean function F [17] is called reversible functions if:

- There is unique one-to-one mapping between its input vector (I_{vec}) and output vector (O_{vec}). Thus, the vector of input state can be recovered from the vector of the output state.
- Fan-out and feedback is not permitted.
- The number of inputs must be equal to number of outputs.

A. Basic Terms related to Reversible Logic

Quantum Cost: Any reversible gate can be recognize using the 1×1 NOT gate, and 2×2 reversible gates such as Controlled-V and Controlled- V^+ (V is a square-root-of NOT gate and V^+ is its hermitian). These gates are called as primitive gates. The quantum cost pertains to the cost of the circuit in terms of the cost of 1×1 and 2×2 primitive reversible gates.

Total Logical calculations: The total logical calculations is another term in reversible logic, which indicates the number of XORs, NOTs and ANDs in the circuit. Total logical calculations can be given as; $L = \alpha + \beta + \delta$, where α = number of XORs, β = number of ANDs and δ = number of NOTs.

Ancillary Inputs: Ancillary inputs are the constant inputs can be described as the inputs to be retained at constant value

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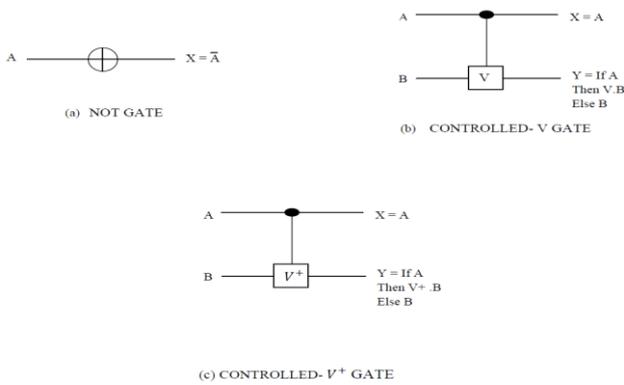


Figure 1. Primitive Reversible gates

of '0' or '1' in order to generate the given logical function.

Garbage outputs : The garbage outputs are the additional outputs in the reversible logic circuit that maintain the reversibility but do not perform any useful operation. The following formula shows relation between garbage output and the ancillary inputs;

Input (n) + Ancillary Inputs (0/1) = Output (k) + Garbage Outputs.

B. Reversible Logic Gates

In reversible logic gates the number of inputs (n) is equal to number of outputs (k). There is unique relationship between inputs and outputs of reversible logic, so that inputs can also be derived from the outputs.

NOT Gate: NOT gate is simplest 1x1 primitive logic gate. The quantum cost of NOT gate is zero [10].

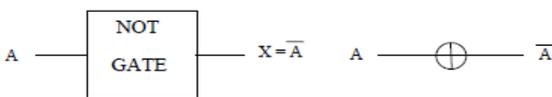


Figure 2 . NOT gate and its quantum representation

CNOT Gate: Feynman gate is 2x2 reversible CNOT (Controlled NOT) gate [14].It is widely used as fan-out purposes.

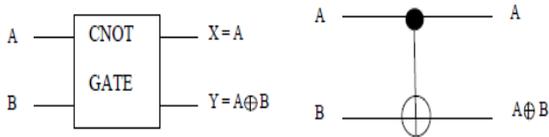


Figure 3. CNOT gate and its quantum representation

Quantum cost for Feynman gate is 1.

CCNOT Gate: Toffoli Gate is called as CCNOT (Controlled Controlled NOT) gate is a 3x3 reversible gate [14]. CCNOT gate is a universal reversible gate i.e. any reversible logic circuit can be constructed by a finite number of CCNOT gates. Quantum Cost for CCNOT gate is 5.

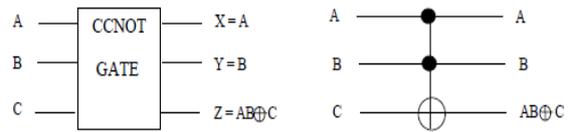


Figure 4. CCNOT gate and its quantum representation

PERES Gate: Peres gate is a new 3x3 Toffoli / CCNOT gate [15]. We can create Peres gate by combining Toffoli / CCNOT gate and Feynman/ CNOT gate.

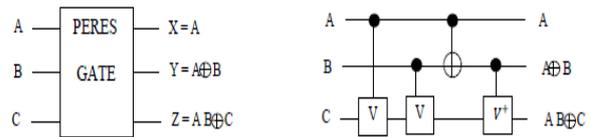


Figure 5. PERES gate and its quantum representation

Quantum Cost for Peres gate is 4. Due to less quantum cost, it is used to implement several logic functions. Peres gate can be used as half adder, if we give 0 to the third input of Peres gate (C=0).Furthermore, this gate can be used as two-input AND gate.

TSG Gate: TSG is a 4x4 reversible gate [3]. The TSG gate is capable of implementing all Boolean functions and popularly used to construct the full-adder circuit. Quantum cost of TSG gate is 14. The output expressions of the TSG gate are rather complex and require large quantum cost to realize it.

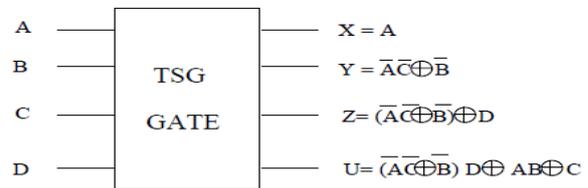


Figure 6.TSG gate and its quantum representation

MTSG Gate: MTSG is a modified 4x4 reversible TSG gate [21]. The MTSG generates very simple output conserving the reversibility logic property. By providing '0' at the D input, we can easily realize the full-adder from

MTSG.

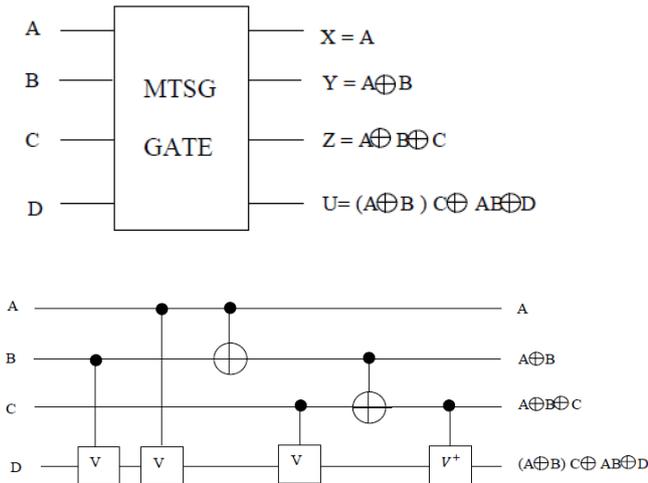
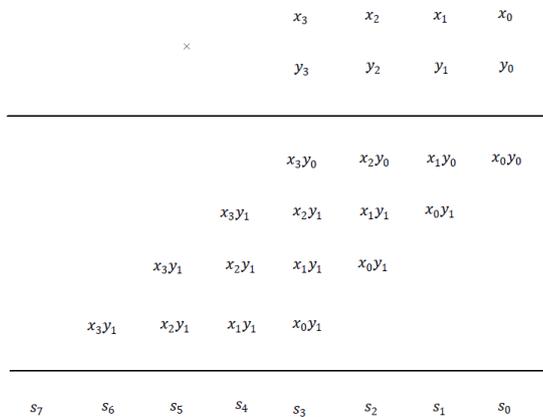


Figure 7. MTSG gate and its quantum representation

The quantum cost of MTSG gate is 6, which is minimum quantum cost to realize full adder. MTSG is very efficient to design reversible circuits as the quantum cost of the MTSG is very low as compared to the TSG gate.

III. OUR PROFOUND REVERSIBLE MULTIPLIER CIRCUIT

In this paper, we have used the reversible Peres and MTSG gates to compute the product of two 4×4 bit binary numbers. The multiplication of two 4×4 bit binary numbers is shown in Fig. 8.



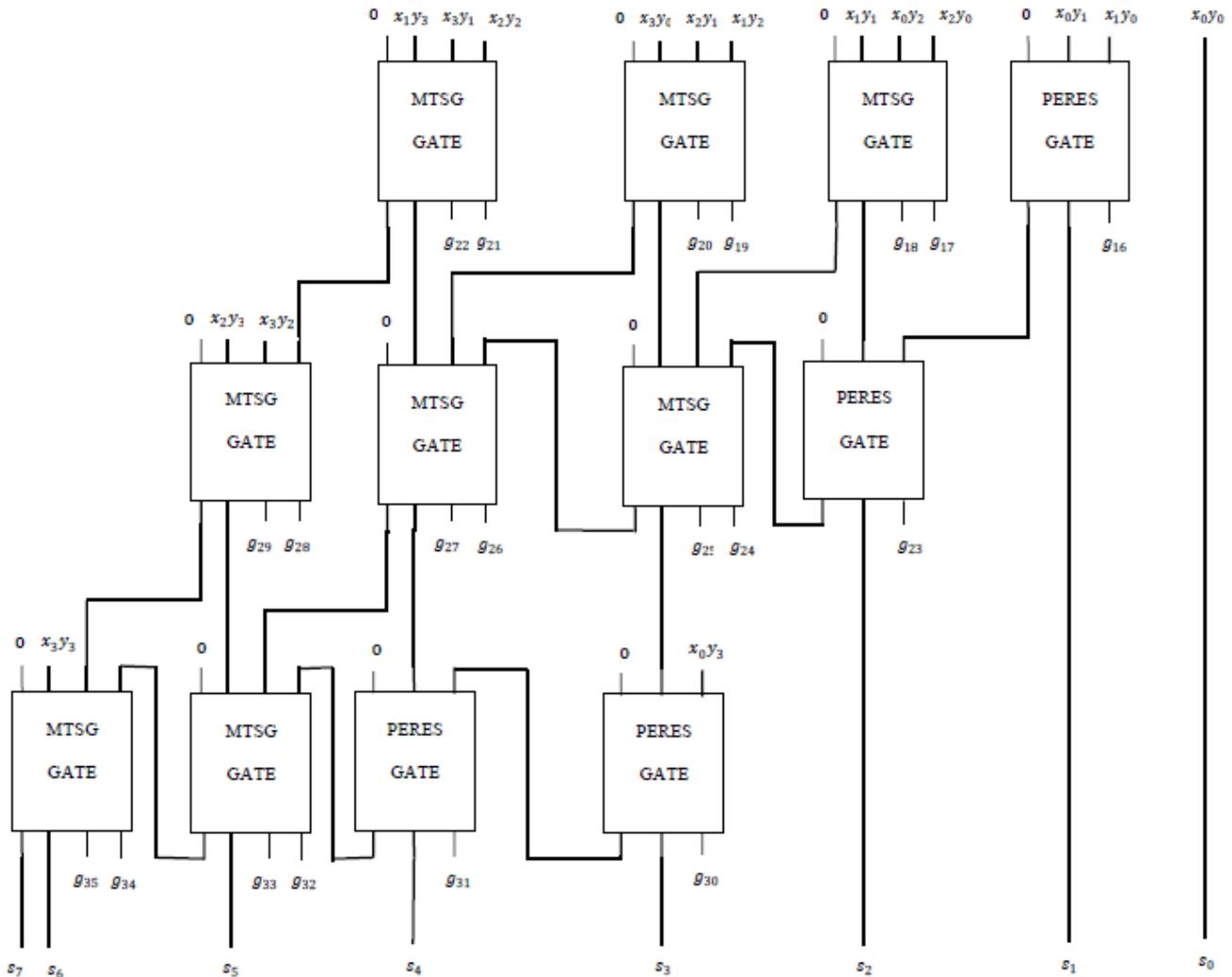


Figure 10. Adder Design with partial product resources

IV. EVALUATION OF REVERSIBLE MULTIPLIER CIRCUIT

The proposed multiplier circuit is more efficient than the existing circuits [4,5,7,8,10,20] in terms of Quantum Cost. Total Quantum cost is one of the main factors in designing the reversible logic, as it acts as important measure of merit to evaluate a reversible logic circuit. The total quantum cost of our proposed design is 128, but the total quantum cost of the existing design in [5] is 234, the total quantum cost of existing design in [7] is 168, the total quantum cost of [10] is 136. So, we can state that our proposed design is also better than all existing designs in term of quantum cost up till now. Proposed circuit of this study has a better quality than the reversible multiplier circuits presented in [10].

V. RESULTS

We have designed and analyzed the reversible multiplier with the PG gate and MTSG gate in VHDL language. Performance with other predesigned multipliers has been compared on the basis of quantum cost.

A. Simulation Result For Reversible Multiplier

Figure shows the simulation results for multiplier using Reversible logic. Here in the following example, the

multiplicand is 1001 and multiplier is 1010. The Output of multiplier is 10010000.

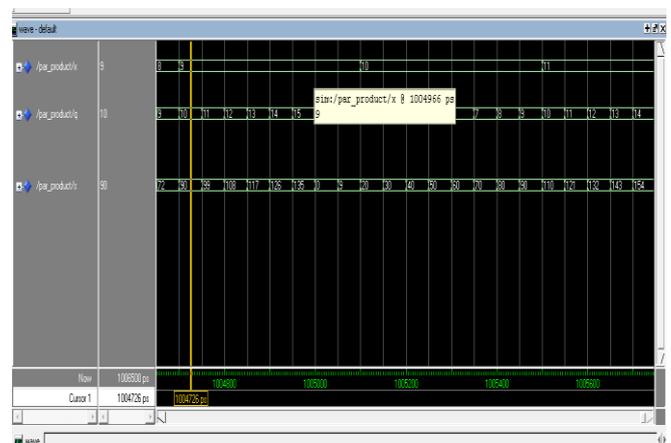


Figure. 11 Simulation diagram of Reversible Multiplier

Fig. 11 shows simulation of reversible multiplier using VHDL programming in Model SIM tool.

VI. CONCLUSION

Multiplication is a fundamental operation in most of the signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore, reversible multiplier design is preferable in low power dissipation VLSI system design. In this paper, we proposed an improved design of 4×4 reversible multiplier using Peres gate and MTSG gate. The performance has been compared on the basis of Quantum Cost. Total Quantum cost of our proposed design is 128, but the total quantum cost of the existing design in [10] is 136. So, the percentage reduction of Quantum cost is 5.88%. So, we can state that our new design is better than all the existing designs in term of quantum cost which is an important measure of merit to evaluate the reversible logic design.

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