Design of a Power efficient Reversible Adder/Subtractor

Harpreet Singh **Chakshu Goel**

***Abstract*— Quantum Computing has emerged as a futuristic form of computing using reversible logic as its basis. Apart from quantum computing, Reversible logic and its logic synthesis has been receiving considerable applause in applications such as low power CMOS design, nanotechnology, DNA computing and optical computing also. This paper propounds an optimised reversible full adder-subtractor design called "WG gate". Design of reversible gates is improved by reducing its parameters like quantum cost, garbage outputs, etc. but this proposed gate is optimised in terms of quantum cost and can be used in various adder-subtractor circuits. Although this paper supplies only an elementary component used to perform arithmetic addition and subtraction, yet more complicated circuits can be built using the reversible logic.**

***Index Terms*—Quantum Computing, Reversible Logic, Logic Synthesis, Quantum Cost, garbage outputs.**

I. INTRODUCTION

Quantum computing has offered a new research aspect to the VLSI technology. As more and more gates and transistors are being fabricated on the same integrated circuit chip, power dissipation becomes a major factor concerning the performance of the integrated circuit. However, power dissipation does not alter the operation of given circuit but do deteriorates speed and lifetime of the given circuit. Power dissipation can be coped up by using an extra circuitry that can be used for lowering down the temperature of the circuit and evacuating the radiated heat. This solution increases the complexity and burden of maintaining extra equipment on the circuit. A novel approach deals with reduction in power dissipation rather than encountering it. Reduction in power dissipation can be achieved by using quantum circuits based on reversible logic. This clarification requires understanding of quantum circuits and reversible logic.

A quantum circuit consists of quantum gates and their interconnections [1]. Quantum gates operate on quantum bits (qubits) as opposed to binary digits (bits) in conventional digital computing which makes its operands different from any other conventional circuit. Also, a qubit can hold more information than a bit [1]. A bit has only two states 0 and 1 while a qubit can be a linear relation of two states basis binary $|0\rangle$ and basis binary $|1\rangle$ denoted as $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$. In case of qubits used in reversible logic, we are solely dependent upon orthogonal states of $|0\rangle$ and $|1\rangle$ having probability $|\alpha|^2$ and $|\beta|^2$ respectively avoiding the use of entangled states. Thus, a qubit will hold the same amount of information as a bit.

Furthermore, an irreversible process can be defined as a process in which cannot be inverted back with time i.e. output states at a particular time are unable to describe the true input states. According to the R. Landeuer [2, 3], there is a finite amount of energy dissipated as heat in case of every irreversible process. This finite energy aforementioned can be described as kTln2 joules, where k (Boltzmann Constant) $=1.38 \times 10^{-23}\ m^2 kgs^{-2}K^{-1}$, T is the temperature in kelvin (K). This energy dissipated per unit time increases as the number of transistors in an integrated circuit increases since each bit loss comprises of energy loss. Ideally, for a reversible process in which there is no bit loss, zero power dissipation is achieved [4]. Considering the statement of Gordon E. Moore, the number of transistors on an integrated circuit will double every two years [5]. There must be an upper limit on the number of transistors that can be lithographically possible on a single chip. Single atom transistor, developed at the Karlsruhe Institute of Germany, gets the Moore's prediction to be concluded [6].

Reversible logic is the unconventional logic usually working on the guidelines of conventional digital logic but with lesser power dissipation, as much as half of the dissipated power can be reduced. Ideally, a process is said to be reversible if it is physically and logically reversed with the course of time. Commenting on physical reversibility of a process, it means there should be no rise in entropy after the completion of the process and on its logical counterpart, the process turns out to be an injective function i.e. inputs can be uniquely derived back from the outputs [4].

In digital electronics, the adder-subtractor is a standalone binary circuit capable of performing both arithmetic operations of addition and subtraction using an input as a control signal. The circuit can also be implemented for its working as adder and subtractor at the same time. Various reversible adder-subtractor designs are proposed in the existing papers [7-9]. The circuits proposed in these preceding efforts utilised more number of gates, generated more garbage outputs and returned high quantum cost. However, the existing design yielded the optimal results for garbage outputs, number of gates and ancillary inputs but the design can be improved in terms of quantum cost, which is 8 according to the quantum representation shown in [11]. The

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proposed circuit can fulfil for its working as half adder, full adder, half subtractor and full subtractor.

II. REVERSIBLE LOGIC

Reversible Logic, as discussed before, works on achieving a process or computation that is actually reversible. This can be accomplished to make that process or computation thermodynamically and logically reversible. There is a criteria that satisfies whether the computational process is reversible or not. For a reversible process,

1. No fan-out is permitted.
2. Number of inputs should be equal to the number of outputs so that the mapping from inputs to outputs or outputs to inputs is one-to-one.
3. Closed loop or feedback is strictly prohibited.

Satisfying the above three arguments, Reversible gates can be made to satisfy for conventional digital requirements but with less, or ideally, no power dissipation. As an example, Reversible gates like Feynman Gate can be used as alternative for conventional XOR gate and Toffoli gate for conventional AND or NAND gate. There are parameters that describe a reversible circuit in terms of their complexity and speed. The definitions of these parameters are given below:

Quantum Cost: The quantum cost of an N × N (i.e. Number of inputs × Number of outputs) reversible gate is the number of 1×1 or 2×2 primitive gates used to model that reversible gate.

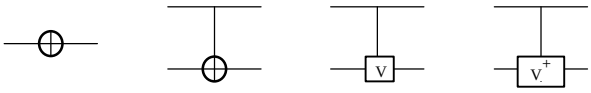

Figure 1. Elementary gates with quantum cost=1

Garbage Outputs: Since in reversible logic, number of outputs should be kept equal to number of inputs and number of outputs are normally less than the number of inputs, there is every possibility that the some of the outputs are not required in the process and are useless. Thus, an undesirable output may be termed as garbage output.

Ancillary Or Constant Inputs: Sometimes mapping the inputs to outputs must not be unique, thus ancillary inputs must be added in order to synthesize a given function.

Delay: The delay in a reversible circuit is counted as the maximum number of gates encountered while passing through any input to an output.

Total logical calculations: Arithmetic sum of the number of XOR calculations, AND calculations and NOT calculations is defined as the total logical calculations taken by the reversible circuit to implement a Boolean expression.

Proposed designs of reversible gates for various logical operations can be found in literature like Reversible NOT gate, Feynman gate, Toffoli gate, Fredkin gate, Peres gate, MKG gate, TSG gate, HNG gate [10].

Reversible NOT gate: This gate is 1×1 gate which outputs the complement of its input. It is the only conventional gate having the characteristics to work as a reversible gate.

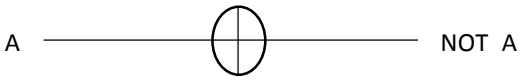

Figure 2. Quantum Representation of NOT gate

Feynman Gate: This gate is a 2×2 reversible quantum gate can be used as an alternative to conventional XOR gate. This gate outputs the exclusive-OR of its two inputs while the second output is a one-through signal.

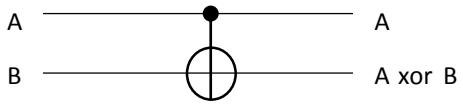

Figure 3. Quantum Representation of Feynman gate

Toffoli Gate: The Tofolli gate is an alternative to conventional AND gate when control input of this gate is set to logic 0 and conventional NAND gate when set to logic 1.

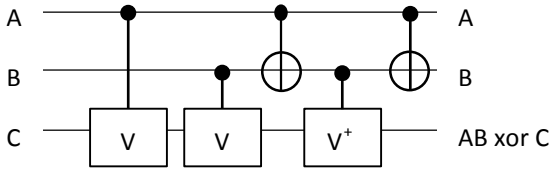

Figure 4. Quantum Representation of Toffoli gate

Fredkin Gate: This 3×3 gate performs a controlled-swap operation. To illustrate, when the control input (in this case, A) is low then B and C are passed as it is but when the control input is high then B and C swap places at the output.

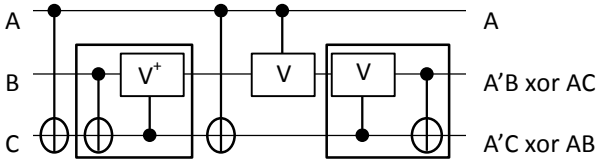

Figure 5. Quantum Representation of Fredkin gate

Peres Gate: This 3×3 gate provides an alternative to toffoli gate for providing AND and NAND output but with a unit less of quantum cost i.e. 4.

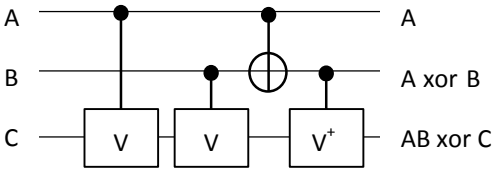

Figure 6. Quantum Representation of Peres gate

MKG Gate: This gate is a 4×4 reversible gate can work singly as a full adder with control input (in this case, D) equals logic 0.

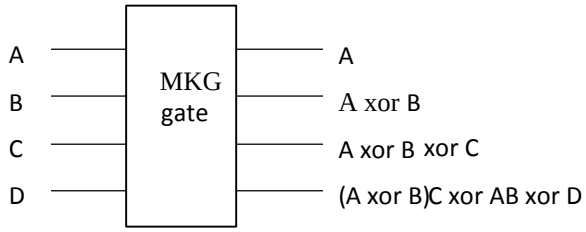

Figure 7. Block Diagram of MKG gate

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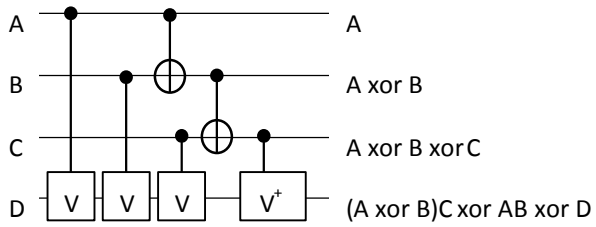

Figure 8. Quantum Representation of MKG gate

III. PROPOSED WORK

This paper propounds a reversible adder-subtractor design which can singly work as a full adder and full subtractor using a control input. Needless to say that the design can also work as half adder and half subtractor as well. The design illustrates a 4×4 WG gate which is optimised in terms of quantum cost. The WG gate, shown in figure 2, has D as its control input and A, B, C being the three adder inputs.

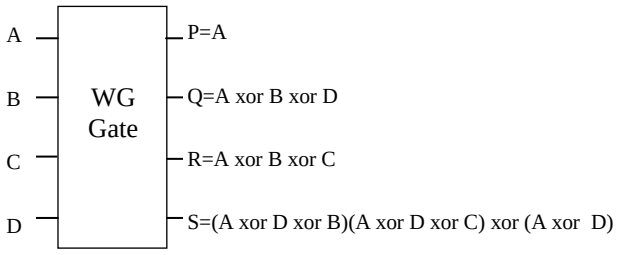

Figure 9. Proposed Reversible WG gate

Besides, the WG gate is also a universal gate i.e. basic gates like AND, OR and NOT can be constructed from the use of a single instance of it.

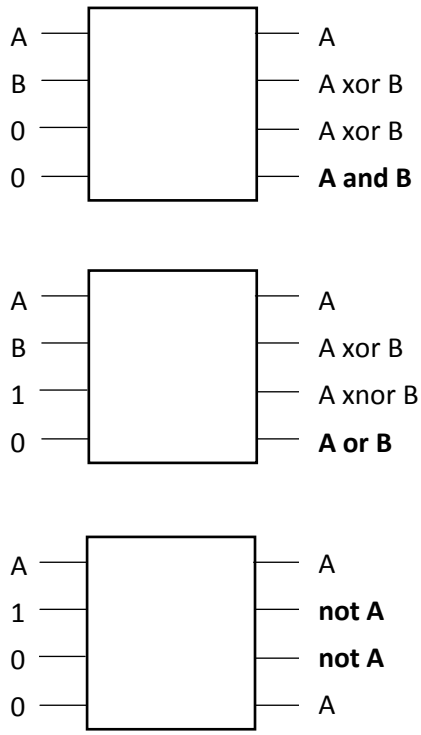

Figure 10. Reversible WG gate working as Universal gate

WG gate as Reversible Full adder: WG gate can work individually as a full adder by setting the control input (in this case, 'D') to logic '0'. In this case,

P= A Q= Carry Propagate
R= Sum S= Carry

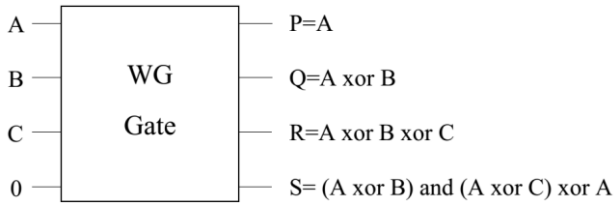

Figure 11. WG gate as reversible full adder

WG gate as Reversible Full subtractor: WG gate can work as a full subtractor by setting the control input (in this case, 'D') to logic '1'.

In the case of Reversible WG gate as full subtractor, the outputs depicts the following:

P= A Q= Borrow Propagate
R= Difference S= Borrow

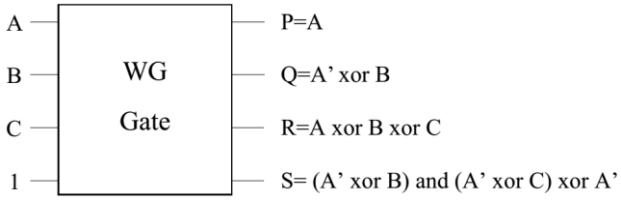

Figure 12. WG gate as reversible full subtractor

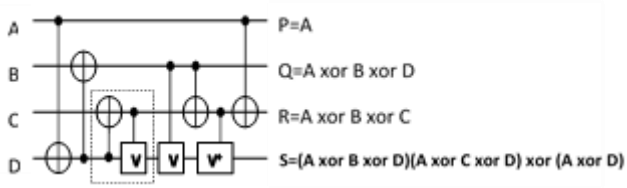

Figure 13. Quantum Representation of WG gate

IV. SIMULATION ANALYSIS

The design was tested for its working in VHDL form as a full adder/subtractor on Spartan3E-XC3S100E in Xilinx ISE 12.4 environment with a speed grade of -4. The simulation was done with an integrated Modelsim-SE 6.2c. Given below are the waveforms for working of WG gate as both full adder and full subtractor using D as control input. Figure 14 and 15 depicts the simulation of the design as full adder and full subtractor respectively.

V. COMPARISON AND RESULTS

The existing designs [7-9, 11] are compared for their design parameters as single-bit full adder/subtractor with the proposed design in this section. The proposed design use less or equal resources for every parameter described.

It is seen from the aforementioned quantum representation that the quantum cost of WG gate is 7. This cost shows an improvement of 12.5% from the compared best of ZRQG gate

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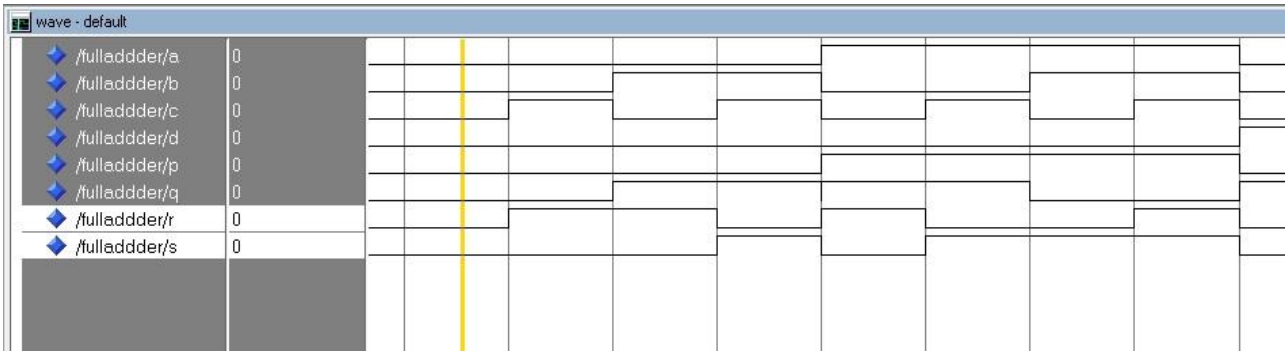

Figure 14. Simulation of WG gate as full adder with control input D=0

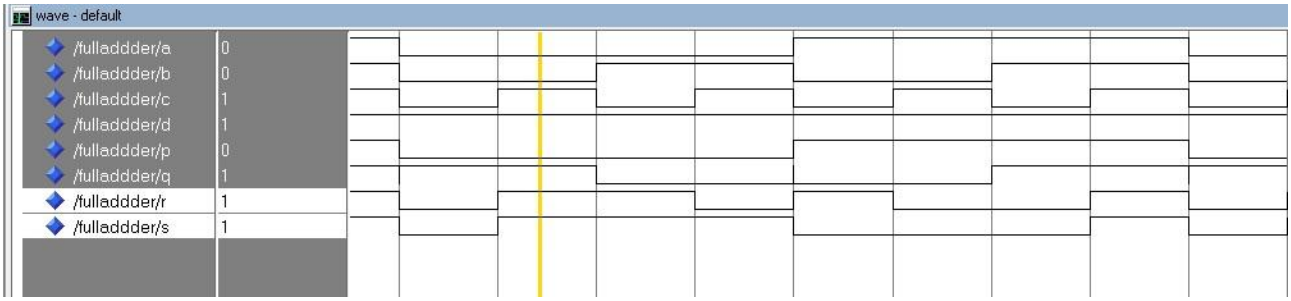

Figure 15. Simulation of WG gate as full subtractor with control input D=1

whose quantum cost is given to be 8 [11]. Moreover, this gate does not require any ancillary inputs and yields two garbage outputs. This is the least number of garbage outputs required to make a full adder as shown in [12].

TABLE I. COMPARISON OF VARIOUS FULL ADDER/SUBTRACTOR DESIGNS

Designs	Quantum Cost	Delay	Number of gates	Garbage outputs	Ancillary inputs
Existing design[7]	21	5	8	5	3
Existing design[8]	30	7	9	11	9
Existing design[9]	9	3	3	2	1
ZRQG gate[11]	8	1	1	2	0
Proposed WG gate	7	1	1	2	0

VI. CONCLUSION

The design proposed here is a computational model related to quantum computing in which subatomic particles are used to perform computations with the help of quantum physics. The reversible logic is used in computing because of its low power dissipation. Evidently, a reversible circuit will be power efficient than a conventional digital circuit. Although, there are parameters of quantum reversible logic which need to be taken care of. The improvement in elementary parameters is worked upon in the modern research. In the proposed work, out of all elementary parameters, the parameter termed as quantum cost is reduced by generating a design which uses less number of elementary gates and resulting in a quantum cost of 7, compared with the quantum cost of 8 achieved in the existing work [11].

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