# Performance Enhancement Guaranteed Cache Using STT-RAM Technology

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**Abstract- Spin Transfer Torque RAM (STT-RAM) is a form of computer data storage which allows data items to read and write faster. Every peripheral circuit have some static power consumption, which is consumed while there is no circuit activity. The main objective of the paper is to reduce the static power consumption in peripheral circuits with the help of STT-RAM technology. Instead of fetching instructions from main memory (L1 instruction cache) a tiny buffer called loop cache is used to serve instructions to the processor, in order to save power. The efficient power down strategy and non- volatility of STT-RAM combined with the loop caches, leads to reduced power consumption. Further to increase the efficiency of the system Performance Enhancement Guaranteed (PEG) cache is encapsulated with the STT-RAM technology.**

***Keywords*—Spin-Transfer Torque RAM (STT-RAM), Caches, instruction caches, loop caches.**

## I. INTRODUCTION

Spin Transfer Torque RAM is an advanced technique which is used to consume less power. Compared to SRAM (Static RAM), STT-RAM has characteristics such as short read time, low leakage power, high density, good compatibility etc. In the STT-RAM technology whenever a program is not running or idle it automatically switches off the power supply to the processor. This leads to the reduced energy consumption. SRAM is a form of semiconductor memory which uses bistable latching circuitry to store each bit [4]. Because of its volatile nature the data is eventually lost when the memory is not powered. To retain the memory and to reduce the power consumption STT- RAM technology is used, as it is an effect in which the orientation of a magnetic layer in a magnetic tunnel junction can be modified using spin polarized current.

STT-RAM is capable of replacing SRAM as last level on chip cache [3]. It is a greatest achievement in magnetic storage from hard disk drives to solid state semiconductor memory [2]. The critical component of many VLSI chip is low power SRAM. Because of large fraction of total power and die area in high performance processor, low power SRAM design is difficult to achieve [4]. The computing system performances affect the read and write speed of cache memories. Because of its large write energy consumption, the dynamic power consumption of STT-RAM L2 cache is much higher than SRAM L2 cache [1]. DRAM has low capacity and high cost benefits compared to STT-RAM [6]. To bridge the performance and power gap between the processor and memory, large last level caches are introduced [5]. Instead of using embedded DRAM or conventional SRAM, the STT-RAM technology is used to achieve reduced chip size and low energy requirements of L3 cache. With the help of Magnetic Tunnel Junction STT-RAM cell is used to store binary data [7]. In order to increase the data execution speed cache memory is kept between processor and RAM. Among the three level caches, L1 cache is the fastest cache and it comes within the processor itself [6]. L1 instruction caches are built using High-performance (HP) cells in order to achieve low access latency whereas L2 caches use low power (LP) cells at a cost of high static power consumption. Due to this, static power of L1 instruction caches is higher than that of L2 caches, and also L2 cache is larger than the primary cache. L3 cache is not at all used nowadays because its function is replaced by L2 cache. Rather than processor L3 caches are found on the motherboard and it is kept between L2 cache and RAM.

## III. LOOP AWARE SLEEPY INSTRUCTION CACHE CONTROLLER

Fig 1 shows the illustration of the architecture. This project is mainly designed to reduce the static power consumption in peripheral circuits based on STT-RAM technology. There are two types of caches; instruction cache and data cache where STT-RAM takes care of instruction cache and data cache are left ideal. Static RAM cache called loop cache which is between the processor and L1 instruction cache. This is used to store the temporary data. The instructions are fetched to the L1 instruction cache and it serves to the processor. L1 instruction cache acts as a main memory. The instructions which are used repeatedly are saved in the loop cache. This enables the opportunity to turn off the L1 instruction cache while the loop cache is operating.

### *A. L1 Instruction Cache*

Cache memory is a high speed memory and it is an area of a computer memory which is used for temporary storage of data and can be accessed more quickly than the main memory and also it comes between processor and RAM to increase the data execution speed. There are three types of cache memory (L1, L2 and L3). Among the three types of cache L1 instruction cache is the fastest cache and



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it comes with the processor chip itself. To achieve low access latency, L1 instruction caches are constructed using high performance cells [2]. The instructions are fetched to the L1 instruction cache then it is served to the processor.

*A. Loop Cache*

Loop cache is a tiny buffer which is used for storing temporary instructions. The cache is the fastest and smallest memory which is capable of storing the copies of the data from the frequently used main memory (L1 Instruction cache). The instructions are fetched from the main memory to the loop cache.

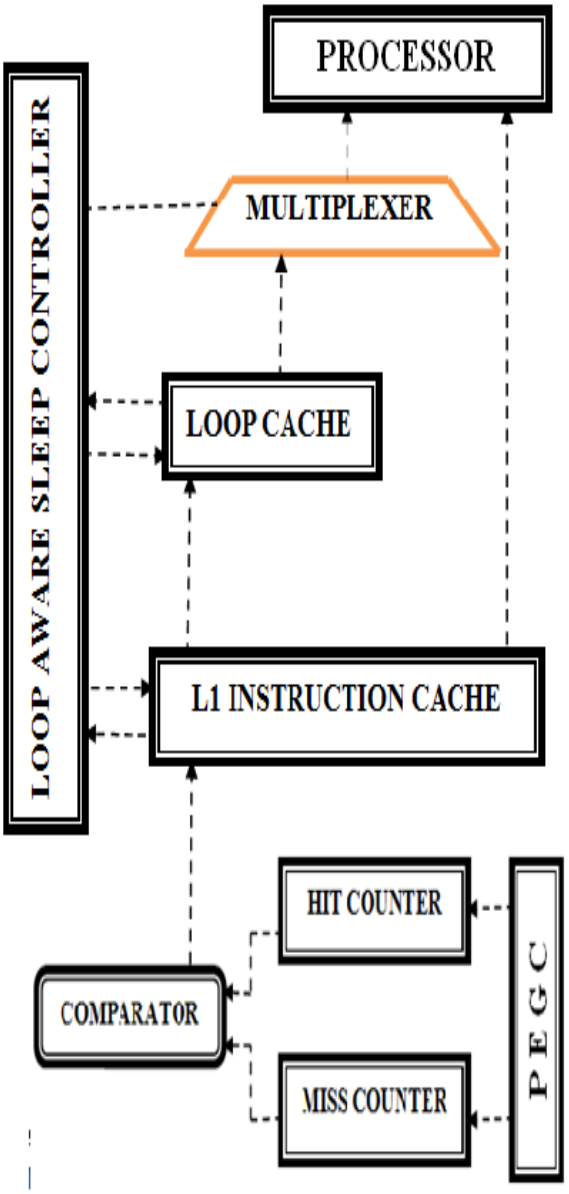


*Fig 1 PEG Cache*

When the loop cache is being accessed, the loop aware sleep controller checks whether the requested address is located inside the program (data provided by the user).If so, the data corresponding to that address is read to check for the data hit and in case if any data miss it is loaded from the L1 Instruction cache.

*1) Standby Mode:* Instructions are taken from the L1 instruction cache and the loop cache is not used in the standby mode. The controller detects the trigger branches and switches to fill state.

*2) Fill Mode:* In fill state, L1 instruction cache still supplies instructions to the processor, but every fetched instruction is also given to the loop cache. The controller checks for the trigger branches, when the trigger branch is taken again, it changes the state to active now the loop cache is ready to use.

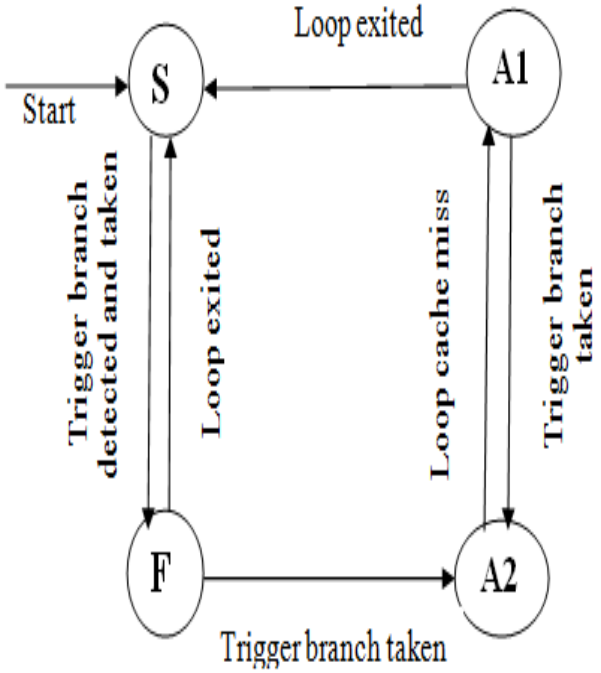


*Fig 2. State diagram of loop aware sleep controller*

*3)Active Mode:* Finally in the active state, the instructions are served to the processor by the loop cache; in the meanwhile the L1 instruction cache can be turned off completely, which means in active state (A2). In case of any problem in the loop cache or loop cache misses, to load the corresponding block from it the L1 instruction cache is powered up by the controller (A1). This case could occur when the control-dependent code in the loop which is not executed. In this situation, the corresponding block is loaded from the L1 instruction cache which is powered by the controller. In order to reduce the static energy consumption the L1 instruction is it is turned off again after the iteration.

The active state consumes the least power, among all the three loop cache states. In the active state through power off instruction caches, the static power and dynamic power is reduced by the less energy access of loop cache in the active state compared to the L1 instruction cache.


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Because of the write energy of loop cache the fill state consumes slightly more dynamic power than the standby state. However the dynamic energy consumption is not considered in this project.

*B.PEG-C Architecture*

PEG-C: Performance Enhancement Guaranteed Cache is used to enhance the performance even in the worst case, without using any cache. The cache hits due to performance enhancement is always more than the cache miss due to performance degradation.

The PEG-C consists of a regular hardware-controlled cache, with two hardware extensions. To monitor the number of cache misses and cache hits two counters are used. Hit counter (HC) and the miss counter (MC) to count the number of cache hits and the number of cache misses respectively. First of all both the counters are reset to zero. The Hit Counter will be increased by one when there is a cache hit. Similarly and if there is a cache miss the Miss Counter will be increased by one. A comparator is designed to compare the values of HC and MC. Based on the HC value, if MC reaches its maximal value the PEG-C will be disabled immediately. This is called *PEG-C Throttling*. Each instruction or data access has to go to the main memory after the PEG-C throttling considering there is no PEG cache. Due to the efficient reuse of the cache space, PEG-C can achieve better performance. So it is desirable for hard real-time systems, non real-time systems and mixed real-time. To dynamically cache instructions PEG-C can be used as a regular cache this leads to good average-case performance.

## IV. SIMULATION RESULTS

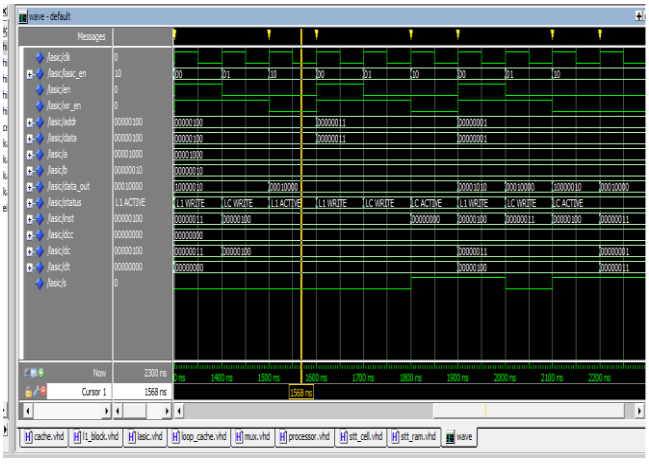

*Fig 3. Simulation result of LASIC block*

*A. LASIC Block*

Compared to the STT-RAM, SRAM has longer write latency, has higher density and also low leakage power. The instructions are fetched to the main memory (L1 instruction cache). These instructions are stored under an 8 bit address. If the address is less than or equal to 3, then the instructions are served from the loop cache to the processor otherwise L1 instruction cache serves the instruction to the processor. In fig 4 the data is stored in the address 4. According to this instruction is served from the L1 instruction cache to the processor. The inputs given to the processor are **a** (00001000) & **b** (00000010). Operations are performed according to the address in which data's are stored.

*B. PEG Block*

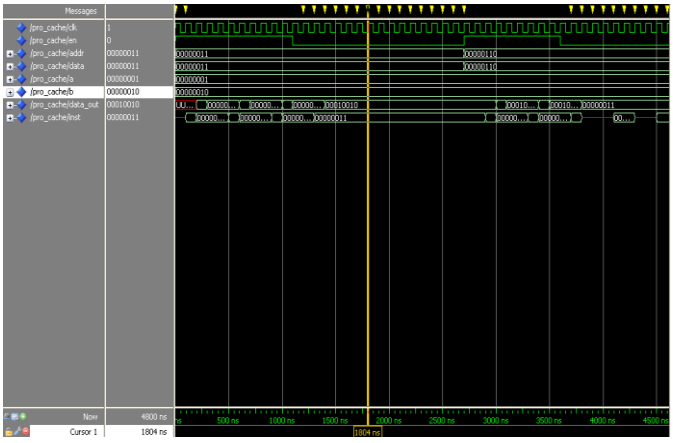

*Fig 4. Simulation results of PEG block*

Increased number of cache miss results in PEG throttling, so the comparator checks for the cache miss, if it reaches the high value compared to that of the cache hit, throttling signal is enabled, immediately PEG cache is disabled and the instructions are served to the processor from main memory. This leads to increased efficiency and low power consumption. The instruction which is missed can retrieve easily.

*C.Power Report*

The power analysis for Static RAM and STT-RAM is given below, whereas SRAM consumes (49 mW) and STT-RAM consumes (47 mW).

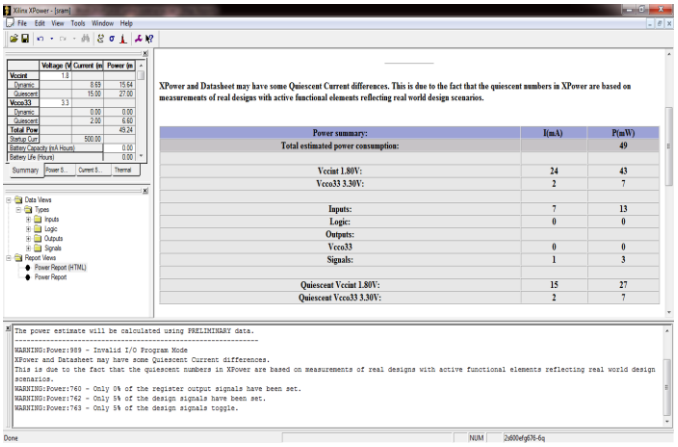

*Fig 5. SRAM*



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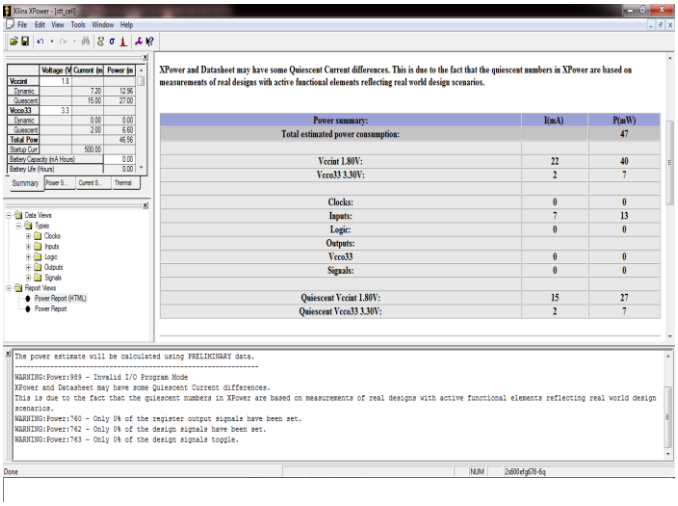


*Fig 6. STT-RAM*

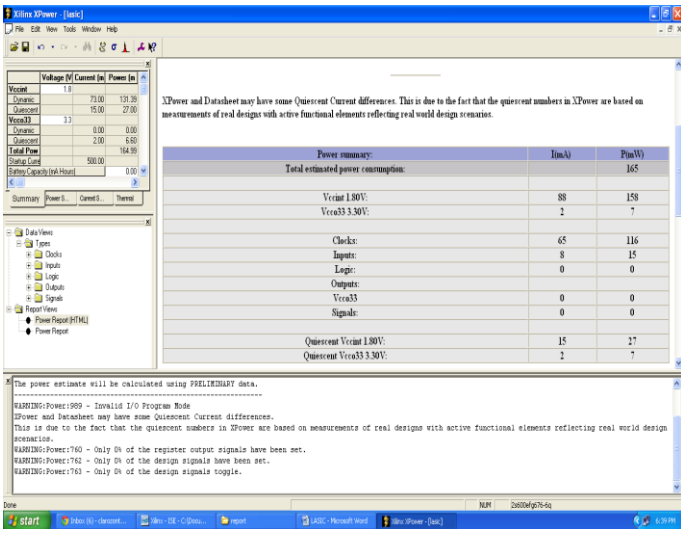


*Fig 7. LASIC*

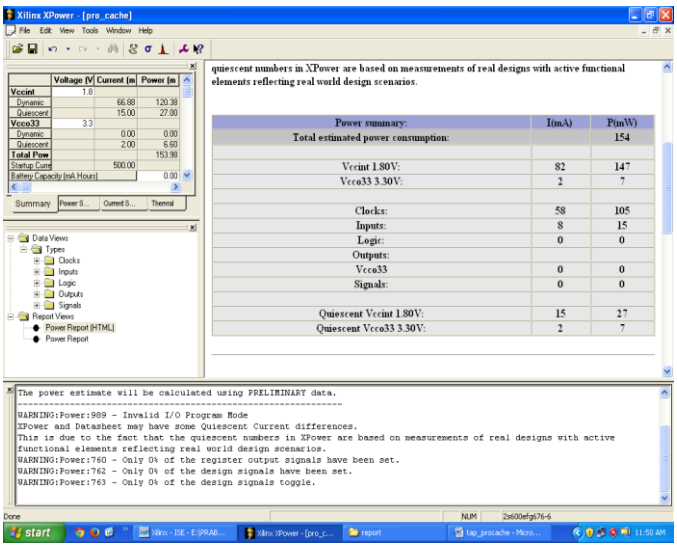


*Fig 8. PEG CACHE*

TABLE I

COMPARISION TABLE

| Methods Used | Power(mW) |
|---|---|
| **SRAM** | 49 |
| **STT-RAM** | 47 |

TABLE II

| Methods Used | Power(mW) |
|---|---|
| **LASIC** | 165 |
| **PEG CACHE** | 154 |

## V. CONCLUSION

The simple architecture of Spin Transfer Torque - Performance Enhancement Guaranteed Cache is presented. This PEG cache gives better predictability, reduced energy consumption and increased efficiency. Likewise it reduces the static energy consumption of STT-RAM instruction caches. The improved loop caches supports all kind of loops, and based on it, controlled sleep mode power-gated L1 instruction cache is constructed. Finally this architecture achieves low power consumption with the use of STT-RAM technology.

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