FPGA Implementation of High Resolution All-Digital Duty Cycle Corrector Using NAND Based Logic

Mrs.S.V.KIRUTHIKA[1], Dr.R.SUDARMANI[2]

Abstract—**The positive and negative edges of the system clock are utilized for data sampling in high speed applications. Thus, the system required an exact 50% duty cycle for input clock. In this paper, a wide-range all-digital duty-cycle corrector (ADDCCs) is presented. A high-resolution ADDCC (HR-ADDCC) is used to obtain an exact 50% output duty cycle with short locking time, without using a half cycle delay line. Experimental results show that the frequency range of the proposed ADDC is 250-1 MHz with DCC resolution is 5-8 ns. In addition, the proposed HR-ADDCC is used to reduce the circuit complexity and leakage power in advanced process technologies and also it is very suitable for system-on-chip applications.**

Keywords—**All-digital duty-cycle corrector (ADDCC), digitally controlled delay line(DCDL), duty cycle corrector (DCC), delay locked loop (DLL).**

I.INTRODUCTION

Variation in voltage and temperature, the rise and fall time of the clock buffer get unbalanced. Require an exact 50% of the clock signal, the duty cycle is corrected. Because the positive and negative edges of the clock are utilized for sampling the input data in high speed data transmission application such as double data rate memories (DDRM), double sampling analog to digital convertor(ADC) and System-on-Chip(SoC) application. Several approaches are available to correct the duty cycle error in both analog and digital. In digital, has less sensitivity, fast locking time and low jitter performance compared to analog. Hence, theall-digital duty cycle corrector (ADDCC) is proposed.

The rest of this paper is organized as follows.Section II explains with the existing work.The proposed ADDCC system architecture is presented in Section III.Section IV describes the circuit implementation of the proposed designs.Section V shows the simulation results of the HR-ADDCC. Finally, the conclusion is given in Section VI.

II. EXISTING WORK

In high resolution ADDCC (HR-ADDCC) consists of a two blocks such as Duty cycle corrector (DCC) and Delay locked loop (DLL). The DCC and DLL blocks can also have inbuilt phasedetector (PD), digitally controlled delay line (DCDL), and control signal. The phase detector is used to detect the phase error between the DLL_CLK and CLK_IN.Depending upon the phase detector output the DCDL can add or remove delay to the input clock signal (CLK_IN).

The DLL align the positive phase of the input clock signal. If the positive phase isaligned, then the DLL get locked. After DLL locking condition, the DCC has to perform the aligning of the negative clock signal. If the negative phase gets aligned, then the DCC get locked.

In this system, a multiplexer based coarse tuning element is used, which can improve the accuracy of the duty cycle correction, but the leakage power and the chip area is more.

To overcome this problem a NAND based DCDL is proposed to reduce leakage power, and to get low area, also the accuracy of the duty cycle correction has improved.

III. PROPOSED WORK

The block diagram of the proposed NAND based high resolution ADDCC (HR-ADDCC) is shown in the Fig.1. Initially, the clock input (CLK_IN) signal is given to the DCC delay line circuit and it produces the output as X signal, then the inverted X signal is passed to the DLL delay line which gives the output signal as Y.

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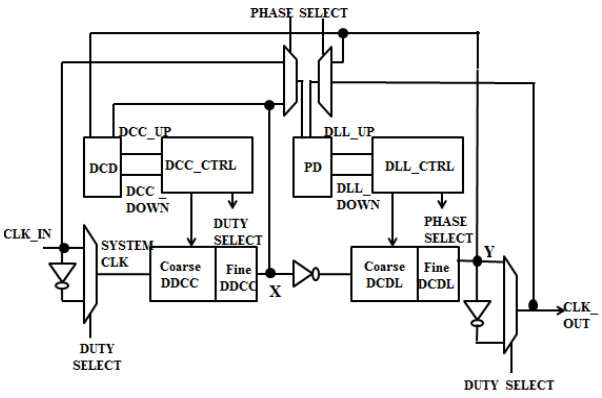

Fig.1 Block Diagram HR-ADDCC

The positive phase of both the X and Y signals are given to the phase detector circuit, it compares the signal and produces the phase error between the two signals (X and Y) as output. Depending upon the signal the DLL_CTRL can adjust the DLL_CODE. If the phase error between the X and Y signal is eliminated then the DLL is locked.

After the DLL is locked. The DCC start to compensate the duty cycle error of the output clock (CLK_OUT) signal. The DCD detects the phase error between the negative phases of the X and Y signals and it produce the output as DCC_UP or DCC_DOWN. The control signal(DCC_CTRL) adjusts the DDCC_CODE according to the outputs of the DCD. Both the positive and negative edge is aligned, and then the DCC is locked.

IV. CIRCUIT DESCRIPTION

A. Sample based Phase Detector

Phase detector is capable of detecting the phase difference between the reference clock signal and the delayed clock signal, and its output is applied to the control logic. Fig.2. shows the block diagram of the sampled-based phase detector (SMPD).

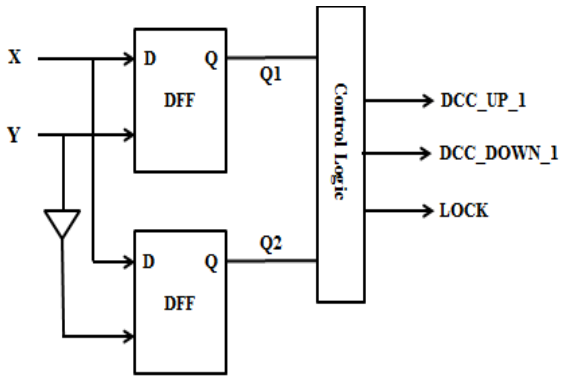

Fig.2 Sampled-based PD

In Fig.2, the two D flip–flops triggered by the clock rising edge which generates the reset signal when the outputs area high. To avoid the problem of a dead-zone band, a delay element is inserted. The output of the D flip-flops is given to the control logic.The comparator compares the input signal and produce the output as either Q1>Q2, Q1<Q2 or Q1=Q2. Table-1 shows the operation of the circuit to be performed.

TABLE-1

Q1	Q2	Action
0	0	Phase is equal
0	1	Add Delay
1	0	Remove Delay
1	1	Phase is equal

B. NAND based DCDL

Fig.3 shows the circuit diagram of the proposed glitch free NAND based DCDL. In these block four stages with two control signals are presented, which are named as T and S. Initially, T= 0 for all the three stages after 3ns delay both the control signal is applied to the fourth stage. Depending upon the fourth stage output the other three stages will operate and produce the glitches free stable output.

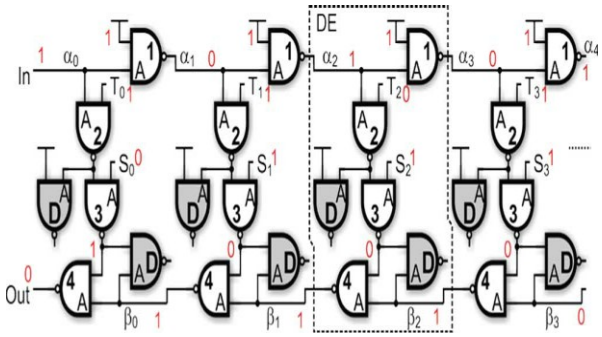

Fig.3 Proposed glitch free NAND based DCDL.

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V. RESULTS AND DISCUESSIONS

The simulation result of the proposed ADDCC is shown in the Fig. 4. The frequency range of the input clock is 250MHz to 1GHz, and the duty-cycle range of the input clock is from 30% to 70%. The power, area and delay between the two methods are compared and it is given in table- 2. Simulation results are based on Modelsim and power report is generated using Xilinx software.

TABLE- 2

Parameters	NAND based DCDL	MUX based DCDL
Total power consumption	32	39
Area	189 MB	220 MB
Delay	5.747 ns	8.941 ns

Fig.4 shows the simulation results for the proposed HR-ADDCC. If the RESET is enable there is no signal goes to the output clock (CLK_OUT). After some delay the RESET is disabled and the signal is flows through the circuit. The positive phase of the clock signal is aligned, the DLL is locked. The output waveform simulation result in DLL locking condition is shown in Fig.4(a).

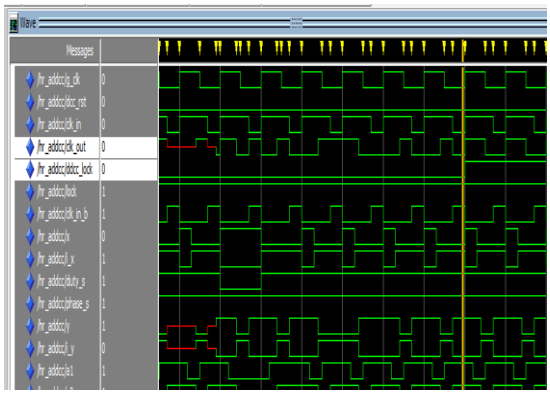

Fig.4(a) Simulation waveform of the DLL locked result

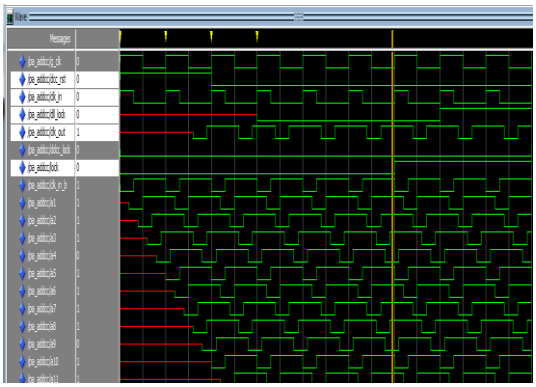

Fig.4(b)Simulation waveform of the Duty cycle correction output

The DCC starts to correct the duty cycle error. If the error is eliminated the DCC get locked and produce an exact 50% output duty cycle. The simulation waveform of the duty cycle correction output is shown in Fig.4(b).

VI. CONCLUSION

In this paper, a NAND based high resolution all-digital duty cycle correctoris presented. By using NAND based DCDL, without using a half cycle delay line a glitch free stable output is obtained. It achieves wide-ranges of operating frequencies and a wide-ranges of input duty-cycle. Furthermore, it reduces the leakage power and area. Thus, it is suitable for System-on-a-Chip (SoC) application.

REFERENCES

1. F. Mu and C. Svensson, “Pulsewidth control loop in high-speed CMOS clock buffers,” IEEE J. Solid-State Circuits, vol. 35, no. 2, pp. 134–141, Feb. 2000.
2. P.-H. Yang and J.-S. Wang, “Low-voltage pulsewidth control loops for SOC applications,” IEEE J. Solid-State Circuits, vol. 37, no. 10, pp. 1348–1351, Oct. 2002.
3. S.-R. Han and S.-I. Liu, “A 500-MHz-1.25-GHz fast-locking pulsewidthcontrol loop with presettable duty cycle,” IEEE J. Solid-State Circuits,vol. 39, no. 3, pp. 463–468, Oct. 2004.
4. K.-H. Cheng, C.-W.Su, and K.-F. Chang, “A high linearity, fast- locking pulsewidth control loop with digitally programmable duty cycle correction for wide range operation,” IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 399–413, Feb. 2008.
5. Y.-J. Wang, S.-K.Kao, and S.-I.Liu, “All-digital delay-locked loop/pulsewidth-control loop with adjustable duty cycles,” IEEE J. Solid- State Circuits, vol. 41, no. 6, pp. 1262–1274, Jun. 2006.

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