Low Power Truncated Binary Multiplier Using Replica Redundancy Block

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Abstract---A reliable low-power multiplier design by adopting algorithmic noise tolerant (ANT) architecture with truncated binary multiplier to build the fixed width reduced precision replica redundancy block (RPR). The ANT architecture can meet the high speed, low power, and area efficiency. To design the fixed-width RPR with error compensation circuit via analyzing of probability and statistics. Using this partial product terms of input correction vector and minor input correction vector to lower the truncation errors, the hardware complexity of error compensation circuit can be simplified.

Keywords -- Algorithmic noise tolerant (ANT), fixed-width multiplier, reduced-precision replica (RPR), and voltage over scaling (VOS).

I. INTRODUCTION

The ANT technique includes both main digital signal processor (MDSP) and error correction (EC) block, as shown in Fig. 1. [2]To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay T_{cp} of the system becomes greater than the sampling period T_{samp}, the soft errors will occur. It leads to severe degradation in signal precision. In the ANT technique, a replica of the MDSP but with reduced precision operands and shorter computation delay is used as EC block.

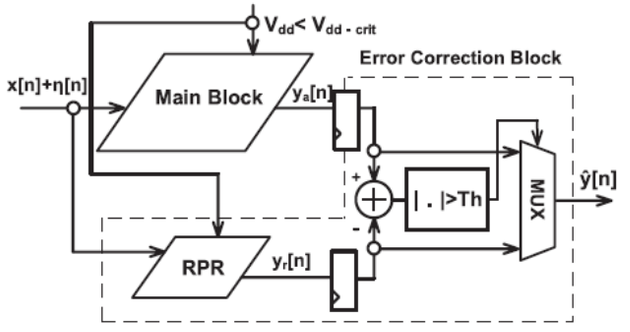

Fig. 1. ANT architecture

Under VOS, there are a number of input-dependent soft errors in its [1]output $y_a[n]$; however, RPR output y_r [n] is still correct since the critical path delay of the replica is smaller than T_{samp}. Therefore, yr [n] is applied to detect errors in the MDSP output $y_a[n]$. Error detection is accomplished by comparing the difference $|y_a[n] - y_r[n]|$ against a threshold Th[4]. Once the difference between ya[n] and yr [n] is larger than T_h, the output $\hat{y}[n]$ is y_r [n] instead of $y_a[n]$. As a result, $\hat{y}[n]$ can be expressed as

$$\hat{y}[n] = \begin{cases} y_a[n], & \text{if } |y_a[n] - y_r[n]| \le T_h \\ y_r[n], & \text{if } |y_a[n] - y_r[n]| > T_h \end{cases} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

T_h is determined by

$$T_h = \max_{\forall \text{input}} |y_o[n] - y_r[n] \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Where $y_o[n]$ is error free output signal.

In this way, the power consumption can be greatly lowered [3]while the SNR can still be maintained without severe degradation.

II. PREVIOUSLY PROPOSED ARCHITUCTURE

The fixed-width RPR to replace the full-width RPR block in the ANT design, as shown in Fig. 2[5], which can not only provide higher computation precision, lower power consumption, and lower area overhead in RPR, but also perform with higher SNR, more area efficient, lower operating supply voltage, and lower power consumption in realizing the ANT architecture[7]. The fixed-width designs are usually applied in DSP applications to avoid infinite growth of bit width. Cutting off n-bit least significant bit (LSB) output is a popular solution to construct a fixed-width DSP with n-bit input and output function. The hardware complexity and power consumption of a fixed-width DSP is usually about half of the full-length one. However, truncation of LSB part results in rounding error, which needs to be compensated precisely[6]. Many literatures have been presented to reduce the truncation error with constant correction value or with variable correction value. The circuit complexity is to compensate with constant corrected value can be simpler manner that of variable correction value; however, the variable correction approaches are usually more precise.

In their compensation method is to compensate the truncation error between the full-length multiplier and the fixed-width multiplier. However, in the fixed-width RPR of an ANT multiplier, the compensation error we need to correct is the overall truncation error of MDSP block. Unlike the compensation method is to compensate the truncation error between the full-length MDSP multiplier and the fixed-width RPR multiplier. In nowadays, there are many fixed-width multiplier designs applied to the full-width multipliers. However, there is still no fixed-width RPR design applied to the ANT multiplier designs[8].

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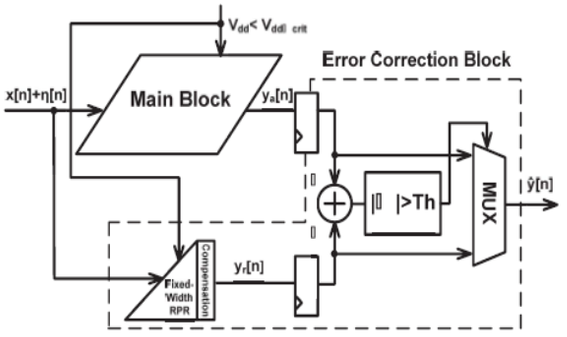

Fig 2. Fixed width RPR block

To achieve more precise error compensation, compensate the truncation error with variable correction value. We construct the error compensation circuit mainly using the partial product terms with the largest weight in the least significant segment. The error compensation algorithm makes use of probability, statistics, and linear regression analysis to find the approximate compensation value[9]. To save hardware complexity, the compensation vector in the partial product terms with the largest weight in the least significant segment is directly inject into the fixed-width RPR, which does not need extra compensation logic gates . To further lower the compensation error, also consider the impact of truncated products with the second most significant bits on the error compensation[10]. In this method propose an error compensation circuit using a simple minor input correction vector to compensation the error remained. In order not to increase the critical path delay, locate the compensation circuit in the noncritical path of the fixed-width RPR. As compared with the full-width RPR design, the proposed fixed-width RPR multiplier not only performs with higher SNR but also with lower circuitry area and lower power consumption[12].

A. Proposed Precise Error Compensation Vector for Fixed-Width RPR Design

In the ANT design, the function of RPR is to correct the errors occurring in the output of MDSP and maintain the SNR of whole system while lowering supply voltage. In the case of using fixed-width RPR to realize ANT architecture, not only lower circuit area and power consumption, but also accelerate the computation speed as compared with the conventional full-length RPR. However, need to compensate huge truncation error due to cutting off many hardware elements in the LSB part of MDSP.
In the MDSP of n-bit ANT Baugh–Wooley array multiplier, its two unsigned n-bit inputs of X and Y can be expressed as

$$X = \sum_{i=0,}^{n-1} x_i \cdot 2^i$$

$$Y = \sum_{j=0}^{n-1} y_j \cdot 2^j \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

The multiplication result P is the summation of partial products of x_i y_j, which is expressed as

$$P = \sum_{j=0}^{2n-1} p_k \cdot 2^k = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1} x_i\, y_j\, 2^{i+j} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4)$$

The (n/2)-bit unsigned full-width Baugh–Wooley partial product array can be divided into four subsets, which are most significant part (MSP), input correction vector [ICV(β)], minor ICV [MICV(*α*)], and LSP, as shown in Fig. 3[10]. In the fixed width RPR, only MSP part is kept and the other part are removed. Therefore, the other three parts of ICV(*β*), MICV(*α*), and LSP are called as truncated part[11]. The truncated ICV(*β*) and MICV(*α*) are the most important parts because of their highest weighting. Therefore, they can be applied to construct the truncation error compensation algorithm.

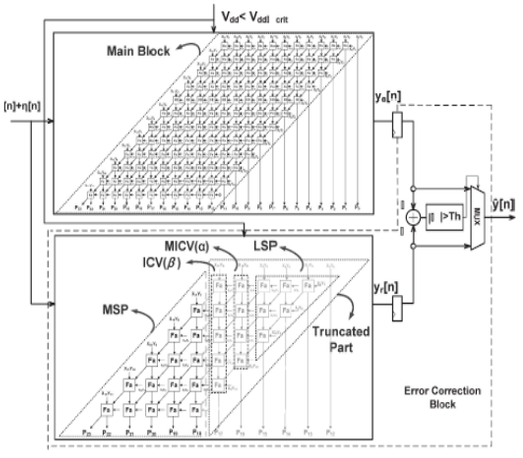

Fig 3. 12x12 bit multiplier is implemented with fixed width RPR

To evaluate the accuracy of a fixed-width RPR, we can exploit the difference between the (*n*/2)-bit fixed-width RPR output and the 2*n*-bit full-length MDSP output, which is expressed as

$$\varepsilon = P - P_t \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(5)$$

Where *P* is the output of the multiplier in MDSP

And P_t is the output of the fixed-width truncated binary multiplier in RPR.

In this baugh wooley method is applied to the multiply accumulate unit and measure the perform.

III. PROPOSED METHOD

In this proposed system , in fig 2 replace baugh wooley multiplier using Wallace tree multiplier and compare the performance. Here in this MDSP block apply to the Wallace tree multiplier method[13].

The Wallace tree has three steps:

1. Multiply (that is - AND) each bit of one of the arguments, by each bit of the other, yielding n^2 results. Depending on position of the multiplied bits, the wires carry different weights.
2. Reduce the number of partial products to two by layers of full and half adders.
3. Group the wires in two numbers, and add them with a conventional adder.

In this Wallace tree multiplier technique is shown in fig4. Here 4x4 bit multiplier is in there.

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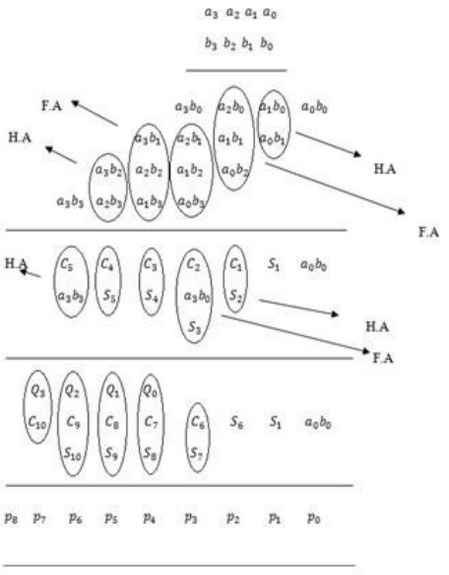

Fig 4 wallace tree multiplier technique

The (n/2)-bit unsigned full-width Wallace tree partial product array can be divided into four subsets, which are most significant part (MSP), input correction vector [ICV(β)], minor ICV [MICV(*α)*], and LSP, as shown in Fig. 3[14]. In the fixed width RPR, only MSP part is kept and the other part are removed. Therefore, the other three parts of ICV(*β)*, MICV(*α)*, and LSP are called as truncated part. The truncated ICV(*β)* and MICV(*α)* are the most important parts because of their highest weighting. Therefore, they can be applied to construct the truncation error compensation algorithm.

IV. APPLICATIONS

In proposed system, in multiply accumulate unit(MAC) will be used. In this unit low power truncated baugh-wooley and Wallace tree multiplier is used and compare the performance.

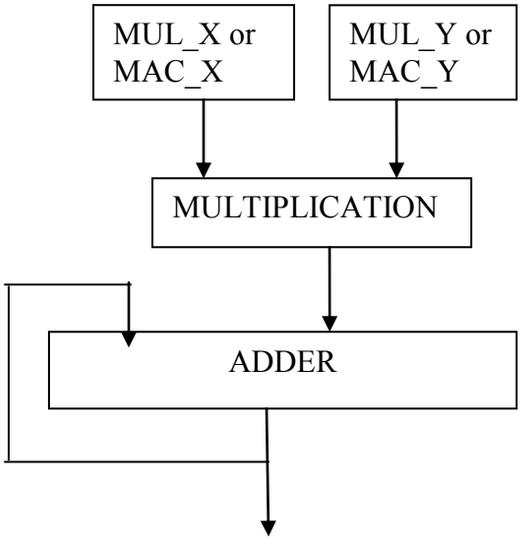

Fig 4. MAC architecture

A. *Baugh Wooley Multiplier*

Fig 4 adder block is same , but the multiplication block apply to the 12 bit truncated baugh wooley multiplier[15]. Here analysis the speed, area and power.

B. *Wallace Tree Multiplier*

Fig 4 adder block is same , but the multiplication block apply to the 12 bit truncated Wallace tree multiplier. Here analysis the speed, area and power[16].

Here adders block both baugh wooley and Wallace tree multiplier used in half and full added circuit.

V.RESULT AND DISSCUTIONS

In this low power truncated binary multiplier is to reduce the delay, power and area, Compare to the existing approach. It is used for high speed devices.

Here Wallace tree multiplier is better then baugh wooley multiplier by applying multiply accumulate unit and then Wallace tree multiplier is reduced the time ,power and area compared to baugh wooley multiplier

In Wallace tree multiplier compared with baugh wooley multiplier delay will reduced 24%,area will reduced 14% and power will reduced 35%.

TABLE I

COMPARISATION TABLE

Functions	Existing function	Proposed function
Time Delay	41.488ns	10.032ns
Area	5145	750
Power	97mW	34mW

VI. CONCLUSION

In this truncated binary multiplier paper is a low-error and area-efficient fixed-width RPR-based ANT multiplier design is presented. In proposed ANT Wallace tree multiplier compared with baugh wooley multiplier delay will reduced 24%,area will reduced 14% and power will reduced 35%. In the presented 12-bit by 12-bit ANT multiplier, the circuitry area in fixed-width RPR can be saved by 86% and power consumption in ANT design can be saved by 65% as compared with the baugh wooley multiplier ANT design.

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