Analysis of 8T SRAM Cell Using Leakage Reduction Technique

Sandhya Patel and Somit Pandey

***Abstract*—The purpose of this manuscript is to decrease the leakage current and a memory leakage power SRAM cell with the Drowsy cache design techniques for circuit. In drowsy cache method, low supply voltage (VDD) is applied to the SRAM cell when only hold operation is performed. When read and write operations have been performed in active mode, high supply voltage is applied. This drowsy cache method can be capable of reduce the leakage of power hold mode. SRAM cell have smallest difficulty in terms of area and speed of the chip. The leakage current in the SRAM cell increases due to the reduction in the length of the channel of the MOSFET. The proposed 8T SRAM cell has been designed using orCad pSpice A/D tool, the results of all simulations has been generated by the pSpice A/D simulator.**

***Index Terms*—SRAM, Leakage Current, Leakage Power, Drowsy Cache, Bit Line, Word Line.**

I. INTRODUCTION

At the nanoscale CMOS technology, the power supply has become a design constraint not only on the handheld and mobile devices, but also in the high-performance processors. Dynamic power dissipation takes place due to the switch activity of CMOS circuits and power dissipation static takes place due to leakage currents. Therefore, the leakage currents are gaining additional importance. But with the reduction of CMOS transistors, gate leakage and sub-threshold leakage current increases. The gate leakage is expected to increase at a rate of 500x by generation of technology while the sub-threshold should increase of leakage by 5x [1]. There are several techniques for leakage reduction introduced by the community of researchers, but each of them must be checked according to the techniques of circuit and the target technology without sacrificing the stability of data, delay etc. Due to big size of the on-chip SRAM, leakage current is the mainly significant determinant of the total energy consumption in the SRAM memory. Rapidly increase of results of leakage current in large quantity of the power consumption. The main challenges to the future the SRAM memory are the leakage of the power consumption, the leakage current and the variation parameter [2-3]. When increase in leakage power in the future technologies due to reduction in the threshold voltage. 8T SRAM cell has been proposed with the goal of reducing leakages [4-6].

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II. 8T SRAM CELL DESIGN

The 8T SRAM cell consists of latch and two n-channels MOSFET based access transistors shown in fig.1; these cross coupled inverters are called as a latch. The latch has four transistors; each bit in a SRAM is stored on four transistors. The drain terminal of n-channel access transistors are connected to the latch inputs and source terminals are connected to the bit line and bit line bar. The additional n-channel transistor M7 is connected to the storage node Q and M8 transistor are connected to the Read word and read bit lines (RDWL and RDBL).

SRAM stability is characterized by the data retention stability through a read operation. In 6T SRAM cell, the data storage nodes are accessed directly through the n-channel access transistors connected to the bit lines. The storage nodes are interrupted due to the voltage division between the latch and the n-channel MOSFET access transistors during a read operation.

Separation of data retention component and data output component means there will be no relationship between I_{cell} and read SNM. To overcome the problem of destruction of data in 6T and 7T SRAM cells during the read operation [7-8], we implement the 8T cell, for which separate word lines and read/write bits are used to separate the output data and the data retention element. In turn, the implementation provides a cell read disturb free operation. As shown in fig.1, 8T SRAM cell has 30% more area than a conventional 6T SRAM cell, however. The 30% area overhead is composed of not only the two added n-channel transistors but also of the contact area of the word-line for write (WWL) operations. While WL contact area is conventionally assigned to the boundary line between two SRAM cells, in this 8T SRAM cell the WWL contact area is assigned to within a cell.

III. 8T SRAM CELL USING DROWSY CACHE METHOD

SRAM cell is a memory element and performs several operations. These operations are read, write and hold operation. It is considered that, read and write operations are performed in active mode of operation. In case of standby mode, hold operation instead of read and write operation takes place.

The hold operation in standby mode takes place by using latching phenomenon of memory so that the data does not vanish during standby state and in this mode very low supply voltage is needed to hold the data.

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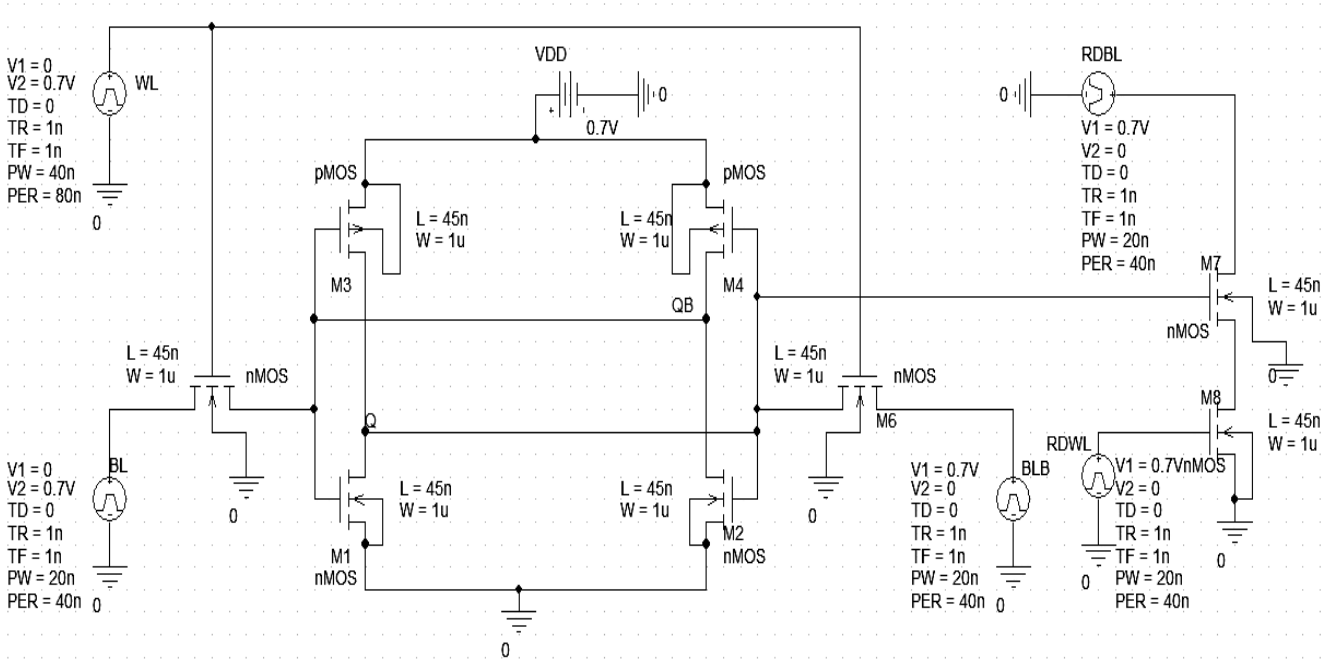

Fig. 1: The Schematic of 8T SRAM Cell

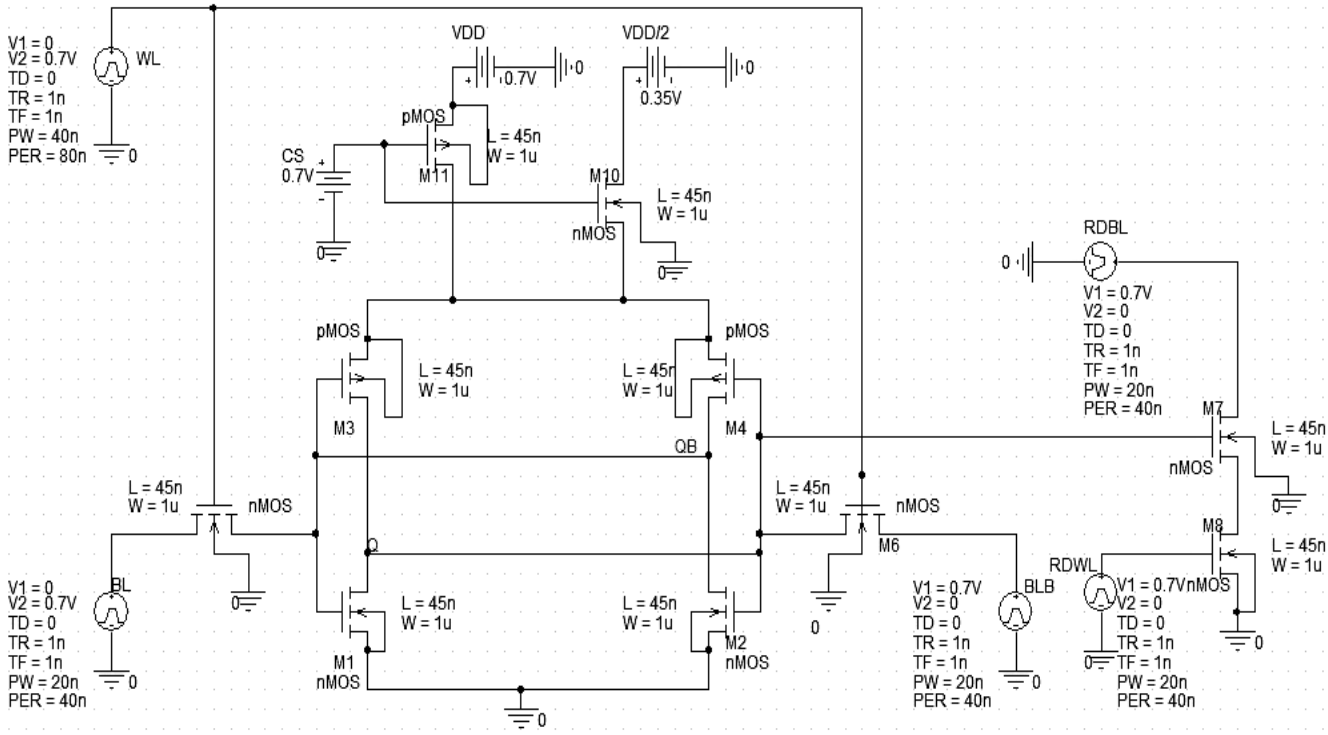

Fig. 2: The Schematic of 8T SRAM Cell using Drowsy Cache Method

In drowsy cache method, low supply voltage (VDD) is applied to the SRAM cell when only hold operation is performed. When read and write operations have been performed in active mode, high supply voltage is applied [9-10]. It has used multiple supply voltages in memory cell. It is known that leakage current reduces on reducing VDD therefore low VDD is used in this technique during standby mode and high VDD during active mode. It has reduced the leakage current and power consumption to enhance the performance of circuit. The schematic of SRAM cell using drowsy cache is shown in Figure 2.

IV. Simulation Results

The proposed 8T SRAM cell has been designed using orCad pSpice A/D tool; all the waveforms have been generated on pSpice A/D simulator. The proposed 8T SRAM cell is decreasing leakage power and leakage current, but it does not decrease enough leakage power and leakage current which leads to application of drowsy cache method to decrease leakage power and leakage current into 8T SRAM cell.

In drowsy cache design, since sleep transistor is used to

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operate at 0 V and 0.7 V. Therefore, when sleep is kept at 0 V, PMOS becomes ON and NMOS turns to OFF state. At this state, VDD becomes equal to .7 V. Similarly, the same design is simulated at sleep equal to 0.7V, at this voltage PMOS becomes OFF and NMOS becomes ON, so that VDD reaches to 0.35V. The waveforms of leakage current at sleep= 0V and sleep= 0.7V are shown in Figure 3, Figure 4.

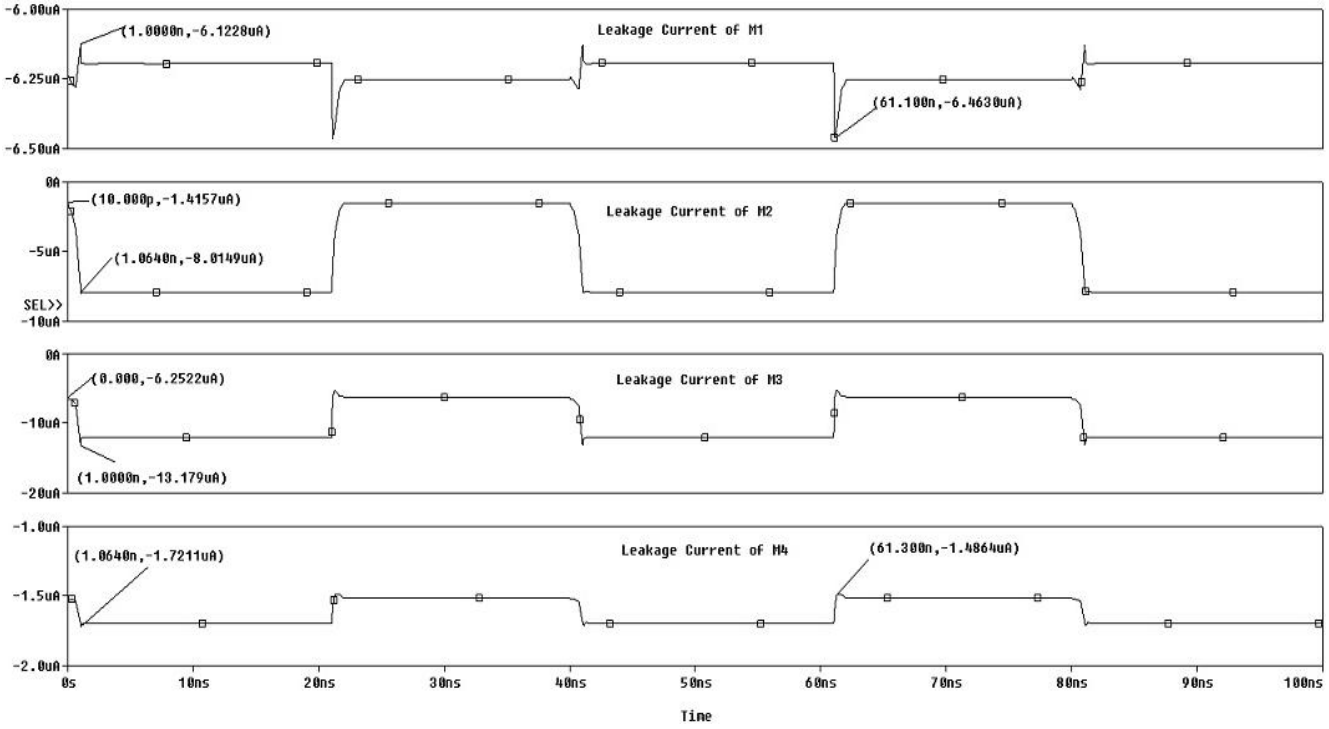

Figure 3: The waveform of leakage current in 8T SRAM cell using Drowsy Cache at sleep=0

The leakage current of M1, M2, M3 and M4 transistors at sleep=0V are $-6.123\mu A$, $-1.414\mu A$, $-6.252\mu A$, and $-1.486\mu A$ respectively. The leakage current of M1, M2, M3 and M4 transistors at sleep=0.7V are $-1.196\mu A$, $-180.018nA$, $-272.870nA$ and $-281.840nA$ respectively.

The waveform of leakage power in 8T SRAM using drowsy cache is shown in figure 5. The leakage power of M1, M2, M3 and M4 transistors are $6.227nW$, $5.710nW$, $22.280nW$ and $25.947nW$ respectively.

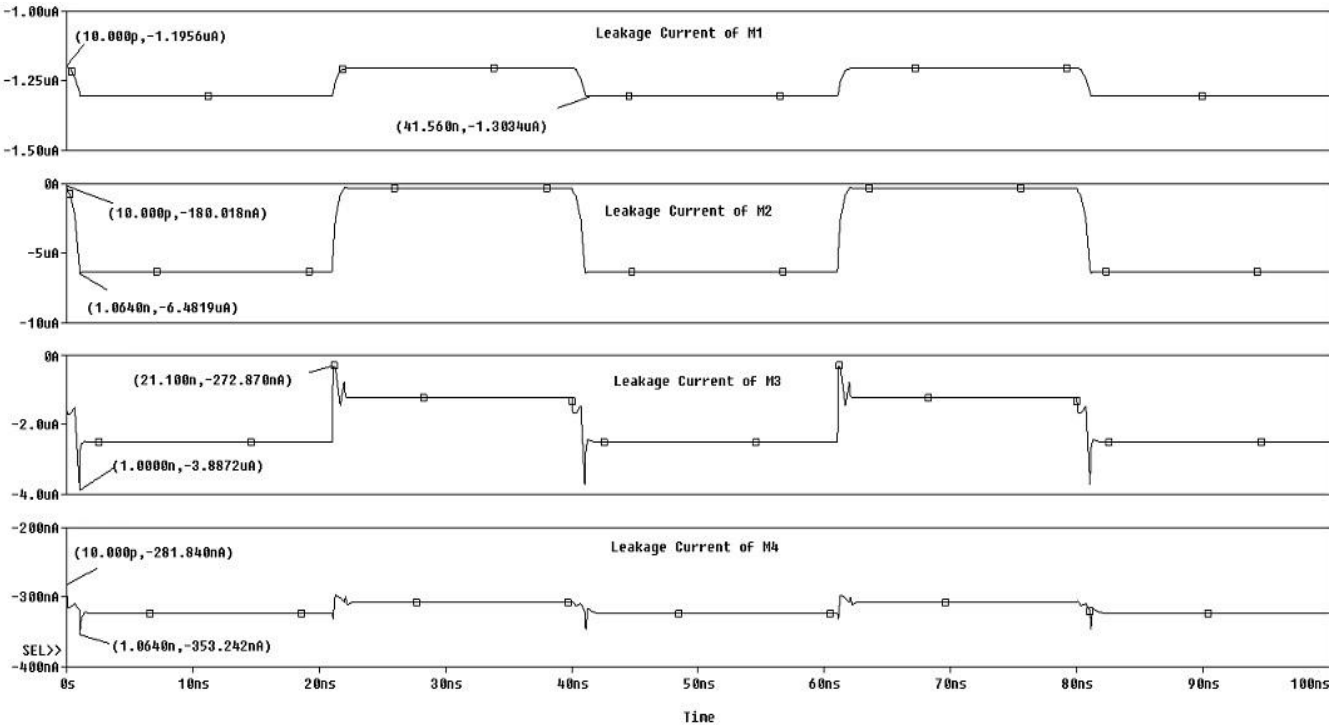

Figure 4: The waveform of leakage current in 8T SRAM cell using Drowsy Cache at sleep=0.7

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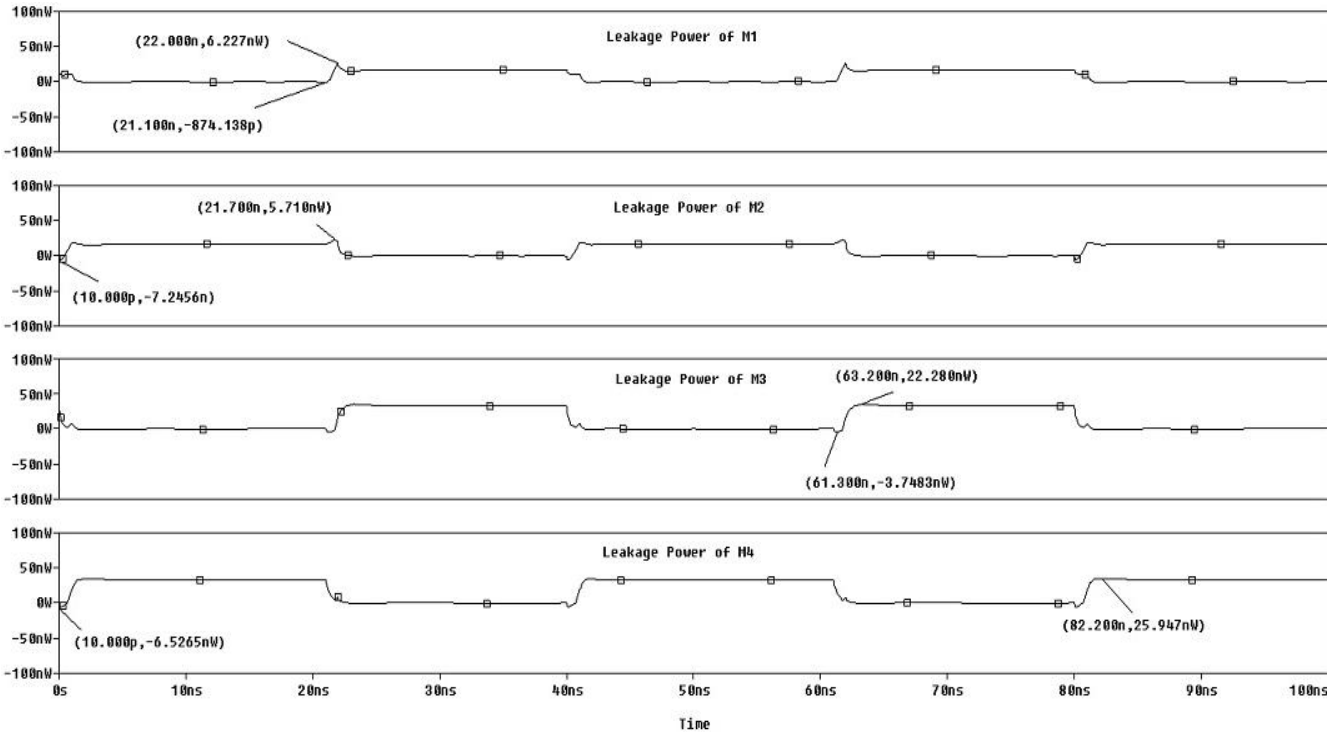

Figure 5: The waveform of leakage power in 8T SRAM cell using Drowsy Cache

The results obtained from the orCad pSpice A/D simulator have been summarized in the table 1. In table 1, we compare the parameters of 8T SRAM cell using drowsy cache method with 8T SRAM cell.

Table. 1 Comparison of Leakage Current and Leakage Power of 8T SRAM with and without Technology

8T SRAM Cell	Leakage Current				Leakage Power			
	M1	M2	M3	M4	M1	M2	M3	M4
Without Technique	45.604*nA*	89.619*nA*	555.915*nA*	552.501*nA*	9.374*nW*	8.082*nW*	25.600*nW*	29.262*nW*
Drowsy cache at sleep=0V	–6.123μ*A*	–1.414μ*A*	–6.252μ*A*	–1.486μ*A*	6.227*nW*	5.710*nW*	22.280*nW*	25.947*nW*
Drowsy cache at sleep=0.7V	–1.196μ*A*	–180.018*nA*	–272.870*nA*	–281.840*nA*				

V. CONCLUSION

Analysis of leakage current and leakage power parameters of 8T SRAM cell has been described in this paper. An analysis of leakage currents in 8T SRAM cell show that leakage currents contribute significantly on the whole leakage power dissipation in hold mode. Leakage reduction in 8T SRAM cell has been predicted using drowsy cache technique. Drowsy cache technique reduces the leakage current and hence power consumption. Among these techniques, drowsy cache design is the prominent technique which could reduce the leakage current by a factor of ~90-95% using sleep at 0.7 V. Therefore power consumption of the 8T SRAM is reduced and performance has been enhanced.

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