

Area efficient Circuit Design of N-bit Carry look Ahead Adder with High Speed by using Static CMOS

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Abstract— ADDER is an important block in digital system. It has applications in digital signal processing to perform finite impulse response and infinite impulse response. Ripple carry adder speed will be disadvantage but area will be less when compared to carry look ahead adder in which area will be the disadvantage but speed will be the advantage. Now we have got the challenge that is to reduce the area but speed should be retained that is carry should be designed separately for generate part and propagate part, so with this two design constraints area and speed are going to be achieved but never the less third important design constraint is power consumption of the circuit which by default will be achieved as we are designing the circuit by using STATIC CMOS. In this project the proposed Adder has been designed by using STATIC CMOS 180nm TECHNOLOGY and the tool being used is TANNER EDA tool.

Index Terms—6TCircuit, 28TCircuit, Carry look ahead Adder, static cmos.

INTRODUCTION

Carry look ahead adder presented was designed by Amita in 2014[1], Implementation of Adder consumes more power as well as more Area but gives more speed. Carry look ahead adders presented was designed by jagannath samanta in 2013[2], out of the many logic styles they have used they say the best design with transistor count is 146 for 4-bit and 452 for 8-bit means design is not an extendable design. K. Ueda[3] employed carry look ahead adder by using pass transistor logic which by default has problem of no full output voltage swing. Y. T. Pai[4] proposed a design for high speed but we are here interested in all the design constraints.

Now we need to design a carry look ahead adder by implementing our own technique such that functional behavior of the circuit should be correct but off course by keeping in mind the design constraints like AREA as well as POWER as these are our concern. We have designed carry look ahead adder by using STATIC CMOS logic style, it has advantage of easily being converted to a layout, because layout is the final implementation of the circuit and circuit is just symbolic representation. To achieve less transistor count

we can chose logic styles like PTL which by default takes less number of Transistors but we have chosen STATIC CMOS which by default takes more number of transistors but we need to design the carry look ahead adder which also by default takes more number of transistors with less number of transistors. Logic style like PTL (Pass Transistor Logic) has disadvantage of less noise immunity as well as the problem of implementing in technology's which has less supply voltages.

I. CARRY LOOK AHEAD ADDER

Adder is going to add 4 bits of A (A3 to A0) and 4 bits of B (B3 to B0) and gives 5-bit result out of those 4-bits will be sum bits and 1-bit will be carry bit. we can design the circuit for Carry look ahead adder which by default gives high speed but at the cost of Area.

Now let us see how can we design the circuit for 4-bit carry look ahead adder coming from the least significant bit side that is A0 and B0 there will not be any Carry in because there was no any previous addition. Now just a Half adder kind of circuit is needed then sum output and PROPAGATE output is one another same because A0 XOR B0 will be the P0 and S0 also, this was our requirement but how to design the circuit, we first designed the XNOR Circuit and then we inverted it and it will be the output for S0 and P0. The XNOR which we designed has two outputs one will be the XNOR function and another will be the NAND function, this will be the complement of the GENERATE as well as the complement of carry out.

Now the second Addition that is A1 and B1 we will be having Carry in which is the Carry out of the least significant bit stage, so our requirement is now Full Adder but how to design the circuit for sum and Carry part, here we need to design the carry in two sections that is GENERATE and PROPAGATE. Earlier we have seen that when designing XNOR one of the output is complement of the GENERATE, so our idea is to design sum part of Full Adder by using XNOR for A1 and B1 and this XNOR function output along with previous carry XOR was required for us because Carry was in complemented form, so XNOR'S XNOR function output is complement of the PROPAGATE and NAND function is complement of the GENERATE and XOR circuit

has two outputs that is first one is XOR function and second is NOR function and first one is Sum output. Till now we have designed Sum part completely and GENERATE part of Carry only but we need PROPAGATE part also and these PROPAGATE and GENERATE part needs to be combined to form Carry output, so this Carry output Circuit has (A1,B1) XNOR'S first output as well as second output and (A0,B0) XNOR'S second output as the inputs.

Now let us see the third Addition that is A2 and B2 along with previous Carry here also we have used XNOR'S to design Sum part and unlike in previous Addition which required one XNOR followed by XOR, here two XNOR'S only were required because previous Carry was in TRUE form not in complemented form and first XNOR'S first output is complement of the PROPAGATE and second output is the complement of the GENERATE and second XNOR'S first output is Sum output but second output is unused. we need to design Carry out part to do this previous Carry output, complement of the PROPAGATE and complement of the GENERATE are given as inputs

Now let us see the fourth Addition that is A3 and B3 along with previous Carry here also we have used XNOR'S to design Sum part and like in previous Addition which required one XNOR followed by another XNOR, here two XNOR'S only were required because previous Carry was in TRUE form not in complemented form and first XNOR'S first output is complement of the PROPAGATE and second output is the complement of the GENERATE and second XNOR'S first output is Sum output but second output is unused. we need to design Carry out part to do this previous Carry output, complement of the PROPAGATE and complement of the GENERATE are given as inputs.

Now let us see the fifth Addition that is A4 and B4 along with previous Carry here also we have required XNOR'S to design Sum part and like in previous Addition which required one XNOR followed by another XNOR, here two XNOR'S only were required because previous Carry was in TRUE form not in complemented form and first XNOR'S first output is complement of the PROPAGATE and second output is the complement of the GENERATE and second XNOR'S first output is Sum output but second output is unused. we need to design Carry out part to do this previous Carry output, complement of the PROPAGATE and complement of the GENERATE are given as inputs.

Now let us see the sixth Addition that is A5 and B5 along with previous Carry here also we have required XNOR'S to design Sum part and like in previous Addition which required one XNOR followed by another XNOR, here two XNOR'S only were required because previous Carry was in TRUE form not in complemented form and first XNOR'S first output is complement of the PROPAGATE and second output is the complement of the GENERATE and second XNOR'S first output is Sum output but second output is unused. we need to design Carry out part to do this previous

Carry output, complement of the PROPAGATE and complement of the GENERATE are given as inputs.

Now let us see the seventh Addition that is A6 and B6 along with previous Carry here also we have required XNOR'S to design Sum part and like in previous Addition which required one XNOR followed by another XNOR, here two XNOR'S only were required because previous Carry was in TRUE form not in complemented form and first XNOR'S first output is complement of the PROPAGATE and second output is the complement of the GENERATE and second XNOR'S first output is Sum output but second output is unused. we need to design Carry out part to do this previous Carry output, complement of the PROPAGATE and complement of the GENERATE are given as inputs.

Now let us see the Nth Addition that is AN and BN along with previous Carry here also we have required XNOR'S to design Sum part and like in previous Addition which required one XNOR followed by another XNOR, here two XNOR'S only were required because previous Carry was in TRUE form not in complemented form and first XNOR'S first output is complement of the PROPAGATE and second output is the complement of the GENERATE and second XNOR'S first output is Sum output but second output is unused. we need to design Carry out part to do this previous Carry output, complement of the PROPAGATE and complement of the GENERATE are given as inputs.

There are 5 cells in this Carry look ahead adder named XNOR,XOR,6T Circuit, 28T Circuit And one NOT gate. XNOR has two inputs and two outputs, XOR has two inputs and one output, 6T Circuit has three inputs and one output. And 28T Circuit has three inputs and two outputs.

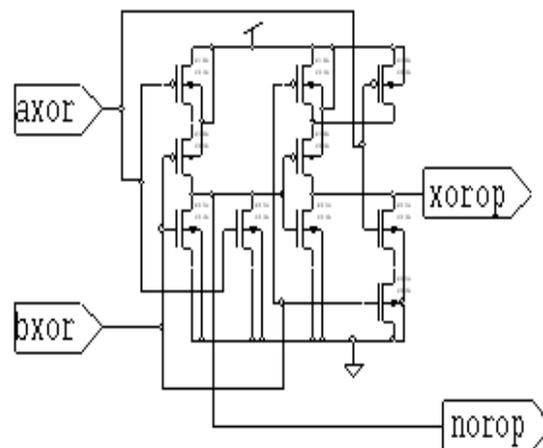


Fig. 1 XOR (X) Circuit

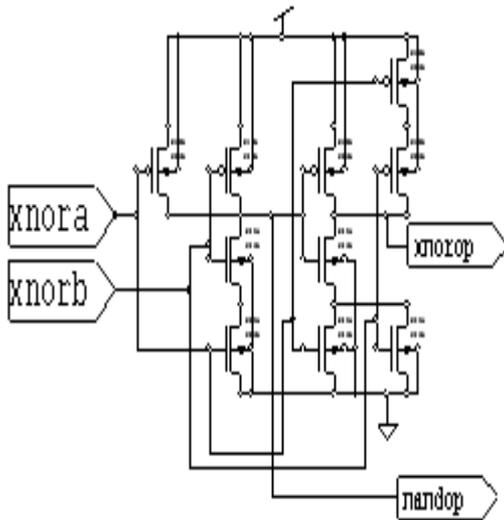


Fig. 2 XNOR (N) Circuit

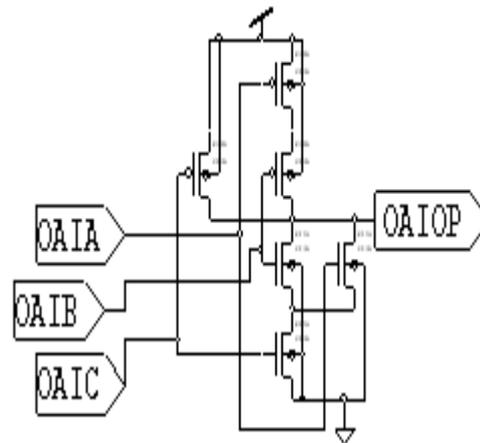


Fig. 3 6T (I) Circuit

XOR needs 10 number of transistors, XNOR Circuit needs 10 number of transistor, 6T Circuit needs six number of Transistor, NOT Circuit needs two number of Transistors and 28T Circuit needs 28 number of transistors. Total number of transistors required are two XNOR Circuits which requires 20 number of transistors, one XOR Circuit needs 10 number of transistors, one not gate needs two number of , one 6T Circuit needs six number of transistors, two 28T Circuit which needs 56 number of transistors so for 4-bit Carry look ahead adder we need totally $56+6+10+20+2$ transistors.

Since our design can be easily extendable to N-BIT we require for N-BIT carry look ahead adder 12 transistors for least significant bit for least significant bit+1 stage 26 transistors are required and from least significant bit+2 TO Most significant bit each stage requires 28 number of transistors so the total number of transistors required for N-BIT carry look ahead adder is $12+26+((N-2)*28)$. total number of cells required are less and as well as they are designed in STATIC CMOS it will be beneficiary for the layout designers to do the Layout.

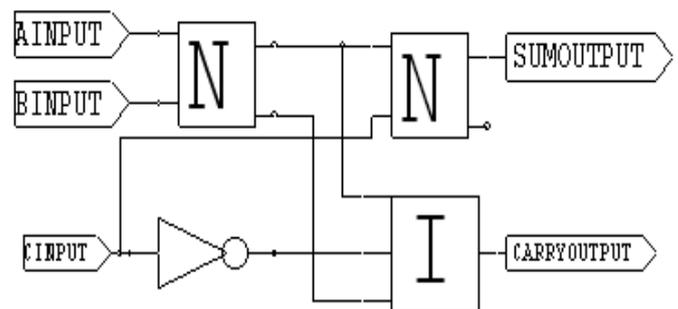


Fig. 4 28T Circuit

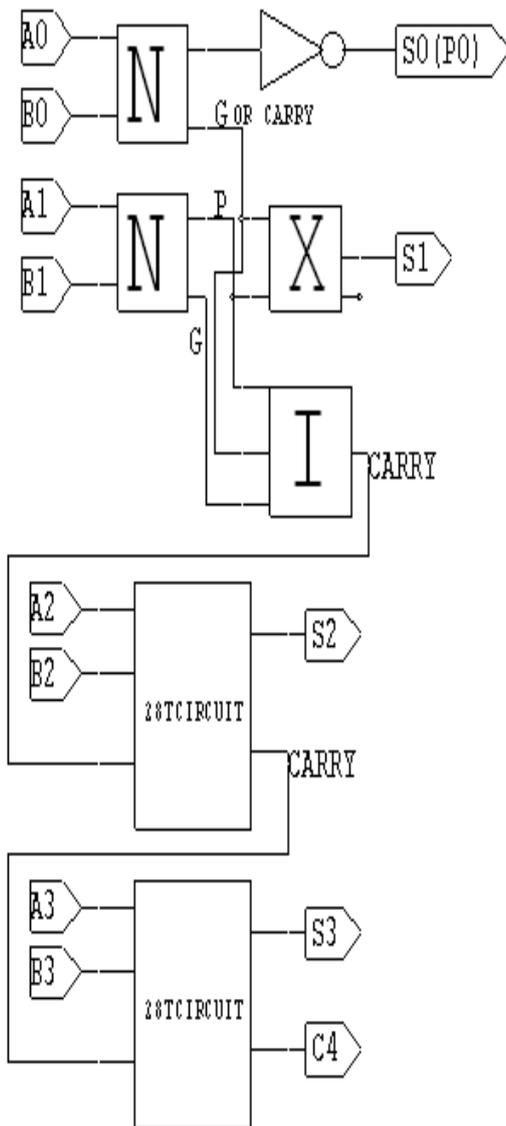


Fig. 5 Block diagram of 4-bit Carry look ahead adder.
(EXTENDABLE TO N-BIT)

II. STATIC CMOS

STATIC CMOS has the advantage of if we design the PULL-UP network then by default we can design the PULL-DOWN network and vice-versa means if we have two PULL-UP networks and two PULL-DOWN networks then path will be like PULL-DOWN followed by PULL-UP if we are designing for logic1 and PULL-UP followed by PULL-DOWN if we are designing for logic0.

We also need to ensure that there are few transistors in series either in PULL-UP network or PULL-DOWN network, having series chain of transistors in PULL-DOWN network is somewhat better than PULL-UP network as N-MOSFET'S will be there in PULL-DOWN network and yes they are faster.

By using this STATIC CMOS layout designers can easily design Floor-planning which includes Placement and as well as Routing and only efficient placement leads to efficient routing which will impact the total Area, speed as well as Power. STATIC CMOS needs more number of transistors because we require equal number of TRANSISTORS in the PULL-UP network as well as in the PULL-DOWN network. supply voltages are very less in recent technologies, so the unknown region will be more when compared to logic1 and logic 0 region if there is any logic levels degradation.

III. PERFORMANCE ANALYSIS

Implementation of 4-bit Carry look ahead adder has been done using STATIC CMOS logic style. Table1 shows POWER comparison of AMITA Carry look ahead adder (Reference1), JAGANNATH SAMANTA Carry look ahead adder(Reference2) and the proposed Carry look ahead adder.. This table clearly shows that proposed Carry look ahead adder has very less power dissipation that too in nano watts than reference2 as well as reference1.

The Carry look ahead adder which we designed using STATIC CMOS logic style uses less number of transistors. It uses 150% less area(number of transistors) than reference2 for 4-bit CLA(carry look ahead adder) and 250% less area(number of transistors) than reference2 for 8-bit CLA(carry look ahead adder). Design which we presented will have only uniform growth with respect to number of transistors as size of the design is increased.

TABLE1 AVERAGE POWER CONSUMPTION IN THREE DESIGNS

4-BIT	Design in Reference1 (mW)	Design in Reference2 (uW)	Design in This paper (nW)
Average Power	1.369	2.67	29.2

TABLE2 COMPARISION OF AREA IN TWO DESIGNS

AREA (no.of transistors)	Design in reference2	Design in this paper
4 bit	236	94
8 bit	744	206

IV. CONCLUSION

Carry look ahead adder is widely used where fast computation is needed especially in multipliers but disadvantage is Area will become worsen as size increases but we were able to design the circuit with less Area and since we have designed Adder using Carry look ahead approach by default we will achieve high speed and coming to the another important design constraint that is power by default STATIC CMOS logic, power consumption will be less. All VLSI design constraints were achieved from our design. we came with our own Design it was possible because of the FULL-CUSTOM Design which allows us to Design our own circuit by taking the leaf level cells as gates or may be Transistors since our Design is implemented in Transistors we have been able to achieve area, power and speed constraints. we have designed our Carry look ahead adder by using STATIC CMOS logic style which generally requires more number of transistors.

we are able to design the Carry look ahead adder by using less number of transistors. It shows an 8-bit Carry look ahead adder r of the proposed technique only needs 206 transistors, the technique which we presented can be easily extendable up to N-bit.

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