Circuit Design of Low area 8-bit magnitude Comparator With Low Power by Static CMOS

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Abstract— **COMPARATOR is an important block in digital system. It has applications in communication and calculation areas. The main intention of this paper is to provide new low power, low area solution for designers at transistor level. We can design the circuits based on finding equivalent Boolean expressions and then converting that Boolean expressions to a circuit, but this kind of approach never gives ultimate optimization, instead conditions based design is a good approach if we can design efficiently. At circuit level, STATIC CMOS logic style can give better results when doing the layout because of its uniform structure. Layout designer can efficiently convert a STATIC CMOS based circuit to a layout over others. In this project the proposed comparator has been designed by using STATIC CMOS 180nm TECHNOLOGY and the tool being used is TANNER EDA tool.**

***IndexTerms*—Logicblock,30TCircuit,Comparator,static cmos.**

INTRODUCTION

Low density parity check (Ldpc) was designed by gallager in 1962[1]. Implementation of ldpc decoder consumes more power, comparator is important module in decoder and it is also used in digital system C-H HUANG[2] developed priority encoder based on logic and module. S-W CHENG[3] employed conditional sum adder to design efficient comparator. J-Y KIM and H-J YOO[4] proposed a design without arithmetic operation which is even more efficient.

Now we need to design a comparator by implementing our own technique such that functional behavior of the circuit should be correct but off course by keeping in mind the design constraints like AREA as well as POWER as these are our concern. We have designed comparator by using STATIC CMOS logic style, it has advantage of easily being converted to a layout, because layout is the physical interpretation of the circuit and circuit is just symbolic representation. To achieve less transistor count we can chose logic styles like PTL which by default takes less number of Transistors but we have chosen STATIC CMOS which by default takes more number of transistors but we need to design the comparator with less number of transistors. Logic style like PTL(Pass Transistor Logic) has disadvantage of not having power rails as well as the problem of logic level degradation.

I. MAGNITUDE COMPARATOR

Comparator is going to compare 8 bits of A(A7 to A0) and 8 bits of B(B7 to B0) and decides whether ALTB(A<B) or AGTEB(A>=B). we can design the circuit for any of the two outputs means only keeping track of when A is less than B and what are all the conditions which confirms ALTB(A<B) is true then and if ALTB(A<B) is not true then AGTEB(A>=B) is true .we need to know what are all the conditions for ALTB(A<B) to become true, if (A7<B7) then ALTB(A<B) should be true and (A7>B7) status also we need to know in the upcoming condition. so we have designed a sub-circuit for these two conditions that is logic block with a7 and b7 as inputs and this logic block has two outputs , the first output is the condition for (A7<B7) and it is low and the second output is the condition for (A7>B7) and it is high. since we are designing the circuit for A<B, this logic block first output can be used as the first condition for A<B and that condition is arranged in 30T CIRCUIT so till now we have designed one condition with one logic block which has the two outputs and inputs as A7 ,B7.

Now let us see the second condition that is if (A6<B6) and if (A7>B7) is false then ALTB(A<B) should be true, so we have designed second logic block with inputs as A6,B6 and logic block's first output is to know the status of (A6<B6) and it is low and we also need (A6>B6) status for the upcoming condition and it is high and logic block second output is for that condition. so to design the second condition this logic block's first output as well as first logic block's second output given to 30T CIRCUIT.

Now let us see the third condition that is if (A5<B5) and if (A7>B7) is false and also if (A6>B6) is false then ALTB(A<B) should be true so we have designed a third logic block with inputs as A5,B5. so first output of this logic block is to know the status of(A5<B5) and it is low. we also need (A5>B5) status for the upcoming condition and it is high and logic block second output is for that condition. So to design the third condition this logic block's first output as well as second logic block's second output and first logic block's second output given to 30T CIRCUIT.

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Now let us see the fourth condition that is if (A4<B4) and if (A7>B7) is false, if (A6>B6) is false and if(A5>B5) is false then ALTB(A<B) should be true so we have designed a fourth logic block with inputs as A4,B4. so first output of this logic block is to know the status of(A4<B4) and it is low. we also need (A4>B4) status for the upcoming condition and it is high and logic block second output is for that condition. So to design the fourth condition this logic block's first output as well as third logic block's second output, second logic block's second output and first logic block's second output given to 30T CIRCUIT.

Now let us see the fifth condition that is if (A3<B3) and if (A7>B7) is false, if (A6>B6) is false, if(A5>B5) is false and if (A4>B4) is false then ALTB(A<B) should be true so we have designed a fifth logic block with inputs as A3,B3. so first output of this logic block is to know the status of(A3<B3) and it is low. we also need (A3>B3) status for the upcoming condition and it is high and logic block second output is for that condition. So to design the fifth condition this logic block's first output as well as fourth logic block's second output, third logic block's second output, second logic block's second output and first logic block's second output given to 30T CIRCUIT.

Now let us see the sixth condition that is if (A2<B2) and if (A7>B7) is false, if (A6>B6) is false, if(A5>B5) is false, if (A4>B4) and if (A3>B3) is false then ALTB(A<B) should be true so we have designed a sixth logic block with inputs as A2,B2. so first output of this logic block is to know the status of(A32<B2) and it is low. we also need (A2>B2) status for the upcoming condition and it is high and logic block second output is for that condition. So to design the sixth condition this logic block's first output as well as fifth logic block's second output, fourth logic block's second output, third logic block's second output, second logic block's second output and first logic block's second output given to 30T CIRCUIT.

Now let us see the seventh condition that is if (A1<B1) and if (A7>B7) is false, if (A6>B6) is false, if(A5>B5) is false, if (A4>B4), if (A3>B3) is false and if(A2>B2) is false then ALTB(A<B) should be true so we have designed a seventh logic block with inputs as A1,B1. so first output of this logic block is to know the status of(A1<B1) and it is low. we also need (A1>B1) status for the upcoming condition and it is high and logic block second output is for that condition. So to design the seventh condition this logic block's first output as well as sixth logic block's second output, fifth logic block's second output, fourth logic block's second output, third logic block's second output, second logic block's second output and first logic block's second output given to 30T CIRCUIT.

Now let us see the eighth condition that is if (A0<B0) and if (A7>B7) is false , if (A6>B6) is false , if (A5>B5) is false , if (A4>B4) is false , (A3>B3) is false, (A2>B2) is false and if (A1>B1) is false then ALTB(A<B) should be true so we have designed this condition(A0<B0) by using one two input NAND gate and one NOT gate. we no need (A0>B0)status as there is no upcoming condition and to design this last condition NAND gate output, seventh logic block's second output, sixth logic block's second output, fifth logic block's second output, fourth logic block's second output, third logic block's second output, second logic block's second output and first logic block's second output given to 30T CIRCUIT.

There are 4cells in this comparator named Logic block, 30T circuit, NANDgate, NOT gate. Logic block has two outputs one for knowing the status for (A<B) and another for (A>B). 30T Circuit is the main cell which gives all the conditions for (A<B) and this is the final cell in our design. NAND,NOT is for least significant bit's of A and B.

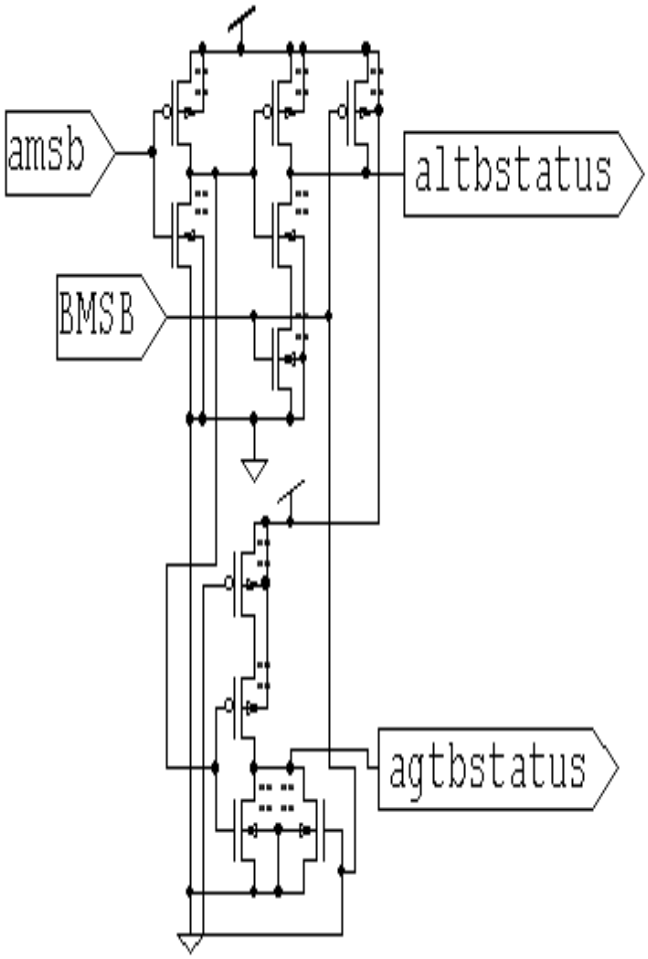

Fig. 1 Logic Block

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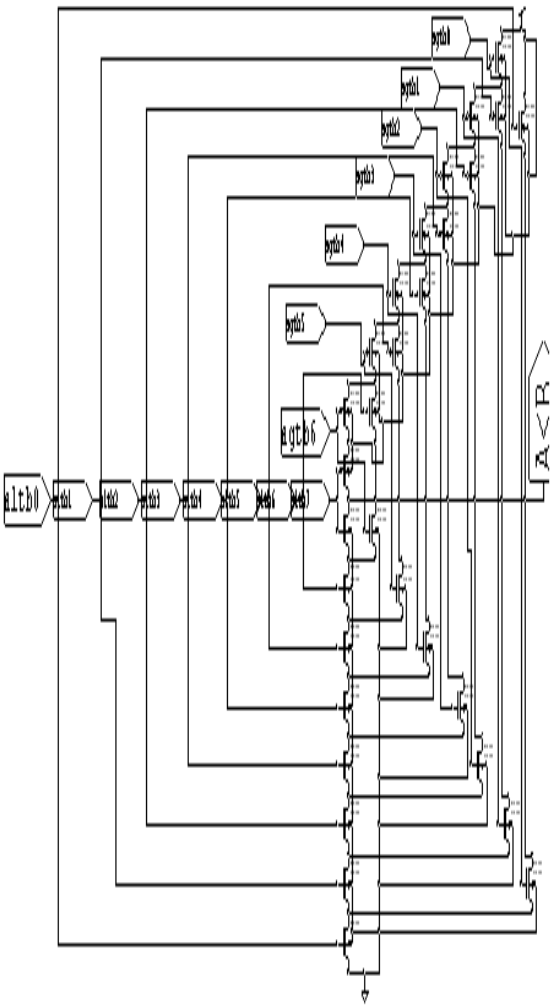

Fig. 2 30T Circuit

Logic block needs 10 number of transistors and 30T Circuit needs thirty number of transistors and NAND Circuit needs four number of Transistors and NOT Circuit needs two number of Transistors. Total number of transistors required are seven logic block's which requires 70 number of transistors, one NAND Circuit which requires 4 number of transistors, one NOT Circuit which requires 2 number of transistors and one 30T circuit which requires 30 number of transistors. So the total transistor count is 106. total number of cells required are less and as well as they are designed in STATIC CMOS it will be beneficiary for the layout designers to do the Layout.

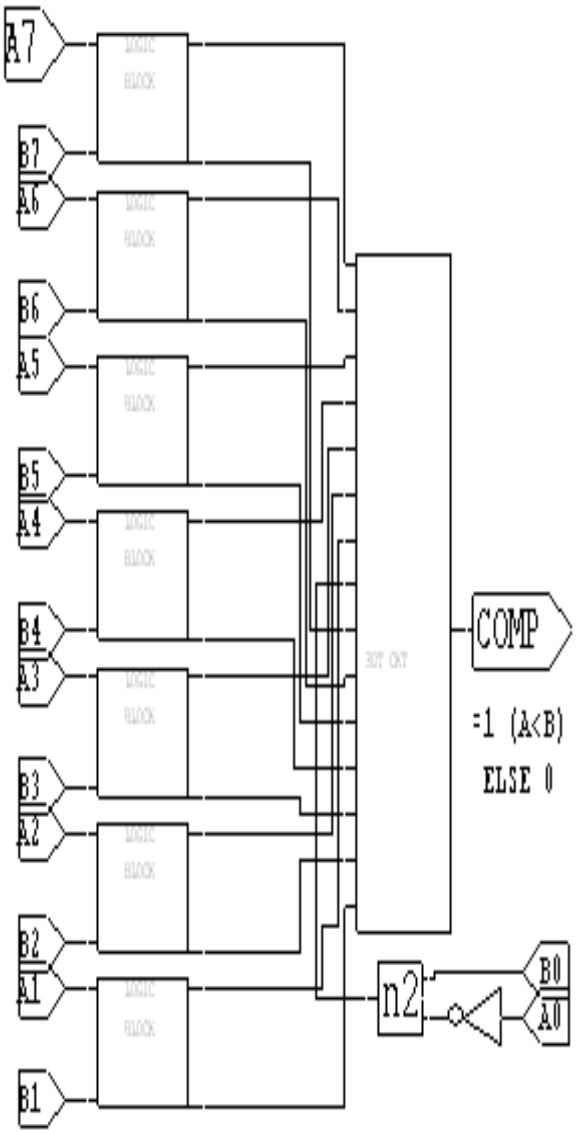

Fig. 3 Schematic of 106 transistor Comparator cell

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II. STATIC CMOS

STATIC CMOS has the advantage of noise immunity because of the power rails, either output will be pulled up to VDD or output will be pulled down to GND and no logic level degradation will be there by using this STATIC CMOS intra-cell routing as well as inter cell routing is easy to do which will result in AREA benefits as well as SPEED. STATIC CMOS needs more number of transistors because we require equal number of TRANSISTORS in the PULL-UP network as well as in the PULL-DOWN network. we can easily differentiate between output voltage high logic level and output voltage low logic level and this will be even more beneficial when the technology is scaled down where the supply voltages are very less so the unknown region will be more when compared to logic1 and logic 0 region.Even though it is recommended that do not place more number of transistors in series either in PULL-UP or PULL-DOWN region as delay is going to be worse. We need to sacrifice the speed in particular section of the circuit for achieving the AREA benefits.

III. PERFORMANCE ANALYSIS

Implementation of 8-bit magnitude comparator has been done using STATIC CMOS logic style. Table1 shows AREA comparision of IMPROVED HYBRID, STATIC CMOS and the proposed COMPARATOR. power dissipation comparision for 8-bit magnitude comparator using IMPROVED HYBRID, STATIC CMOS and the proposed COMPARATOR for various supply voltage(VDD) are shown in TABLE2. This table clearly shows that proposed STATIC CMOS has less power dissipation than IMPROVED HYBRID as well as STATIC CMOS over various supply voltages(VDD). The comparator which we designed using STATIC CMOS logic style uses less number of transistors. It uses 32% less area(number of transistors) than IMPROVED HYBRID and 25% less area(number of transistors) than STATIC CMOS.

TABLE1 COMPARISION OF AREA IN THREE DESIGNS

	Design in reference9	Design in reference10	Design in this paper
Area(number of transistors)	154	142	106

TABLE2 AVERAGE POWER(μW) CONSUMPTION IN THREE DESIGNS

Supply Voltage(VDD)	Design in reference9	Design in reference10	Design in this paper
1.4	21.4	0.092	0.014
1.2	12	0.066	0.010
1	6.05	0.044	0.006

IV. CONCLUSION

Power is becoming an important design constraint these days especially because of the battery operated devices as well as Area which in turn directly proportional to Cost of the Design one would always wants to buy a product with low cost and we can also incorporate additional functions with in the prescribed Area.we came with our own Design it was possible because of the FULL-CUSTOM Design which allows us to Design our own circuit by taking the leaf level cells as gates or may be Transistors since our Design is implemented in Transistors we have been able to acheive area and power constraints, even though we want Speed also to be more it might not be possible always . we have designed our comparator by using STATIC CMOS logic style which generally requires more number of transistors.

we are able to design the comparator by using less number of transistors than IMPROVED HYBRID which is a mix of HYBRID PTL / CMOS logic style. It shows an 8-bit comparator of the proposed technique only needs 142 transistors, the technique which we presented can be easily extendable up to 64-bit with some Design Techniques to be implemented to ensure that Delay is not worse.

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