Analysis of Harmonics in Z-Source NPC Inverter Fed BLDC Motor Drive

B.Karunamoorthy, DR.Somasundareswari, K.P.Thanusre

Abstract— **Power quality issues are the major concern in various applications. Variation in power quality may cause the power fluctuations and harmonic ripples in the devices that are used in the control circuits. It is necessary to limit the Total harmonic distortion within standards and to maintain power factor to improve the life of the power electronic component used in the particular system. Z-Source inverter is a newly invented topology which can be used for higher power application and it has tremendous advantages like improved power quality, compare to the converter fed voltage source inverter less harmonic distortion. Therefore, main purpose of this paper is to limit the Total harmonic distortion (THD) and to maintain the power factor by using space vector modulation technique. Proposed system is simulated by using MATLAB software.**

Index Terms- **THD, Power factor, Z-Source inverter, Neutral-point clamped inverter, Space vector modulation technique.**

I. INTRODUCTION

BLDC motor is widely used motor drive for both domestic and industrial purpose due to exclusion of mechanical commutator and brushes. Rotor position can be evaluated by using sensor and sensorless technique. Hall sensor is used to estimate the rotor position in sensor technique whereas; in sensorless technique back emf is used to sense the rotor position.

Neutral point clamped inverter is commonly used topology in medium voltage drives. In former publication alternative phase opposition disposition scheme and phase disposition scheme is used as modulation scheme. Above modulation scheme have high harmonic distortion. To decrease the harmonic distortion combination of both upper and lower shoot through technique is implemented by using space vector modulation technique.

To overcome the disadvantages of X-Shape network, LZ-network is used which consists of three diodes and two inductors.

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II. EXISTING SYSTEM

Existing system uses bridgeless buck boost converter fed voltage source inverter to control the speed of BLDC motor.

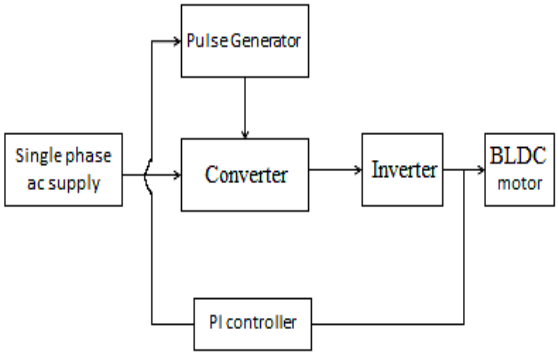

Fig.1. Existing system block diagram

Bridgeless buck boost converter operates in three modes. During mode I switch S1 will be in conduction and inductor L1 gets charged. During mode II switch S2 starts to conduct and inductor L2 gets charged. During mode III inductor enters into the discontinuous mode and capacitor supplies to the load.

There are different controllers used to control the speed of motor in closed loop. Compare to the various controller PI controllers has increased voltage gain and system stability is more. So PI controller is used to control the DC-link voltage of voltage source inverter. Sensor technique is used to measure the rotor position and depend on the position sensed switches in voltage source inverter are triggered.

The main drawback of existing system is attainable output voltage is less than the input voltage and to avoid the conduction of same leg device dead-time should be provided. Compare to the proposed system, switching stress are more in the existing system and no of components used also more.

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III. PROPOSED SYSTEM

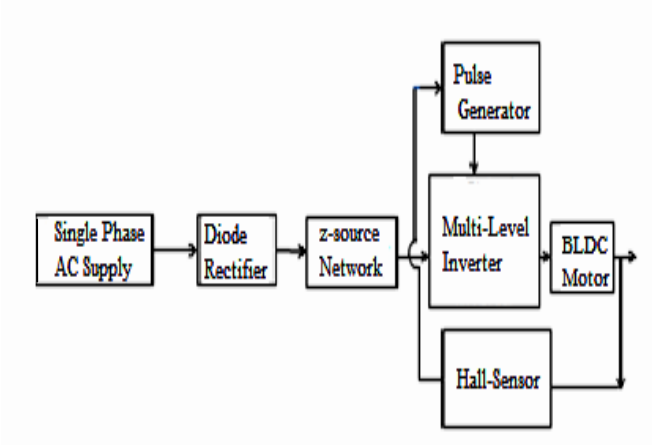

Fig.2. Proposed system block diagram

Proposed system consists of Z-Source inverter and main advantage of the Z-source inverter is compare to the existing system its boosting ratio is twice times greater. By using sensor technique, speed of the motor is controlled by adjusting DC-link voltage of Neutral-point clamped inverter.

The unique feature of the two-level Z-source inverter is that the output ac voltage fundamental can be controlled to be any value between zero and (theoretically) infinity regardless of the dc source voltage. To regulate the Z-Source inverter shoot-through states space vector modulation technique is used.

A. Z-Source Network:

Z-source inverter is a recently invented topology used mainly in photovoltaic, fuel cell applications [1] and [2]. In conventional Z-Source topology there are many disadvantages. To overcome the problems in traditional Z-source network recently there are different topologies are invented [5], [6] and [7]. In proposed paper LZ-Source network was implemented. Z-source inverter working modes classified into shoot-through mode and non-shoot through mode.

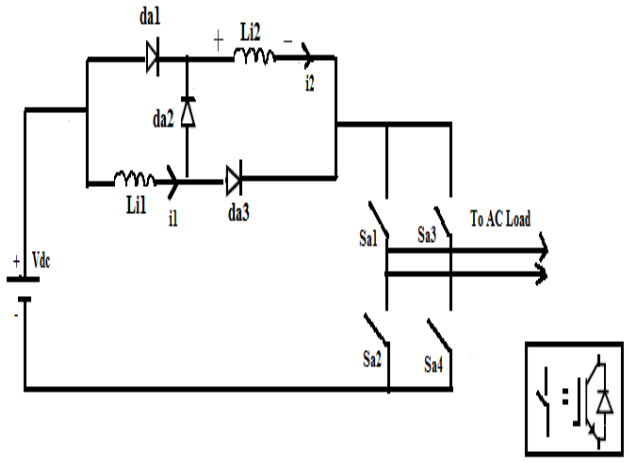

Fig.3. Z-Source Network

In shoot through mode inductors are connected in series and supplies energy to the main circuit and during non-shoot through mode inductors are connected in parallel and stores energy.

B. Neutral point clamped Inverter:

In these inverters, the voltage across semiconductor Switches are limited by diodes connected to various DC levels as such it is called Diode Clamed Multilevel inverters. Levels in inverter can be increased by increasing the number of capacitors across DC bus source [3]. Earlier NPC topologies were limited to three-levels. Later levels are extended by interconnection of two capacitors across the DC bus. The schematic figure of an n-level neutral point clamped inverter is shown in figure 1.

Neutral point clamped inverter consists of four Switches and four anti-parallel diodes. The DC voltage is divided into two by using DC capacitor [8]. The clamping diodes are the diodes linked to the neutral point, DZ1, DZ2. The output terminal A can be coupled to the neutral through one of the clamping diode. The voltage applied to the DC-Capacitor is denoted by E voltage, and it equals half of the total direct current voltage V_d.

The advantages of NPC inverter are:

1. The capacitance requirements of the inverter are less due to the common DC bus. Efficiency is high for fundamental switching frequency. By adjusting the neutral point DC-bus voltage, error in the converter output can be reduced.

In this paper sequence of switching states is done by using space vector modulation technique.

C. Space Vector Modulation Technique:

Advantage of Space vector modulation technique is it has less harmonic and less switching transients. Totally NPC inverter has twenty seven switching states. There are three switching states for each inverter leg. Switching state 1 represents top two switches are turned on and resultant pole voltage is equal to $1/2V_{dc}$.Switching state 0 represents inner two switches are turned on and resultant pole voltage is equal to zero. Conduction of bottom two switches is presented by -1 and resultant pole voltage is equal to $-1/2V_{dc}$ [3] and [4].

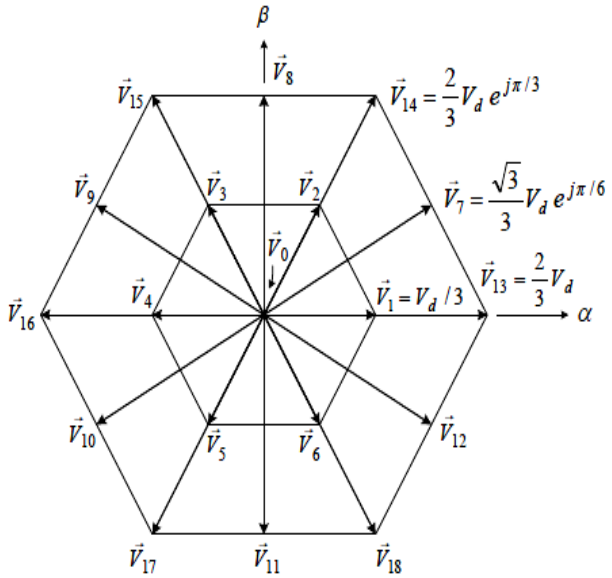

Fig.4. Vector Diagram for different switching states

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Space vector complex representation is given by,

$$U(t) = \frac{2}{3}\left[Ua + Ube^{j(\frac{2}{3}\Pi)} + Uce^{j(-\frac{2}{3}\Pi)}\right] \quad (1)$$

Where 2/3 is a scaling factor.
Modulating reference vectors are represented by

$$Vr\alpha = 2/3[Vra - 0.5(Vrb + Vcr)] \quad (2)$$

$$Vr\beta = \sqrt{3}/3[Vrb - Vrc \quad (3)$$

No power is supplied to the load during the switching states (111), (000), (1,-1,-1).The three major steps to obtain the proper switching states during each sampling period for the SVPWM method are
1) Choose the proper basic vectors.
2) 2nd step is to calculate the dwelling time of each sector.
3) 3rd step is to select the appropriate sequence of sectors

Space voltage vectors of neutral point clamped inverter is classified into large voltage vector, medium voltage vector, small voltage vector and zero voltage vector *(V_o)*. The plane comprises of 6 triangular sectors (I to VI enclosed by solid lines. Each major sector signifies 60'of the fundamental cycle. Major sectors are further divided into four regions. Totally it consists of twenty four switching states and the vertices of These regions represent the voltage vectors. Among the diverse vectors closest to the reference voltage vectors are selected. After choosing the proper sequence, the duty cycle of vector can be calculated.

Switching transitions can be eliminated by proper selection of switching sequence. Only medium and small vector contribute to charging of the capacitors. At ideal conditions the small vectors will cancel each other in every switching period and during one fundamental period medium vector will get cancel each other. The converter will never operate at ideal for balance DC-bus voltage. The several issues like limited switching frequency, the phase currents variation during a fundamental period, variation of reference during a fundamental period, the unsymmetrical nature of electrical parameters, and the switches are not ideal causes unbalance problem.

IV.PROPOSED SYSTEM SIMULATION

The simulation of neutral point clamped inverter fed BLDC motor drive is shown in the fig5.The proposed method is simulated by using MATLAB software.

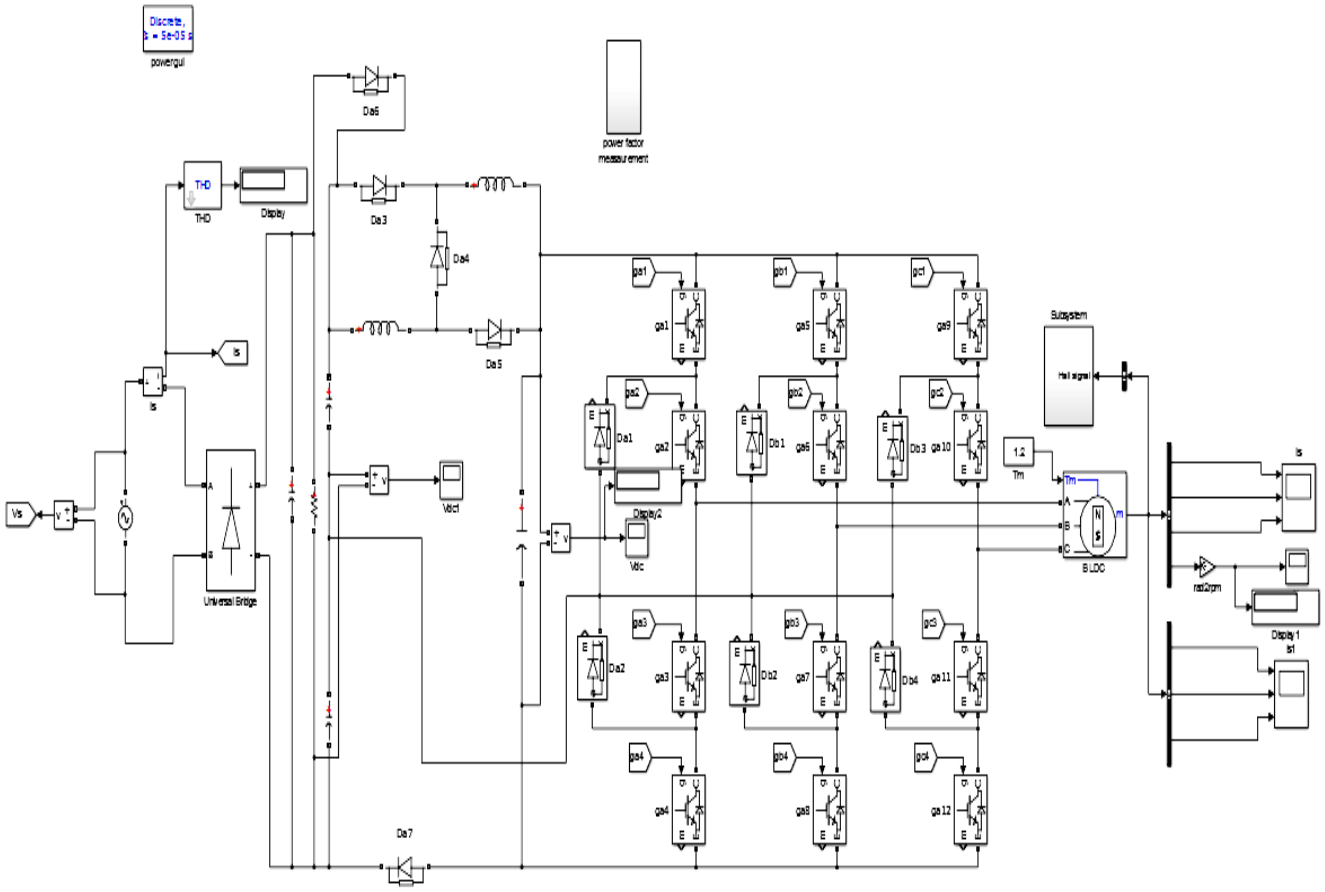

Fig5: Simulation diagram of proposed Technique

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Table 1: Speed, THD, and PF for different input voltages

Input voltage	Speed	THD	PF
55	194.5	13.5%	0.996
68	332.6	17%	0.996
75	438.6	15%	0.996
105	635.2	15%	0.996
170	1148	9%	0.996
240	1710	7%	0.996

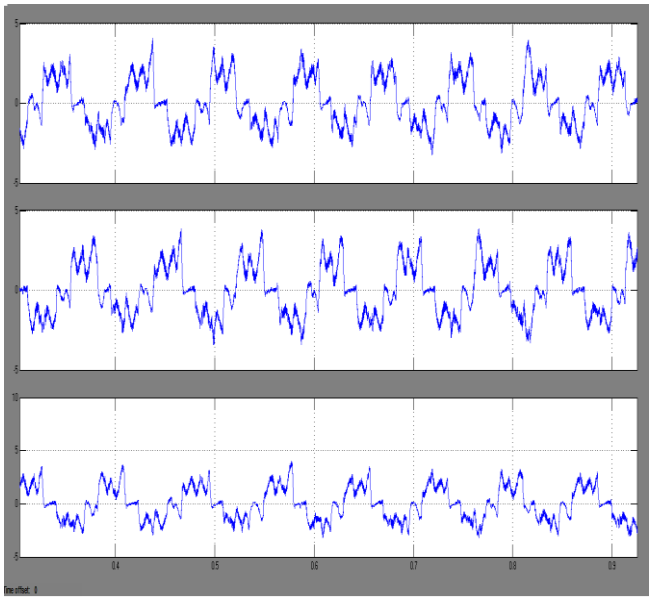

Fig.6. Simulation output of proposed system for 75v input supply

Speed, THD and power factor for different input voltages are noted in the table (I). In the proposed technique THD value is limited upto 7% and power factor is maintained within the unity for different input voltage. Compare to the existing system proposed system has less harmonic distortion and improved power factor for the same speed performance.

V.CONCLUSION

The Z-source inverter based NPC fed BLDC motor drive has been proposed. By proper switching of NPC inverter using space vector modulation technique advantages like voltage boosting, better output spectral quality are achieved. For speed control a satisfactory performance has been achieved and variation in supply voltage is within the acceptable limits of IEC61000-3-2 power quality indices at ac mains.

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BIOGRAPHY

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