Full Custom Design of Low Power 8-bit Magnitude Comparator With Small Transistor Count by Static Cmos

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Abstract— **COMPARATOR is the basic module in digital system. It is widely used in communication and calculation areas. The main objective of this paper is to provide new low power, area solution for very large scale integration (VLSI) designers. We can design the circuits at gate level as well as transistor level but designing the circuits at gate level is never equivalent to designing the circuits at transistor level since transistor level circuit design is lower level of design abstraction when compared to gate level. At circuit level, STATIC CMOS logic style can give better results over others when we design efficiently.In this project the proposed comparator has been designed by using STATIC CMOS 180nm TECHNOLOGY.**

***IndexTerms*—Logicblock,12TCircuit,10TCircuit,Comparator, static cmos,8Tcircuit.**

INTRODUCTION

Low density parity check (Ldpc) was designed by gallager in 1962[1]. Implementation of ldpc decoder consumes more power, comparator is important module in decoder and it is also used in digital system C-H HUANG[2] developed priority encoder based on logic and module. S-W CHENG[3] employed conditional sum adder to design efficient comparator. J-Y KIM and H-J YOO[4] proposed a design without arithmetic operation which is even more efficient.

Now we need to design a comparator by following our own technique such that functionality mismatch should never occur but design constraints like power and area should be achieved. We have designed comparator by using STATIC CMOS logic style, it has advantage of low power consumption but dis-advantage of area with respect to number of transistors, so here we will have the challenge to design the comparator with less number of transistors. Logic style like PTL(Pass Transistor Logic) has advantage of less number of transistors it has the problem of logic level degradation.

I. MAGNITUDE COMPARATOR

Comparator is going to compare 8 bits of A(A7 to A0) and 8 bits of B(B7 to B0) and decides whether ALTB(A<B) or AGTEB(A>=B). we can design the circuit for any of the two outputs means only keeping track of when A is less than B and what are all the conditions which confirms ALTB(A<B) is true then and if ALTB(A<B) is not true then AGTEB(A>=B) is true .we need to know what are all the conditions for ALTB(A<B) to become true, if (A7<B7) then ALTB(A<B) should be true and (A7>B7) status also we need to know in the upcoming condition. so we have designed a sub-circuit for these two conditions that is logic block with a7 and b7 as inputs and this logic block has two outputs , the first output is the condition for (A7<B7) and it is low and this output is being given to one of the inputs of the 8 input nand gate and this nand gate output is the output of the comparator so till now we have designed 1 condition with logic block which has the two outputs.

Now let us see the second condition that is if (A6<B6) and if (A7>B7) is false then ALTB(A<B) should be true, so we have designed a 8T circuit with inputs as A6,B6 and logic block's second output and we also need (A6>B6) status for the upcoming condition and circuit for this is one inverter and one two input nor gate and 8T circuit output is given to the one of the inputs of the 8input nand gate.

Now let us see the third condition that is if (A5<B5) and if (A7>B7) is false and also if (A6>B6) is false then ALTB(A<B) should be true so we have designed a 12T circuit with inputs as A5,B5 and two input nor gate output whose inputs are (A7>B7) status and (A6>B6) status. so first output of 12t circuit is our third condition. we also need (A5>B5) status for the upcoming condition that is the second output of12t circuit.12T circuit first output is given to one of the inputs of the 8input nand gate.

Now let us see the fourth condition that is if (A4<B4) and if (A7>B7) is false , if (A6>B6) is false and if (A5>B5) is false then ALTB(A<B) should be true so we have designed a 10T circuit with inputs as A4,B4,(A7>B7)status , (A6>B6) status and (A5>B5) status. So output of this 10T circuit is our fourth condition. we also need (A4>B4)status for the upcoming condition for that one inverter and one two input nor gate with inputs as A4,B4 has been designed and 10T circuit output is given to one of the inputs of the 8input nand gate.

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Now let us see the fifth condition that is if (A3<B3) and if (A7>B7) is false , if (A6>B6) is false and if (A5>B5) is false and if (A4>B4) is false then ALTB(A<B) should be true so we have designed a 12T circuit with inputs as A3,B3,(A7>B7)status , (A6>B6) status , (A5>B5) status and (A4>B4) status. So the first output of this 12T circuit is our fifth condition.we also need (A3>B3)status for the upcoming condition that is the second output of 12T circuit. 12T circuit first output is given to one of the inputs of the 8input nand gate.

Now let us see the sixth condition that is if (A2<B2) and if (A7>B7) is false , if (A6>B6) is false , if (A5>B5) is false , if (A4>B4) is false and (A3>B3) is false then ALTB(A<B) should be true so we have designed a 10T circuit with inputs as A2,B2,(A7>B7)status , (A6>B6) status , (A5>B5) status , (A4>B4) status and (A3>B3)status . So the output of this 10T circuit is our sixth condition.we also need (A2>B2)status for the upcoming condition for that one inverter and one two input nor gate with inputs as A2,B2 has been designed and 10T circuit output is given to one of the inputs of the 8input nand gate.

Now let us see the seventh condition that is if (A1<B1) and if (A7>B7) is false , if (A6>B6) is false and if (A5>B5) is false , if (A4>B4) is false, if (A3>B3) is false and if (A2>B2) is false then ALTB(A<B) should be true so we have designed a 12T circuit with inputs as A1,B1,(A7>B7)status , (A6>B6) status , (A5>B5) status , (A4>B4) status, (A3>B3)status, and (A2>B2)status. So the first output of this 12T circuit is our seventh condition.we also need (A1>B1)status for the upcoming condition that is the second output of 12T circuit. 12T circuit first output is given to one of the inputs of the 8input nand gate.

Now let us see the eighth condition that is if (A0<B0) and if (A7>B7) is false , if (A6>B6) is false , if (A5>B5) is false , if (A4>B4) is false , (A3>B3) is false, (A2>B2) is false and if (A1>B1) is false then ALTB(A<B) should be true so we have designed a 10T circuit with inputs as A0,B0,(A7>B7)status , (A6>B6) status , (A5>B5) status , (A4>B4) status, (A3>B3)status, (A2>B2)status and (A1>B1)status . So the output of this 10T circuit is our eighth condition.we no need (A0>B0)status as there is no upcoming condition and 10T circuit output is given to one of the inputs of the 8input nand gate.

There are 4 blocks in this comparator named Logic block,8Tcircuit,10Tcircuitand 12Tcircuit. Logic block compares MSB(Most Significant Bit) of A and B that is A7,B7. 8Tcircuit was required for getting the (A6<B6)true condition. 10Tcircuit was required for getting the (A4<B4),(A2<B2) and (A0<B0) true condition. 12Tcircuit was required for getting the (A5<B5),(A3<B3) and (A1<B1) true condition.

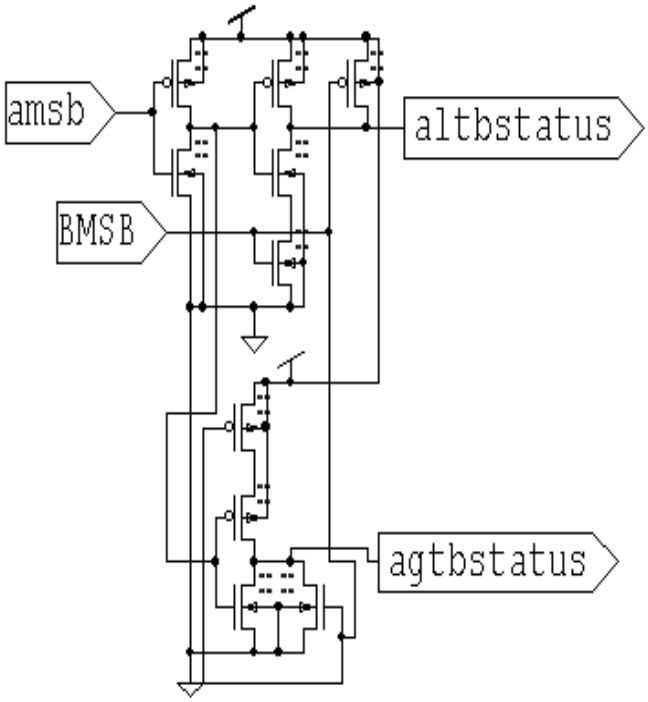

Fig. 1 Logic Block

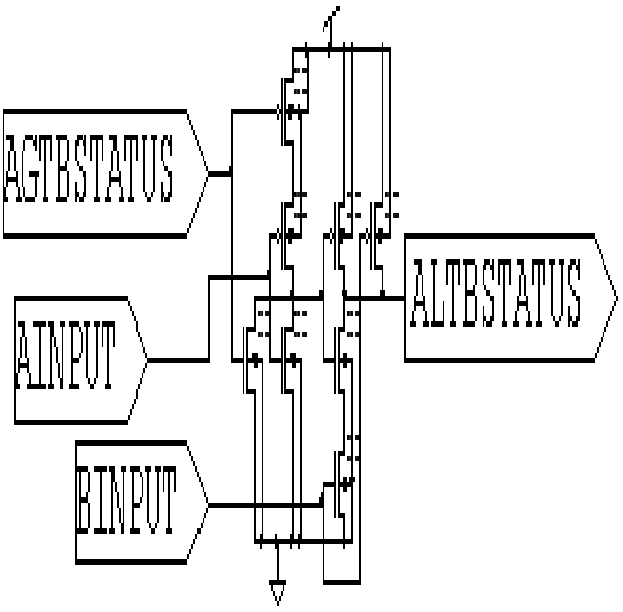

Fig. 2 8T Circuit

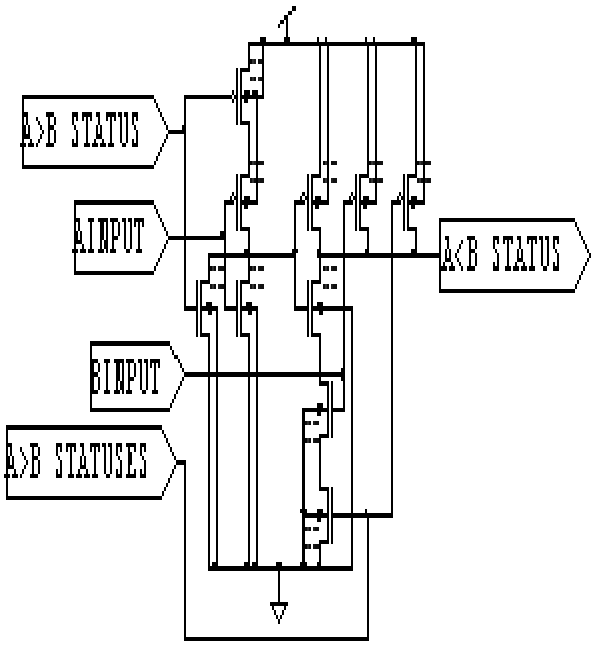

Fig. 3 10T Circuit

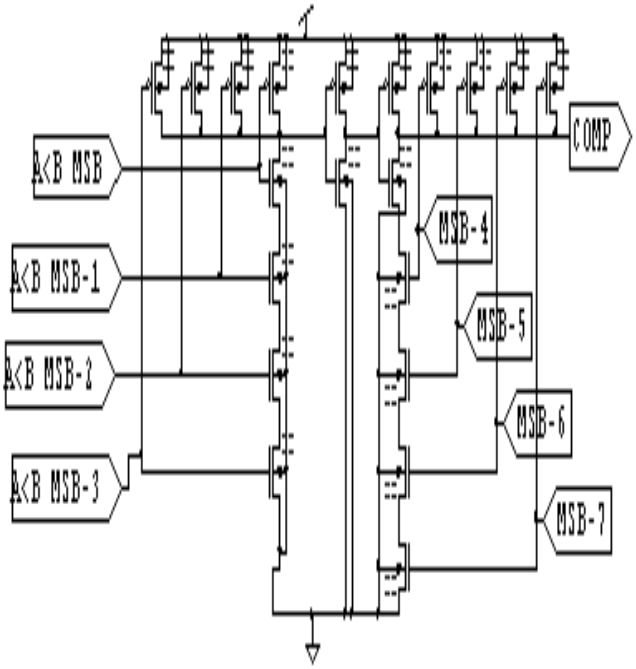

Fig. 5 8input NAND gate

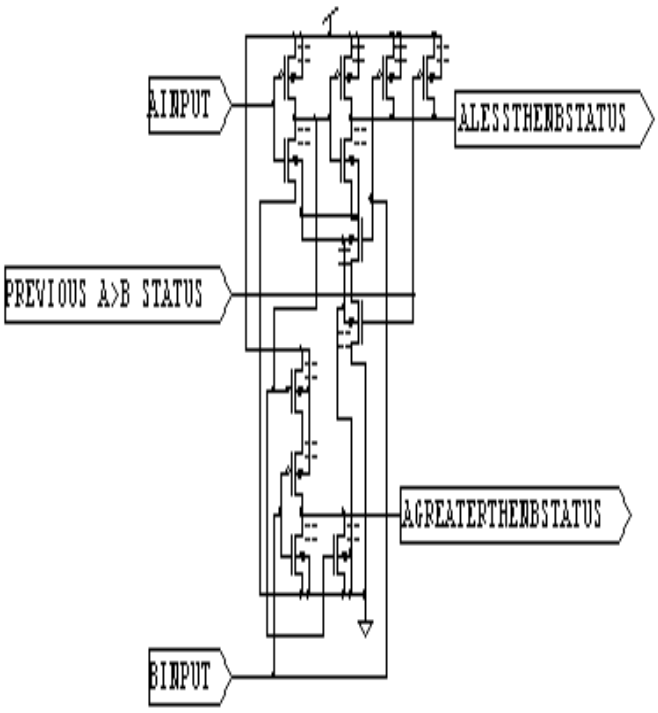

Fig. 4 12T Circuit

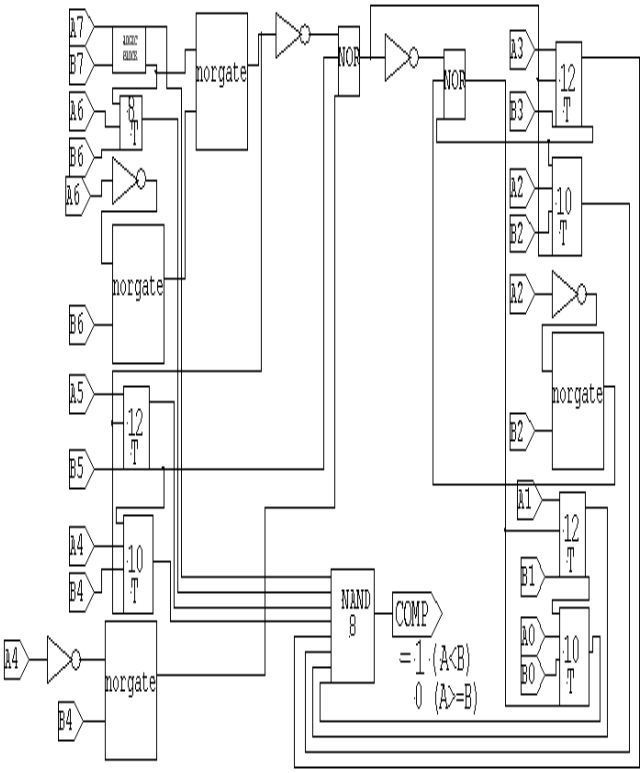

Fig. 3 8-BIT MAGNITUDE COMPARATOR

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Logic block needs 10 number of transistors and 8T Circuit needs eight number of transistors and 12T Circuit needs twelve number of Transistors and 10T Circuit needs ten number of Transistors. Total number of transistors required are one logic block which requires 10transistors,one 8T Circuit which requires 8transistors, three 10T Circuits which requires 30 transistors, three 12T Circuits which requires 36 transistors, six not gates which requires 12 transistors, four 2input nor gates which requires 16transistors, two 3input nor gates which requires 12transistors, one 4input nand gate which requires 8transistors and one 5input nand gate which requires 10transistors.

II. STATIC CMOS

STATIC CMOS has the advantage of low power consumption since if N-MOSFET is on then corresponding P-MOSFET is OFF.STATIC CMOS needs more number of transistors because if we require N-number of TRANSISTORS in the PULL-UP network we also need N-number of TRANSISTORS in the PULL-DOWN network. STATIC CMOS has advantage of full output voltage swing, so these full voltage levels can make sure in the upcoming section's N-MOSFET'S and P-MOSFET'S fully on or off. we can easily differentiate between output voltage high logic level and output voltage low logic level and this will be even more beneficial when the technology is scaled down. Even though it is recommended that not more than 4 number of transistors should be in series either in PULL-UP or PULL-DOWN region as delay is going to be worse. We need to sacrifice the speed in particular section of the circuit for achieving the AREA benefits.

Here the challenge also Lies in Designing the layout for comparator by doing some exclusive work on maximum possible layout sketches for individual cells and then finally select the best one for an individual cell so that the final layout can achieve optimal design constraints using STATIC CMOS cells and Advantage of using STATIC CMOS only is we can Merge the cells comfortably so that unnecessary spacing between the cells can be minimized

III. PERFORMANCE ANALYSIS

Implementation of 8-bit magnitude comparator has been done using STATIC CMOS logic style. Table1 shows AREA comparision of IMPROVED HYBRID and STATIC CMOS. power dissipation comparision for 8-bit magnitude comparator using IMPROVED HYBRID and STATIC CMOS for various supply voltage(VDD) are shown in TABLE2. This table clearly shows that STATIC CMOS has very less power dissipation than IMPROVED HYBRID over various supply voltages(VDD). The comparator which we designed using STATIC CMOS logic style uses less number of transistors. It uses 7.7% less area(number of transistors) than IMPROVED HYBRID.

TABLE1 COMPARISION OF AREA IN TWO DESIGNS

	Design in reference (Improved hybrid)	Design in this paper (Static cmos)
Area(number of transistors)	154	142

TABLE2 COMPARISION OF POWER IN TWO DESIGNS

VDD(V)	Average power consumption(μ W)	
	Design in reference (Improved hybrid)	Design in this paper (Static cmos)
1.4	21.4	0.077
1.2	12	0.056
1	6.05	0.038

IV. CONCLUSION

Power is becoming an important design constraint these days especially because of the battery operated devices as well as Area which in turn directly proportional to Cost of the Design one would always wants to buy a product with low cost and we can also incorporate additional functions with in the prescribed Area.we came with our own Design it was possible because of the FULL-CUSTOM Design which allows us to Design our own circuit by taking the leaf level cells as gates or may be Transistors since our Design is implemented in Transistors we have been able to acheive area and power constraints, even though we want Speed also to be more it might not be possible always . we have designed our comparator by using STATIC CMOS logic style which generally requires more number of transistors.

we are able to design the comparator by using less number of transistors than IMPROVED HYBRID which is a mix of HYBRID PTL / CMOS logic style. It shows an 8-bit comparator of the proposed technique only needs 142 transistors, the technique which we presented can be easily extendable up to 64-bit with some Design Techniques to be implemented to ensure that Delay is not worse.

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