SPEED ENHANCEMENT IN 64 - BIT PARALLEL PREFIX VLSI ADDER USING AN EFFICIENT METHOD

B.Lokeswar Reddy , G.Reddi Basha , G.Ganga Basha

Abstract— High speed computation is an important parameter to evaluate the overall performance of computing devices. To manipulate the addition operations with more speed and accuracy parallel prefix addition is a better method. In this paper a 64-bit parallel prefix addition is implemented with the help of cells like black cell and grey cell for carry generation and propagation. This process will gives high speed computations with high fan-out and makes carry operations easier. Xilinx 14.5 vivado tool has been used for the simulation of proposed 64-bit adder. A comparison is made with the help of various range of inputs and also it has been made as efficient as possible in terms of number of transistors , their topology and number of nodes than comparing to previous versions. A clear cut comparison is made with the past techniques involved in the parallel prefix adders for VLSI circuits in terms of power consumption, propagation delay, Logic levels, fan out, number of nodes.

Index Terms— Parallel prefix adder, propagation delay, black cell, carry propogation , grey cell.

I. INTRODUCTION:

High speed applications like digital signal processing microprocessors and mobile devices mostly based on addition process.The main objective of parallel adder is to minimize the logic complexity and delay by improving the performance of the system with the factors like area and power.High performance computations can be performed with the help of parallel prefix adder based on the implementation of carry look ahead adder.The transistor topology is different from carry look ahead adder.The carry generation and propogation is unique in this type of adder.The objective of the parallel prefix adder is to implement the n-bit addition process in VLSI technology .Since 20 years parallel prefix adders are famous for their high speed.Addition is performed in three steps.Initially carry is generated and propogated by using input bits. Next all the carry signals are calculated in parallel. Finally obtaining the sum of the inputs. The system consists of AND, OR and XOR gates. Propogation of carry to a corresponding stage . Black cell consists of two AND gates and one OR gate and grey cell consists of one OR gate and one AND gate.

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B.Lokeswar Reddy*, Assistant professor, Department of ECE,GVIC,madanapalli, India.*

G.Reddi Basha*, Assistant professor, Department of ECE,SVIST ,Kadapa, India.*

G.Ganga Basha, *M.Tech. student, Department of ECE, GVIC, madanapalli, India.*

II. WORKING SCENARIO OF PARALLEL PREFIX ADDER:

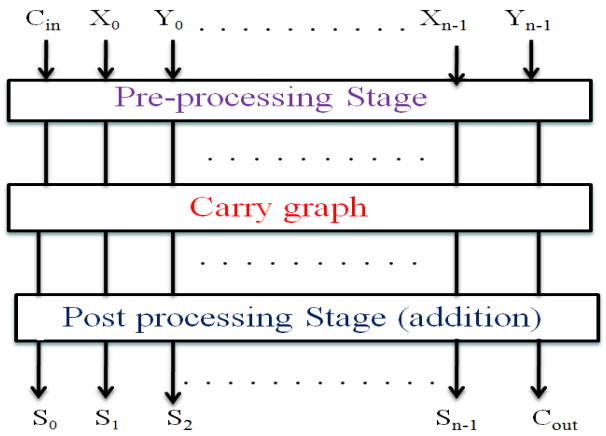


Fig.1: Working Scenario of parallel prefix adder

III. EXISTED PARELLEL PREFIX ADDERS:

Design of prefix addition network specifies the model of parallel prefix adder. The parallel prefix adder given by Kogg Stone gives low fan-out and high logic depth which leads to a complex network of prefix addition and also contains more number of interconnections. Brent Kung adder design gives minimal number of calculating nodes, but the design itself has maximum logic depth. The area will be reduced due to number of nodes but complexity will be high due to high logic depth. Han-Carlson adder design is the combination of both Brent Kung and Kogg Stone adders, which gives balance between nodal count and logic depth. Knowles also presented an adder design, which gives low logic depth and improved fan-out. There is another adder which combines the benefits of prefix addition and Carry save adder i.e. sparse tree binary adder. Sklansky developed a topology which leads to low depth in the interconnecting nodes. Ladner and Fischer proposed a general design to construct a parallel prefix network with high depth when compared with Sklansky topology but achieved maximum fan-out for the critical path. Integer linear programming is

also another method for parallel prefix computation. Mathew Ziegler and Mircea Stan proposed an adder for parallel prefix computation for minimizing delay and area known as best logarithmic adder for fan-out of two. There are some more adders designed by Haiku Zhu, Chung-Kuan and Ronald Graham, can produce minimal depth for n-bit adder. The proposing adder is about 64-bit adder with parallel prefix computation which is closely related to Ladner and Fischer adder.

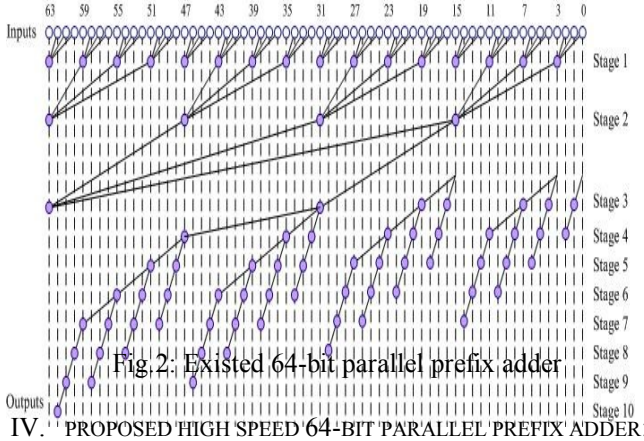


Fig.2. Existed 64-bit parallel prefix adder

IV. PROPOSED HIGH SPEED 64-BIT PARALLEL PREFIX ADDER:

The proposed high speed 64-bit parallel prefix adder is shown fig 2. Main theme of the design is to eliminate huge delays in overall for carry calculations. So the logic depth of the proposed design is optimal.The 64-bit parallel prefix adder has seven stages of computations. Design of parallel prefix adder can be implemented with the help of CMOS logic, but CMOS logic constructs only inverting functions so that cascading odd cells and even cells alternatively gives the result of eliminating inverters between those two cells. Two inputs of each stage will be given to XOR gate and AND gate such that itlooks like a half adder circuit. In the first stage we calculate all 64-bit inputs with the help of half adders such that the results will be propagated towards next stages. Subsequent stages follows the same procedure so as the number of half adders will be reduced stage by stage. Each half adder consist one AND gate, which requires five transistors and XOR gate requiresthirteen transistors so that each half adder requires 65 transistors. The topology of the design must be simple to reduce the logic depth, because each input again requires one buffer for impedance matching. So we are going to use cells like black, grey and white cells for the reduction of number of transistors. White cell is a half adder and black cell consists one OR gate and two AND gates and grey cell consists of one OR gate and one AND gate. By all means we reduced transistor count,which also leads to low power and low area specifications.In the proposed 64-bit parallel prefix adder logic cells has been preferred, depending upon the stage we use number of logic cells. The final stage of the design gives the sum signal as oneoutput and carry signal as other output. The stages at both ends can be operated with high speed because of simple topology in the network. Amid, all of this the performance depends on the intermediate stages. We also compared Brent Kung and Ladner Fischer adders for n-bit at various values of n, like propagation delay and network complexity. The proposed adder is as shown in Fig.3, which can overcome various problems in existed adders like shown in Fig.2.

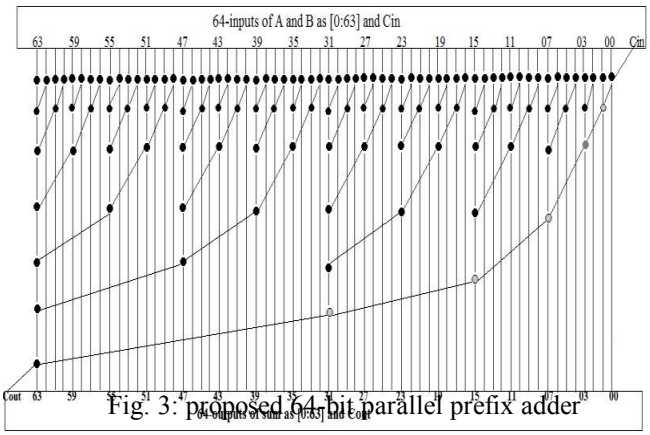


Fig. 3: proposed 64-bit parallel prefix adder

V. ESSENTIAL LOGICAL BLOCKS IMPLIMENTED:

A. BLACK CELL :

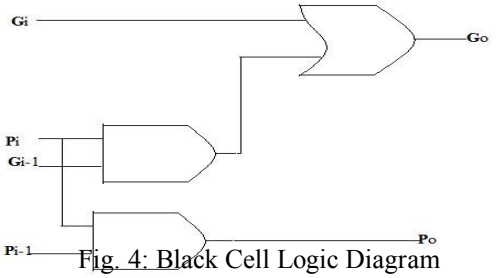


Fig. 4: Black Cell Logic Diagram

The Boolean equations for the above logic diagram of black cell are

(1) Go = Gi +Pi.Pi-1;
(2) Po = Pi.Pi-1

B. GREY CELL :

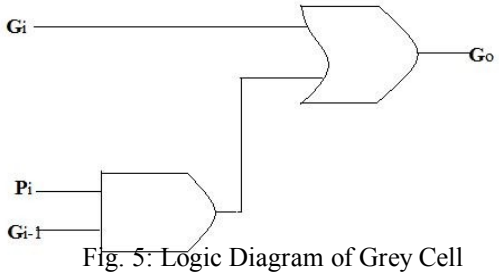


Fig. 5: Logic Diagram of Grey Cell

The Boolean equation of the above logic diagram of grey cell is

Go = Gi+Pi.Pi-1

The two cells shown in the figures 4 and 5 are for the purpose of reducing number of transistors such that the logic will become simple and the number of transistors be also reduced. Black cell gives two outputs one for normal sum and the other is for propagation of carry.

C. WHITE CELL :

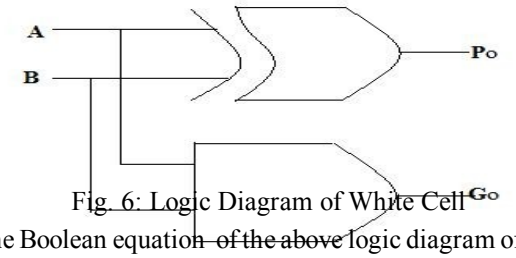


Fig. 6: Logic Diagram of White Cell

The Boolean equation of the above logic diagram of white cell is

Po = AB′+A′B; Go = AB

The simulation results shown in Fig.6 gives complete idea about the design of proposed 64-bit parallel prefix adder and also gives the values like propagation delay and logic depth. The values shown in the table are obtained from the code and simulation results. We also compared those results with the existed adders like Brent Kung, Kogg Stone and etc. so that the comparison describes the efficiency of the proposed 64-bit parallel prefix adder. Chart of the simulated results is a pictorial representation of the design's comparison is also shown. Transistor count also reduced such that the logic depth and propagation delay reduced as in the followed charts.

Table1: Comparison table with output results

Parameter	Existed adder	Proposed adder	comparison
Delay in ns	>1280(B.K.)	1280	reduced
Logic depth	High (B.K.)	Low (B.K.)	reduced
Transistor count	>2500	1800	reduced

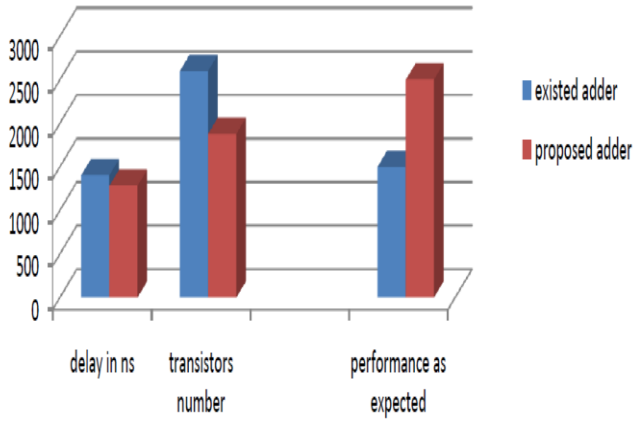
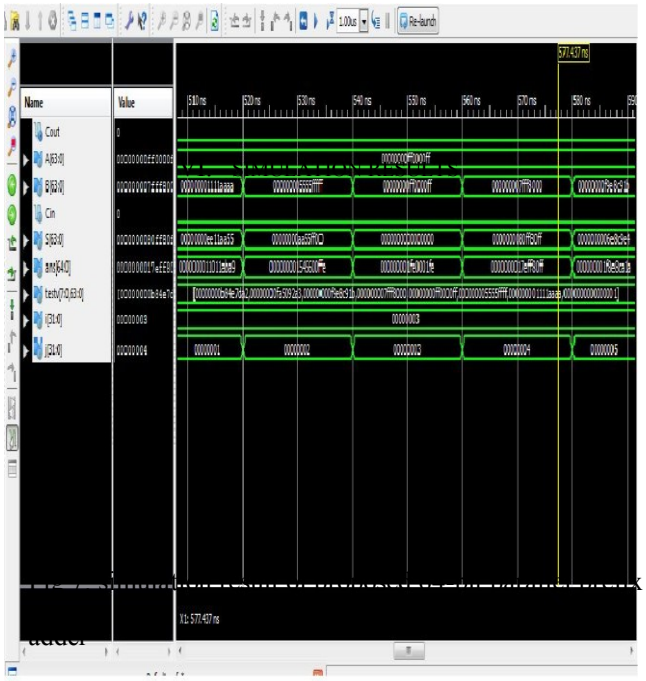


Chart1: Comparison chart in pictorial representation



VII. CONCLUSION

The parallel prefix adders design is an efficient method of all conventional adders. Proposed 64-bit high speed parallel prefix adder has achieved the low propagation delay by overcoming the problems in previous adders like 16-bit, 32-bit Brent Kung and Ladner and Fischer designs. The performance has been compared at various input ranges by keeping trade-off between propagation time and logic depth, and also achieved high fan-out. The proposed 64-bit high speed parallel prefix VLSI adder made the computation in seven numbers of stages and also generated sixty three outputs with the help of 845 nodes. We have used Xilinx 14.1 vivado version tool for the purpose of simulating the Verilog code. The simulation result of proposed 64-bit parallel prefix adder has proved the efficiency of the design. This design is a conventional one for the purpose of arithmetic and logic calculations at wide and complex range of inputs. The proposed design is also preferable for multipliers and for various data computations , applications and extensions.

REFERENCES

[1] R.Zimmermann' Binary Adder Architectures for Cell-Based VLSI and their Synthesis' ETH Dissertation 12480' Swiss FederalInstitute of Technology' 1997.

[2] R.P Brent and H.T Kung 'A regular layout for parallel adders' IEEE Trans., C-31(3):260-264, March 82

[3] R.Ladner and M. Fischer' "Parallel prefix computation"'Journal of ACM. La Jolla' CA' vol.27' no.4' pp. 831-838' October 1980.

[4] J. Sklansky' "Conditional sum addition logic"' IRE Transactions on Electronic computers. New York' vol. EC-9' pp. 226-231' June 1960.

[5] P.Kogge and H.Stone' "A parallel algorithm for the efficient solution of a general class of recurrence relations"' IEEE Transactions on Computers' vol C-22' no.8' pp.786-793' August 1973.

[6] P.Ramanathan' P.T.Vanathi' "A Novel Logarithmic Prefix Adder with Minimized Power Delay Product"' Journal of Scientific & Industrial Research' Vol. 69' January 2010' pp. 17-20.

[7] T. Han and D. Carlson' "Fast area efficient VLSI adders'" Proceedings of the Eighth Symposium on Computer Arithmetic. Como' Italy' pp.49-56' September 1987. (Pubitemid 17613979)

[8] S.Knowles' "A family of adders'" Proceedings of the 15th IEEE Symposium on Computer Arithmetic. Vail' Colarado' pp.277-281' June 2001.

[9] David Harris' "A Taxonomy of parallel prefix networks'" Proceedings of the 37th Asiloma Conference on Signals' Systems and Computers acific Grove' California' pp.2213-2217' November 2003.

[10] Andrew Beaumont-Smith' and Cheng-Chew Lim' "Parallel Prefix Adder Design'" Department of Electrical and Electronic Engineering' the University of Adelaide' 2001.

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AUTHOR'S BIOGRAPHY:

AUTHOR 1:

B. Lokeswar Reddy,Graduate in ECE from KSRM College of Engineering,Kadapa, affiliated to JNTU Ananthapur. Obtained M.Tech. Degree in VLSI system Design from AVR & SVR college of engineering,Nandyal, affiliated to JNTU Ananthapur.Working as Assistant Proffessor in GVIC, Madanapalli, A.P.satate,India.

AUTHOR 2:

G.Reddi Basha , Graduate in ECE from SVCET,Chithoor, affiliated to JNTU Hyderabad. Obtained M.Tech. Degree in Digital Electronics and Communication Systems (DECS) from MITS , Madanapalli, affiliated to JNTU Ananthapur .Working as Assistant Proffessor in SVIST,Kadapa,A.P.satate,India.

AUTHOR 3:

G.Ganga Basha, Graduate in ECE from VITS,proddatur, affiliated to JNTU Anantapur. Persuing M.Tech. in VLSI & ES (2012-2014) in GVIC, Madanapalli, affiliated to JNTU Ananthapur , A.P.satate,India.