VLSI Design and Performance Analysis of Different Full Adder Topologies at 0.25 Micrometer Technology Node

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Abstract— **Full Adders are the most important components in digital design which not only perform addition operations, but also helpful in calculating several other functions such as subtraction, multiplication and division operations. Different types of adders are frequently essential in VLSI technology according to the requirement *in* processors to ASICs. In modern research we have found that Complementary Pass transistor Logic (CPL) is much more power-efficient than complementary *CMOS*. In this paper describes the power consumption and propagation delay of one-bit CMOS (Complementary MOSFET) full adder, CPL(Complementary Pass Transistor Logic) full adder, Domino logic full adder, and Transmission gate full adder designed using TANNER EDA, using 0.25 micrometer technology node with different CMOS logic design styles. When a feasible layout is found, the layout mask layers are drawn using a layout editor tool according to the layout design rule. The actual performance of the circuit can be determined by performing a SPICE simulation. It is reported that for Transmission gate full adder the parameters like Dynamic and Static Power consumption and total propagation delay is less, for a particular aspect ratio, so the Transmission gate full adder is much better for use in VLSI technologies.**

Index Term --- One-Bit CMOS full Adder, Domino Logic Full adder, CPL full adder, Transmission Gate Full adder, CMOS logic design style.

I. INTRODUCTION

Today the demand of low-power Very Large Scale Integration (VLSI) as well as minimum area design is increasing at very high rate. Reduction of power consumption makes a device more consistent. The need for devices that consume a minimum amount of power was a major driving force behind the fabrication of CMOS technologies. At the circuit level design, there are so many choices for power savings exists for implementing combinational circuits. This is because all of the important parameters governing power dissipation—switching capacitance, transition activity, and short-circuit currents—are strongly subjective by the chosen logic style.

Depending on the application, this type of circuit design to be implemented, and this design technique used, different performance parameter become more important. In the previous study in past, the parameters like high speed, low cost and small area were the major issues of concern, but due

to great demand of low power devices power Considerations are now gaining the attention of the community associated with VLSI design. In recent years, the growth of fast computing devices and wireless communication systems has made power dissipation a most critical design parameter [6]. In the absence of low-power design techniques circuits generally suffer from very short battery life, while packaging and cooling them would lead to an unavoidable increase in the cost of the product. In addition, reliability is strongly affected by power consumption. The High power dissipation is also associated with high temperature operation, which, in turn, may well tend to the failure mechanisms in the system. Two components determine the power consumption in a CMOS circuit:

1. Dynamic power consumption
2. Static power consumption

CMOS devices have very low static power dissipation, which is the result of leakage current. This power consumption occurs when all inputs are held at some valid logic level and the circuit is not in the charging states. But, when switching at a very high frequency, dynamic power consumption can contribute considerably to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption. Dynamic power dissipation occurs when the circuit is operational, whereas static power dissipation becomes an issue when the circuit is in off state or is in a power-down mode. There are three major sources of power dissipation in digital CMOS circuits, which are summarized in following equation:

$$P_{tot} = P(dynamic) + P(static) \qquad (1)$$

The first term represents the switching component of power, where CL is the load capacitance, f_{clk} is the clock frequency.

$$Pd = CL * VDD^2 * f_{clk} \qquad (2)$$

Where

Pd = transient power consumption
VDD = supply voltage

The second term is due to the direct-path short circuit current, Isc, which arises when both the NMOS and PMOS transistors are simultaneously in active condition, conducting current directly from the supply to the ground.

Finally, the leakage current $I_{leakage}$ which can arise from substrate injection and sub-threshold effect is primarily determined by fabrication technology considerations. The switching power dissipation in CMOS digital integrated circuits is a strong function of the power supply voltage.

$$I_{leakage} = Is * e\ (qv/kT-1) \qquad (3)$$

Where
Is = reverse saturation current v = diode voltage

k = Boltzmann's constant (1.38 *10−23J/K).

$$PS = V_{DD} * I_{SC} \qquad (4)$$

Where
VDD = supply voltage
Isc= current into a device (sum of leakage currents)

Therefore, reduction of VDD emerges as a very effective means of limiting the power consumption. However, the saving in power dissipation comes at a significant cost in terms of increased circuit delay. Since the exact analysis of propagation delay is quite complex, a simple first order derivation [7] can be used to show the relation between power supply and delay time.

$$Td = CL * VDD/ (K*VDD-VTH)^{\alpha} \qquad (5)$$

Where
K = Transistor's aspect ratio (W/L)
VTH = Transistor threshold voltage
α = Velocity saturation index which varies between 1 and 2.

Unfortunately, reducing the supply voltage reduces power, but when the supply voltage is near to threshold voltage, from equation (5), the delay increases drastically [8]. Section II, gives the four important adder architectures, designed in this paper for W/L ratio of 1.5 for NMOS and 3 for PMOS and supply voltage is 1.8V in all cases. Results of quantitative comparisons based on simulations of different adder architectures by using different logic design styles are given in section III. Some conclusions and references are finally drawn in Section IV and V, respectively.

II. LOGIC DESIGN STYLE

A. CMOS Full Adder:

The conventional CMOS full adder has 28 transistors and is based on the regular CMOS structure. The CMOS full adder circuit is shown in Fig. 1.A 1-bit full adder has three 1-bit inputs (a, b, and c) and two 1-bit outputs (sum and carry). The relations between the inputs and the outputs are expressed as:

Sum = A ⊕ B ⊕ Ci   (a)
Carry = A ∗ B + B ∗ Ci + Ci∗ A   (b)

The CMOS structure combines PMOS pull-up and NMOS pull-down networks to produce considered outputs. In this style all transistors (either PMOS or NMOS) are arranged in completely separate branches, each may consist of several sub-branches [1]. Mutually exclusiveness of pull-up and pull-down networks is of a great concern. Advantages of the CMOS logic style are its robustness against voltage scaling and transistor sizing (high noise margins) and thus reliable operation at low voltages and arbitrary (even minimal) transistor sizes (ratio less logic) [2].Disadvantage of complementary CMOS is the substantial number of large PMOS transistors, resulting in high input loads.
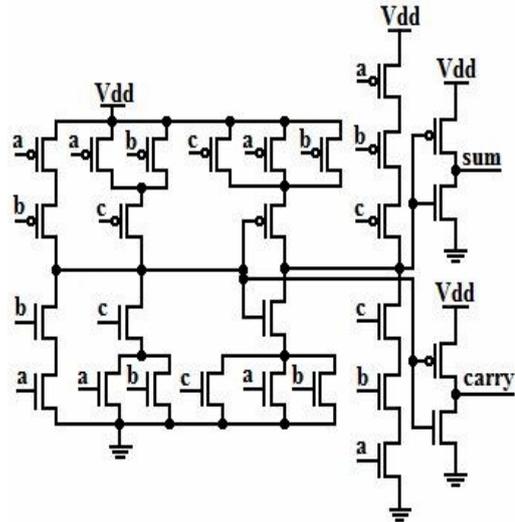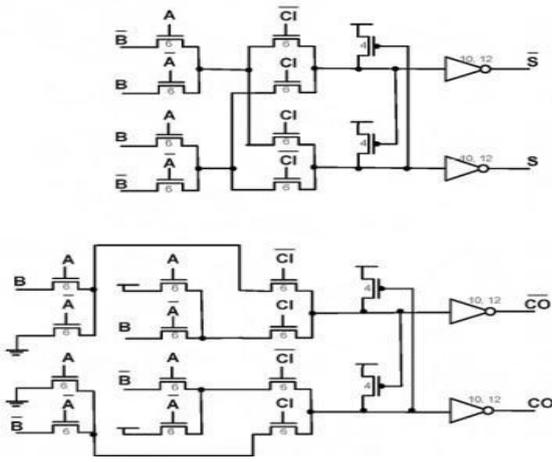

Fig. 1 CMOS Full Adder [8]

B. Complementary Pass Transistor Logic -CPL Full Adder:

The complementary pass-transistor logic (CPL) full adder has 32 transistors and is based on the CPL logic. A CPL logic full adder circuit is shown in Fig. 2. In the circuit, there are two small pull-up PMOS transistors for swing restoration in the Sum output signal and the complementary Sum output signal, and another two small pull-up PMOS transistors for swing restoration in the Carry output signal and the complementary Carry output signal [2].CPL full adder provides high-speed, full-swing operation and good driving capabilities due to the output static inverters and fast differential stage of cross coupled PMOS transistors .Due to the presence of lot of internal nodes and static inverters, there is large power dissipation [4].

The differential stage, on the other hand, leads to considerably larger short- circuit currents. Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs. The advantages [3], of pass logic transistors include smaller number of transistors and smaller input loads, along with MUX and especially XOR circuits being implemented efficiently. The disadvantage, of pass transistor logic is that Threshold voltage drops through the NMOS transistors makes it necessary to maintain IAIN output voltage level; as a result inverter is used at output which increases the number of transistors.

C. Transmission Gate Full Adder (TGA):

The transmission-gates CMOS (TGCMOS) full adder has 20 transistors and is based on transmission gates. The transmission gate full adder circuit is shown in Fig 3.These adders are inherently low power consuming and are good for designing XOR or XNOR gates. The main disadvantage of this logic style is that they lack driving capability [4]. When transmission gate full adders are cascaded, their performance parameters degrade significantly. Transmission gate full adder produces buffered outputs of proper polarity for both the sum and carry. The circuit is simpler than the conventional full adder. It uses complimentary properties of NMOS and PMOS transistor. It is built by connecting a PMOS transistor and an NMOS transistor is in parallel, these are controlled by the complementary control signals. Both the PMOS and NMOS transistors will provide the path for the input logic "1" or "0", respectively, when the NMOS and PMOS are turned on simultaneously. Thus, there is no voltage drop problem occurred whether the 1 or the 0 is passed through it.
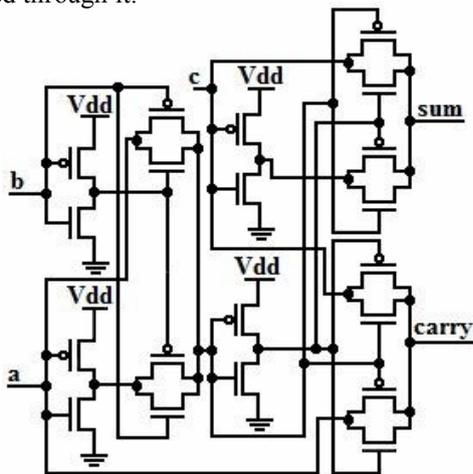

Fig. 3 Transmission Gate Full Adder [8]

D. Domino Logic Full Adder (DLA):

Domino logic is a CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. It allows a rail-to-rail logic swing. The Dynamic Domino, circuits operate using a sequence of pre-charge and evaluation phases orchestrated by the system clock signal as in Fig. 4. Domino gates are faster than their complementary

CMOS counterparts but, on the other hand, they are more susceptible to input noise. This is due to the leakage currents flowing through the Pull down network, which can cause an unwanted discharging of the dynamic node. Dynamic domino gates have the severe limitation of not being able to implement inverting logic functions (such as NOR, NAND, XOR) and high power consumption due to clock [5]. Advantages of this type of adder are that they have smaller areas than conventional CMOS logic. This type of adders may have charge distribution problem. Operation is free of glitches as each gate can make only one transition.
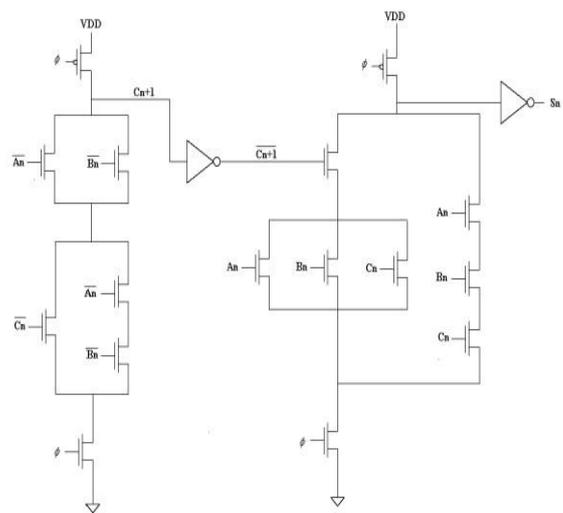

Fig. 4 Domino Logic Full Adder

TABLE I.
Comparison of Various Parameters

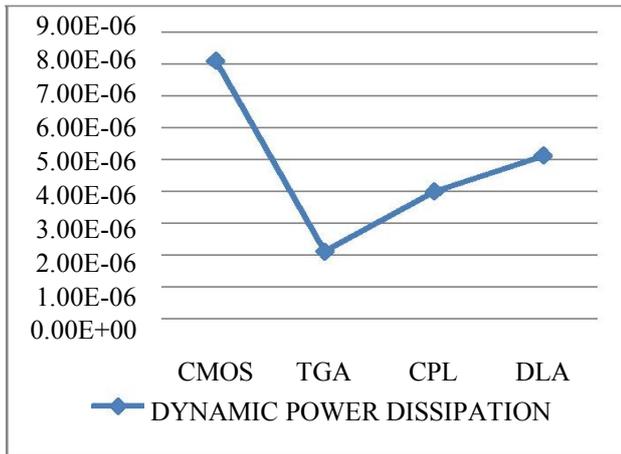| Full Adder Type	Dynamic PD (in watts)	Static PD (in watts)	PD Sum (in sec)	PD Carry (in sec)
CMOS	8.11E-6	2.01E-10	1.76E-10	1.00E-8
CPL	3.99E-6	2.52E-10	1.71E-10	1.00E-8
TGA	2.11E-6	1.82E-10	5.91E-10	1.00E-8
DLA	5.12E-6	NA	8.01E-11	3.01E-8

III. GRAPHICAL REPRESENTATION OF RESULT

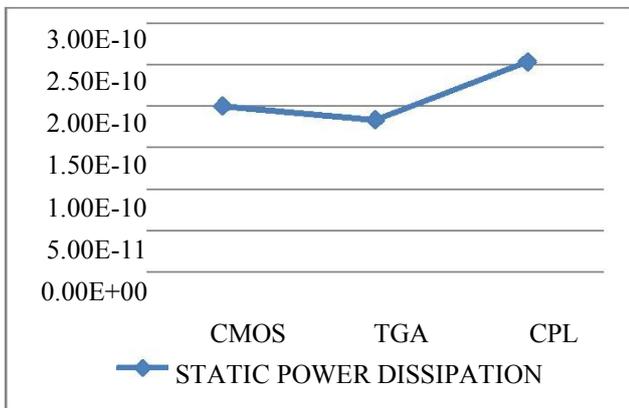Fig. (a) Dynamic Power Dissipation
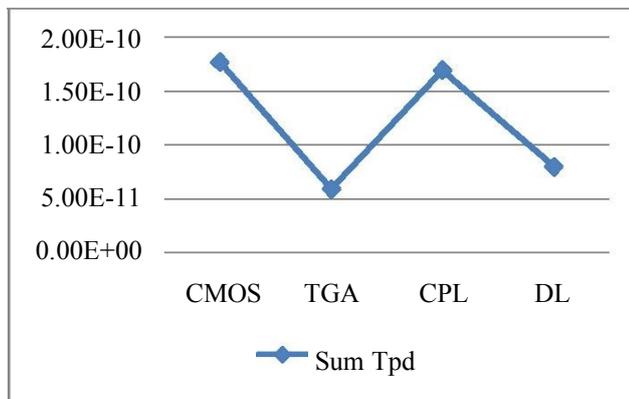

Fig. (b) Static Power Dissipation
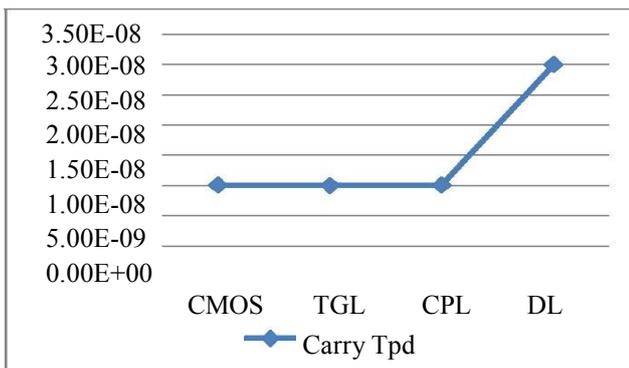

Fig. (c) Sum Propagation Delay

Fig. (d) Carry Propagation Delay

IV. CONCLUSION

From the simulation results it is observed that Transmission Gate Full Adder is the most efficient adder since it has the minimum power dissipation and delay. As a result it is the fastest adder among CMOS, DLA TGA and CPL. Dynamic power consumption can be decreasing by reducing the voltage supply, switched capacitance, and frequency at which the device logic is clocked. CMOS Power consumption for full adder topologies is the function of load capacitance, frequency of operation, and voltage supply.

A reduction of any one of these is beneficial. A reduction in CMOS power consumption provides several benefits like minimum heat are generated, which reduces the problems associated with high temperature, such as this required need for the heat sinks. This provides the user with a product that costs less. In addition to the reliability of the system is increased due to lower-temperature stress gradients on the device. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

REFERENCES

[1] Mahnoush Ruholamini, Amir Sahafi, Shima Mehrabi and Nooshin Dadkhahi Researches and Sciences Center of Hesarak, Tehran, Iran, "Low-Power and High-Performance 1-BitCMOS Full-Adder Cell", *Journal of computer*,vol.3, no. 2, Febuary 2008 .

[2] Reto Zimmermann and Wolfgang Fichtner, *Fellow,IEEE "*Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic", *IEEE journal of solid state circuits*, vol. 32, no. 7, July 1997.

[3] Lixin Gao, "High Performance Complementary Pass Transistor Logic Full Adder", *International Conference on Electronic & Mechanical Engineering and Information Technology*, Guangdong Jidian Polytechnic, China, 2011.

[4] Vahid Foroutan, Keivan Navi and Majid Haghparast, "A New Low Power Dynamic Full Adder Cell Based on Majority Function", *World Applied Sciences Journal* 4 (1): 133-141, 2008 ISSN 1818-4952, Islamic Azad University and Shahid Beheshti University, Tehran, Iran.

[5] Sun,S., and Tsui,P., "Limitation of CMOS supply-voltage scaling by MOSFET threshold voltage*", IEEE Journal of Solid-State Circuits*, Vol. 30, pp. 947-949, 1995.

[6] Vivek Kumar, Vrinda Gupta, Rohit Maurya, "A Study and Analysis of High Speed Adders in Power-Constrained Environment", *International Journal of Soft Computing and Engineering (IJSCE*) ISSN: 2231-2307, Volume-2, Issue-3, July 2012.

[7] Chandrakasan, A. Brodersen, "Low Power Digital Design",Kluwer Academic Publishers, R., 1995.

[8] Reza Faghih Mirzaee, Mohammad Hossein Moaiyeri, Keivan Navi, "High Speed NP-CMOS and Multi- Output Dynamic Full Adder Cells",*International Journal of Electrical and Electronics Engineering*, 4:4 2010.