TEST OF ERROR INTRODUCING IN FLASH ADC

Navneet Nagar, Prof. R.B. Gaikwad

Department of Electronics and communication Engineering, Ujjain Engineering Collage, Ujjain, M.P. (India)

Abstract: **This paper is proposed for BIST scheme for ADC static testing Data acquisition time and accurate instrumentation are the most significant contributors to ADC test cost. For most ADC products, static linearity (INL/DNL) test is required. This paper presents a methodology for estimating an ADC's dynamic performance from its tested INL data, without requiring additional data acquisition or additional accurate sinusoidal sources. The tested INL(k) data is used to compute the power at harmonic frequencies. Memory and computation requirement is very small comparing to that in traditional spectral testing.**

When combined with a BIST approach for INL testing, this method offers a very low cost BIST solution to ADC dynamic performance testing.

1. INTRODUCTION

The A/D converters play an important role between analog and digital signals. The flash ADC is a frame of AD converters having very high data conversion speed , low-resolution and large chip area along with large power dissipation. The flash ADC architecture uses 2"-1comparators to convert an n-bit data without the requirement of sampling-and-hold circuits. Fig. 1 shows an example of a traditional flash ADC architecture.

Analog-to-digital converters are essential building blocks in modern electronic systems. They form the critical link between front-end analog transducers and back-end digital computers that can efficiently implement a wide variety of signal-processing functions. The wide variety of digital-signal-processing applications leads to the availability of a wide variety of analog-to-digital (A/D) converters of varying price, performance, and quality. Ideally, an A/D converter encodes a continuous-time analog input voltage, VIN, into a series of discrete N-bit digital words that satisfy the relation much power consumption.

$$VIN = VFS \sum_{K}^{N-1} \frac{b_k}{2^{k+1}} + E$$

Where VFS is the full-scale voltage, b_k are the individual output bits, and ² is the quantization error. This relation can also be written in terms of the least significant bit (LSB) or quantum voltage level

$$VQ = VFS/2\text{^}N = 1\ LSB$$

$$\text{As } VIN = VQ \sum_{k=0}^{N-1} bk * 2^k + E$$

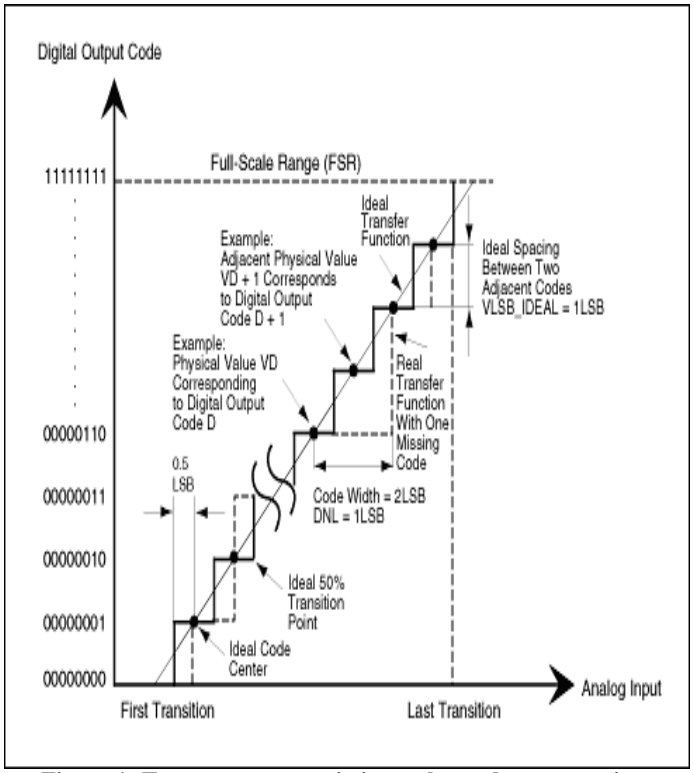

Figure 1: To guarantee no missing codes and a monotonic transfer function, an ADC's DNL must be less than 1LSB.

2. SOURCES OF STATIC ERROR

Static errors, that is those errors that affect the accuracy of the converter when it is converting static (dc) signals, can be completely described by just four terms. These are offset error, gain error, integral nonlinearity and differential nonlinearity.

Each can be expressed in LSB units or sometimes as a percentage of the FSR.

3. OFFSET ERROR

The offset error as shown in Figure 3 is defined as the difference between the nominal and actual offset points. For an ADC, the offset point is the midstep value when the digital output is zero, and for a DAC it is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by a trimming process. If trimming is not possible, this error is referred to as the zero-scale error.

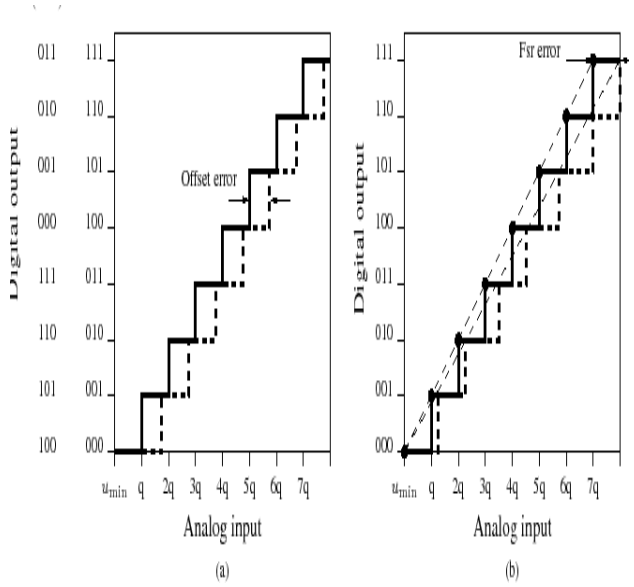

Figure 2: Gain Error

The gain error shown in Figure 2 is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the midstep value when the digital output is full scale, and for a DAC it is the step value when the digital input is full scale. This error represents a difference in the slope of the actual and ideal transfer functions and as such corresponds to the same percentage error in each step. This error can also usually be adjusted to zero by trimming.

The differential nonlinearity error shown in Figure 3 (sometimes seen as simply differential linearity) is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB. Therefore if the step width or height is exactly 1 LSB, then the differential nonlinearity error is zero. If the DNL exceeds 1 LSB, there is a possibility that the converter can become non monotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC there is also a possibility that there can be missing codes i.e., one or more of the possible 2n binary codes are never output. 0

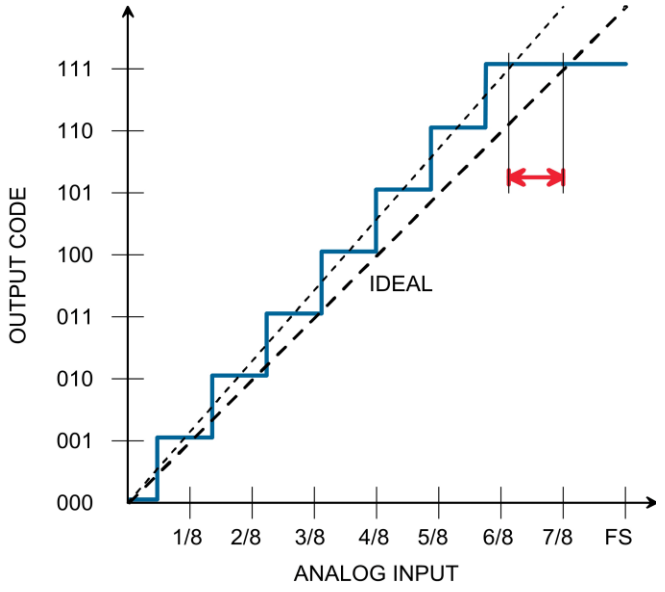

Figure 3: Differential Nonlinearity (DNL) Error

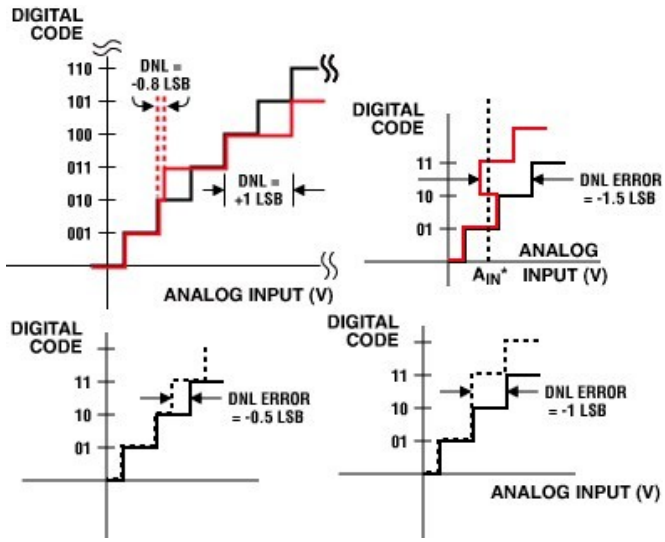

Figure 4: Integral Nonlinearity (INL) Error

The integral nonlinearity error shown in Figure 4 (sometimes seen as simply linearity error) is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a best straight line which is drawn so as to minimize these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. The second method is called end-point linearity and is the usual definition adopted since it can be verified more directly. For an ADC the deviations are measured at the transitions from one step to the next, and for the DAC they are measured at each step. The name integral nonlinearity derives from the fact that the summation of the

differential nonlinearities from the bottom up to a particular step, determines the value of the integral nonlinearity at that step.

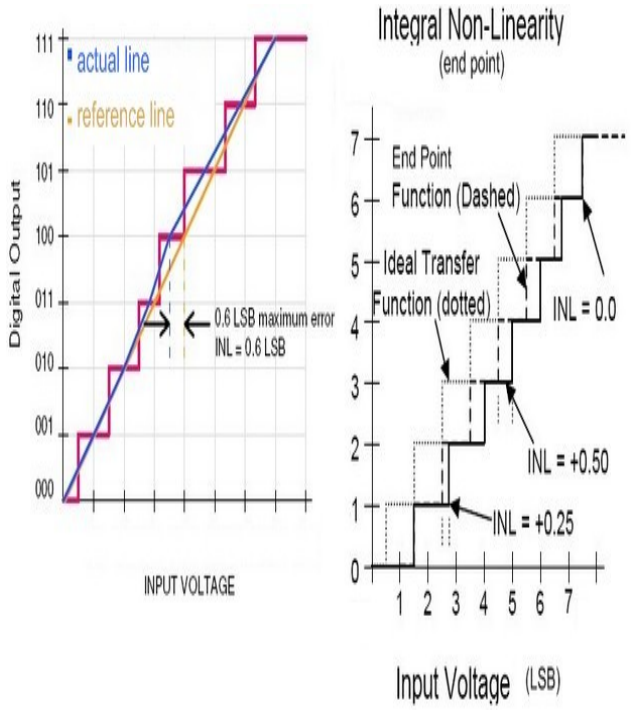

Figure 5

4. BACKGROUND

ADC testing can be categorized into dynamic testing and static testing. The dynamic testing measure these parameter such as signal to noise ratio, harmonic distortion, intermodulation distortion. The static testing includes these parameter such as integral non linearity(INL), differentia non linearity(DNL), gain error and offset error. Previous methods for testing Flash ADC's are almost universally based on generating a precise, analog signal on-chip as a testing input for the ADC. The signal is often a ramp or sinusoid, and many publications have been devoted just to designing highly reliable signal generators. The output of the ADC with the test signal applied can then be analyzed with histogram methods or by FFT analysis. Histogram method is commonly used in static testing and FFT analysis is commonly used in dynamic testing.

5. PROPOSED HISTOGRAM-BIST TEST METHOD

The Histogram method is also known as code density method. It is a one of the most popular techniques in the industrial context for ADC testing. Given an analog input signal, the histogram shows how many times each different digital code word appears on the ADC outputs. In the Histogram Test of ADCs, a sinusoidal stimulus signal with amplitude A, offset C and phase at the origin ϕ, is applied to the input:

$$V(t) = C - A.\cos(2\pi f.t + \phi)\ldots(1)$$

This signal is sampled by the ADC at a rate fs and M samples are acquired. The sample instants are given by

$$t_j = \frac{j}{f_s},\ j= 0,1,\ldots..M\text{-}1\ldots\ldots(2)$$

The digital output codes are used to compute the cumulative histogram, ck, which is the number of samples that have an output equal to or less than k. This histogram is then used to compute the estimated value of the transition voltages:

$$T_k = C - A\cos\left\{\frac{c_{(k-1)}}{M}\pi\right\},\ k = 1,..2^{n_b} - 1 \qquad (3)$$

in which n_b is the number of bits of the ADC.

The definition of transition voltage T_k, is the value of DC voltage that when applied to the ADC input leads to half the samples having an output code of k-1 or less. From the estimation of the transition voltages it is possible to obtain other parameters of interest like the code bin widths defined as

$$\hat{W} = \hat{T}_{k+1} - \hat{T}_k,\ k=1, 2, \ldots..2^{n_b}\text{-}2$$

The analog test signal is applied to ADC's input, the ADC generates digital code corresponding to the input signal. Only with digital code, the error detector decides whether the ADC has any fault or not.

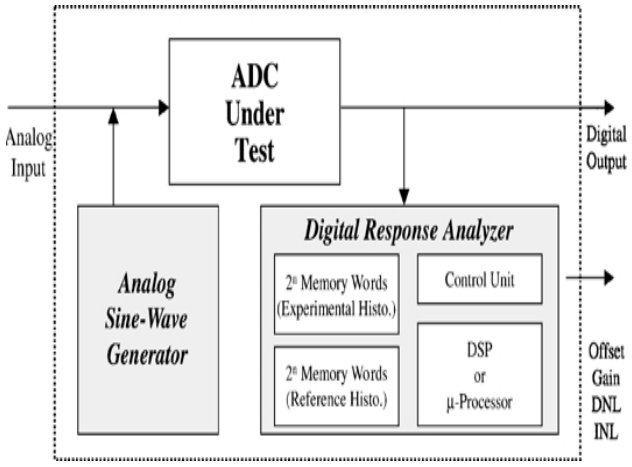

Figure 6

The basic effect of offset in A/D converters is frequently described as a uniform lateral displacement of the transfer function, while a deviation from ideal gain corresponds to a difference in the transfer function's slope after offset

compensation. With regard to performance verification and test, offset and gain can be defined as two parameters, VOS and G, in a straight line fit for the real code transition levels, as given on the left hand side in equation (4) [3, 4]. The values for offset and gain can be determined through an optimization procedure aiming at minimum matching error ε(k) between gain and offset adjusted real transition levels and the ideal values (right side of equation (4))

$$G\times T[k]+ V_{os}+\epsilon[k]= Q\times(K-1) +T[1] \text{ for } 1<K< 2^N - 1$$

where G is the gain, VOS the offset, Q the ideal code bin width, T[1]ideal the ideal first transition level, and T[k] the real transition level between codes k and k-1. The value for VOS corresponds to the analogue equivalent of the offset effect observed at the output.

Differential nonlinearity (DNL) is a measure of the deviation of the gain and offset corrected real code widths from the ideal value. DNL values are given in LSBs for the codes 1 to (2N-2) as a function of k as:

$$DNL[k](LSB) = \frac{W[k]-Q}{Q}, \text{ for } k= 1,2,..2^N - 2$$

where W[k] is the width of code k determined from the gain and offset corrected code transition levels and Q the ideal code bin width.

The INL/gain error is de_ned by the di_erence between the ADC's output and the ideal output that is obtained by counting the clocks in the ramp signal generator. The INL/gain error can be caused either by the nonlinearity or by the gain error of the ADC under test.

6. TEST EFFICIENCY DEFINITION

The test efficiency corresponds to the ability of the different test flows to detect faulty devices. Actually, as the classical FFT-based test procedure detects by definition all the faulty devices with respect to dynamic specifications, the test efficiency represents the aptitude of the considered test flow to detect faulty devices in terms of static specifications that would be detected by a histogram-based procedure.

In a population of ADCs to be tested, each instance is either fault-free (FFS) or faulty (FtS) versus given static specifications, and either fault-free (FFD) or faulty (FtD) versus considered dynamic specifications. Considering the correlations between static and dynamic parameters, we expect that several components which are faulty in terms of static specifications are also faulty versus dynamic requirements and will be rejected by a spectral analysis. The efficiency of the dynamic test procedure is thus defined as follows:

$$\xi = \frac{n\ (Ft_S \cap FT_D)}{nFt_S}$$

where (n FtS ∩FtD)represents the number of faulty instances according to static specifications whose measured dynamic parameters are also beyond dynamic specifications, and FtS n is the total number of faulty instances in the population with respect to static specifications.

7. CONCLUSION

The histogram test method for ADC is usually invoked in the context of external testing because of the large amount of hardware resources required for its implementation; two large RAMs and DSP capabilities. The calculation of the ADC parameters, which usually requires complex operations. It has been demonstrated that good estimates of offset, gain, DNL and INL can been obtained using operations as simple as addition, subtraction and division.

REFERENCE

1. Relative Techniques with Histogram Technique for Estimation of Different Testing Strategy of ADC Dr. R. S. Gamad, Manish jain oct. 2013
2. Estimation of Error in Nonlinearity in ADC using Standard Histogram Technique. R.S. gamad and D.K.Mishra 2008
3. ADC Integral Non-Linearity Testing with Low Linearity Monotonic Signals Bharath K Vasan, Degang J Chen, Randall L Geiger ieee2011
4. INL/DNL Measurements for High-Speed Analog-to-Digital Converters (ADCs) by maxim integrated 2001
5. Novel Threshold-Based Standard-Cell Flash ADC Marcel Siadjine Njinowa1, Hung Tien Bui1, François-Raymond Boyer 2012

