An Adiabatic 8T SRAM

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Abstract— A review on different adiabatic approach for the 8t SRAM cell is presents in this paper. In this paper, 8T SRAM cell to perform the write and read operations which employs a single bit line scheme. An SRAM is considering in the most development stage today, with its different variations as well as to support low power application. Stability factor and Leakage power is becoming the most important factor on SRAM (Static Random Access Memory) cells. A novel 8T SRAM cell design is considering reducing the leakage and also reducing the stability issues as compare to 6T SRAM cell. Now by including adiabatic circuit into 8T SRAM cell is become a new promising approach on consumption of power. The different adiabatic SRAM circuits proposed in the resent years are outlined in this paper.

Index Terms— SRAM, Adiabatic technique, Power Dissipation, Energy Recovery, Bit line.

I. INTRODUCTION

With the recent trend toward portable communication devices and computing system the devices demand for more power to operate smoothly. Therefore there is a concern factor for reducing the power dissipation in the design of any digital system. [3]. in the technology, the power consumption of the memory circuits is growing rapidly. Designing that memory cell with good data read and write stability and can consume lower power while performing any operation.

In Earlier time mostly landlines are used but now a day's portable devices such as hand held mobile devices are used and personal digital assistants like laptop, tablets, i-phone etc are gaining attraction and become more popular and as well as making changes in every aspect of our daily lives. The multimedia data processing, which includes the image/video applications, is the major reason for enhancing the demand for portable device market. A large amount of memory access require on the most of applications, which results in power consumption and thus limits the battery life time.

In this paper, discussions are about the new technique known as adiabatic technique for reducing the power in the SRAM cell. Section 2 discuss about the SRAM architecture and it working in different topology. Section 3 explains about the functioning of adiabatic technique.

II. SRAM BASICS

SRAM stands for static random access memory it is a volatile memory and can hold data as long as power is applied. There are three different modes that is reading mode, writing mode and hold mode of operation are operates on the SRAM cell. In the SRAM cell data is kept as long as power is turned on because of the latch and by using latch there is not any refresh operation is not required. This means 100% of the time reading and writing are going to perform. There are various topology of SRAM are available which is depending upon the number of transistor used.

The most widely used configurations in SRAM architecture is six transistors SRAM cell. The circuit consist of two cross coupled inverter connected back to back, the inverter are made up of one PMOS and one NMOS transistor in 6T SRAM cell and there is two more NMOS transistors are added in this 6T SRAM cell.

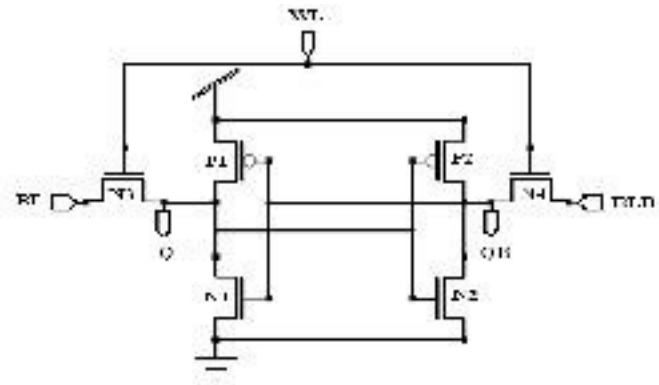


Figure1. Conventional 6T SRAM Cell

In this control signal is denoted by WL i.e. word line which control whether the bit line is to connect with the SRAM cell or not. The data for both read and write operation is transfer through BL and BLB. It is not necessary to have two bit lines, both the signal are complementary to each other and it improves noise margin. Hold mode is performing when the word line is low. Then the SRAM is in hold mode and it will hold the data into the latch.

But in the 8T SRAM cell writing is same as 6T SRAM cell and for the reading operation two more transistors are performed the read operation. This will improve the read

Stability. In 6T SRAM cell there is a problem of read stability which can be solve in this 8T SRAM cell.

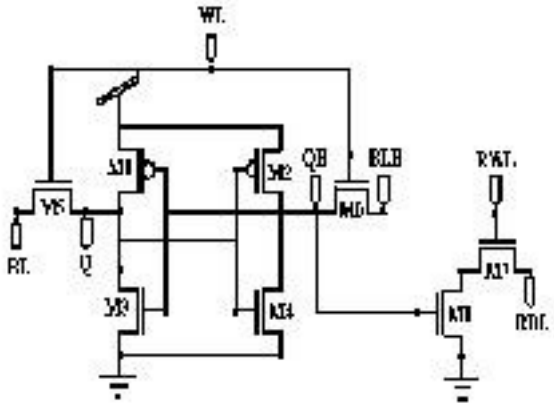


Figure2. Existing 8T SRAM Cell

2.1 Write operation of 8T SRAM

For the write operation, in order to store logic '1' to the cell, BL is charged to Vdd and BLB is charged to ground and for writing logic '0' BL is charged to ground and BLB is charged to Vdd. Then the NMOS access transistors are turn ON by switching the word line to Vdd. When the access transistors are turned ON, the values of the bit lines are written into Node Q and Node QB. The node which storing the logic '1' will not go to full Vdd because of voltage drops across the NMOS access transistor.

2.2 Read operation of 8T SRAM

For the read operation, the RBL is charged to VDD. When the cell enters into the read mode, the RWL turns high and the WL signal turns low. The storage data is transferred to the bit line through M7 and M8. The dedicated read port temporarily decouples the read path from the storage nodes, enabling a nondestructive read operation since M5 is turned off.[7] Considering the logic 1 and 0 then operation of original Q stores '0' and QB Stores '1' and channel of the read connected to the ground. M8 has a path to the ground, so the value '0' store in Q will be transmitted to M8 Then let us assume the Q stores "1", then the QB stores "0", when the read word line is chosen, there is no path from GND to M8

Then if Q stores"1", how can it be read out? [6]. Then into this operation external circuit is provided.

2.3 Hold operation of 8T SRAM

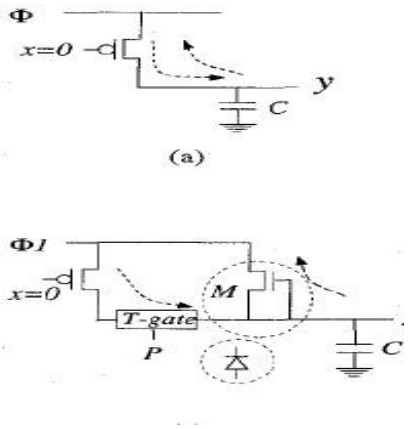
For hold operation, the word line is connected to ground. The access transistors NMOS_3 and NMOS_4 disconnect the cell from the bit lines. The two cross-coupled inverters formed by PMOS_1, PMOS_2, NMOS_1, NMOS_2 will continue to reinforce each other as long as they are connected to the Supply and NMOS_7 and NMOS_8 are waiting for some time.

III. ADIABATIC LOGIC

An adiabatic process is a process that occurs without the transfer of heat or matter between a system and its surroundings [3]. Adiabatic is a word derived from Greek letter "impassable" which is widely used in thermodynamic principle that is state change with no loss and gain of heat.

The adiabatic principle can be best explained with Fig. 3

Figure3. Basic recovery processes.



In adiabatic circuit designs presented in every switching operation is enforced to be nearly non dissipative. However, inverse logic functions are required to perform the energy recovery. Thus energy E taken out from the supply is given by CV^2dd for complete cycle. But out of this total energy half is only stored in the C and other half is dissipated. To charge a node with associated capacitance *C* from 0. In this, Fig3 it is clearly show that energy is dissipated through the circuit.

To recover the energy a gate is placed and denoted by M so energy is recovered into this circuit. Instead of gate a diode is placed so energy can be reused and not dissipated. Conservation of energy is known as adiabatic logic.

In Fig.4 RC circuit is shown it is used on switching circuit. This circuit depends upon the on and off operation.

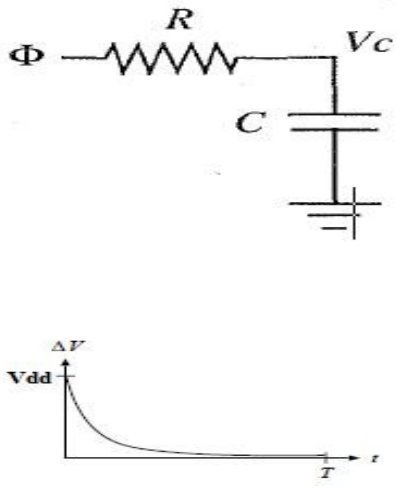


Fig 4: Charging an RC tree with a switch

The overall energy dissipated in the transition has been reduced to being proportional to

$$E = \frac{RC}{T} CV^2dd$$

Where, R is the effective resistance of the driver device, T is the time over which the switching occurs, C is the capacitance to be switched and Vdd is the voltage.

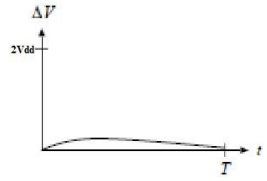


Fig. 5: Adiabatic charging of an RC tree

Hence by increasing the time constant T the energy can also be reduced.

IV. PREVIOUS WORK ON ADIABATIC LOGIC

Initially principle of adiabatic switching is explained by Yibin Ye and Kaushik Roy in [9] for logic gates. There are many techniques are used for energy conservations. In this paper, Authors consider the circuit level technique for the low energy computation by using reversible and partially reversible logic. Author completely explained the basic concept of adiabatic principle in which power clock is used. Power clock is used in adiabatic instead of pulse clock. In this paper many inverse logic gates are used there is a reason of using this gates. The controlling signal for the discharging path can be show output by an inverse logic gate because the every logic function in the circuit is reversible. Many common logic primitives, like NAND, NOR, and XOR are irreversible so this can be used into this reversible logic circuit. Authors present a design in Fig. 6, which is not based on reversible logic primitives. The circuit recovers most of the energy involved in the operations. The advantage of this design is simple for use and practicality used for implementation. Their design is essentially based on the, where the recovery path is controlled by a local signal so it is called as self-control scheme The design achieves lowest possible dissipation without requiring inverse logic functions.

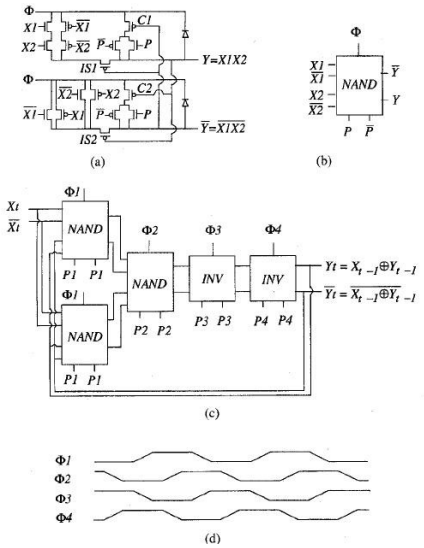


Fig.6: Circuit for NAND/AND using adiabatic block

A basic logic gate (NAND/AND) is shown in Fig. 6(a). It uses differential signaling: both input signals and their complements are required and an output signal and its complement are generated. The circuit consists of two branches. In each cycle, one branch is charging and the other is not. Thus, the constant load capacitance condition is satisfied without loss of energy. Authors conclude that the logic gates can recover about 90% of the total energy as that in conventional gates at 1MHz frequency.

Another SRAM technique, a constant load energy recovery SRAM design [5] provides a constant capacitive load to the power clock, regardless of memory operation or data access pattern. The memory architecture for constant load is shown in fig. 7 with dummy bit line. Moreover non selective precharge is used to ensure a constant memory load during the write operation. A dummy bit line of equal capacitance will connect to the power clock when the bit line is disconnected from the power clock during non-write cycle. It shows about 37% of energy saving as compared to conventional SRAM in 400 MHz frequency and 2.5V supply.

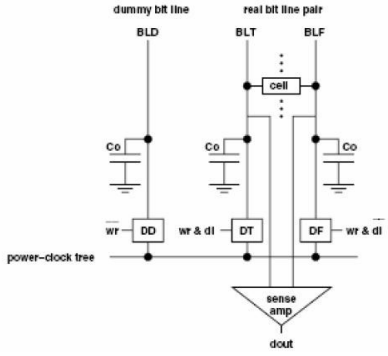


Fig. 7: Constant load memory with dummy bit line and energy recovery driver

Another adiabatic 1 Kb SRAM was designed by [8] in which maintaining a large VDD when gradual charging during writing and reading operation so that the problem of variation in threshold voltage is overcome. Fig. 8 shows the circuit of adiabatic SRAM cell in 6T topology. Here the cell is connected with a simple circuit, an extra NMOS and PMOS transistor only. The PMOS transistor is connected between the power line and MCPL and the NMOS transistor is connected between GND and MCPL. In this circuit, recycling of the charges is not considered but operation in the memory cell circuit is adiabatic and quasi static so that the problems of electro migration are solved. The circuit is simulated in 180nm technology and VDD is 1.8 V. At 100 MHz operating frequency the power reduction is about 42% as compared to its counterpart.

This circuit can be used on 8T SRAM operation also. By this circuit diagram, it is easy to know what is happening into this paper.

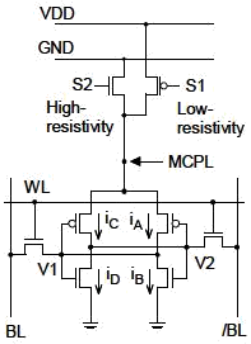


Fig. 8: Adiabatic SRAM cell with two extra transistors.

Another ultralow power 8T SRAM cell is designed by [4] uses a proposed 8T SRAM cell and compare it with adiabatic circuit and non-adiabatic circuit for the average power dissipation is reduced. Fig. 9 shows the proposed 8T SRAM cell in which adiabatic operation is performed. The average Power of the designs can be verify 65nm and 45nm Processes. Power reduction can be considered at 90-91% as compared to the conventional 8T SRAM cell.

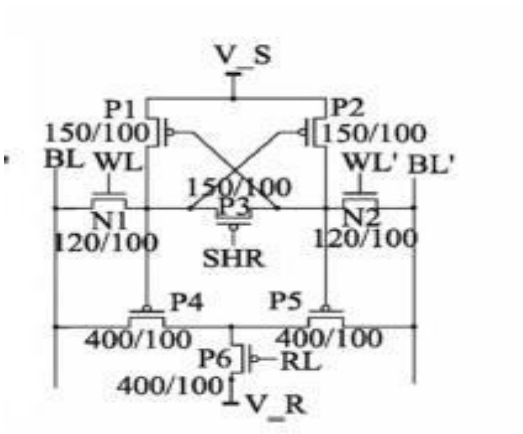


Fig. 9: 8T Proposed SRAM cell

V. CONCLUSIONS

The work on adiabatic memory and its power reduction capability is listed out in this paper. It shows that the different SRAM architecture proposed techniques, there voltage supply, operating frequency, process technology and there percentage power reduction.

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