Parallel Algorithms and VLSI Structures for Median Filtering of Images in Real Time

Ivan Tsmots, Dmytro Peleshko, Ivan Izonin

Abstract— **The most tasks of the digital image processing require the implementation of the median filter in real-time, providing the constraints in terms of the size and power consumption. The parallel algorithms and structures for the realization of the median filter, which focused on VLSI technology, are discussed in this article. The authors formulated the requirements for the median filter devices of images in real time, where one of the ways to ensure them is the hardware implementation of the median filter with the extensive use of the dimensional and temporal parallelization and consideration of recent advances in VLSI technology. Moreover, the parallel algorithms of the median filter for VLSI implementations are analyzed and developed. Also, the median filter device, based on these algorithms, is developed and patented, where the introduction of new elements and relationships among them provides the performance increase in comparison with the similar devices. The structures and analytical expressions for evaluating the major characteristics of the median filter devices (equipment costs, calculation time of the median, effectiveness) are built. The structure of conveyor device is the fastest and the most effective by the criteria of the equipment use among the considered structures of median filter devices.**

Index Terms— **bitwise comparison method, insertion sort method, median filter device, parallel algorithms, VLSI structures.**

I. INTRODUCTION

The methods and tools for digital signal and image processing are widely used in various fields such as control theory, medicine, various artificial intelligence systems and communications facilities, other. Due to the rapid development of technical means to competitiveness require fast and efficient analysis of signals and images, their transmission, there is a significant increase of the requirements for the processing of digital images.

Complications of mathematical tools for image analysis makes it necessary to improve existing and develop new methods and high-speed processing devices that will be meet the criteria (hardware complexity, speed, etc.) required by the applied field of application .

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The selection useful information from images which distorted in different ways is the primary task whose solution is increasingly used complex nonlinear filtering techniques, including median filter.

The purpose of article is to develop algorithms and VLSI structures for median filter to improve the ratio of performance / hardware costs for technical devices of signal and image processing for the systems of artificial intelligence.

II. MEDIAN FILTERING ON THE BASIS OF THE INSERTION SORT METHOD

The structure of the median filter device in real time depends by the frequency of receipt numbers and the number of input channels. The conveyer device with parallel or sequential implementation of algorithms is widely used for quick median filtering. Median calculation on the basis of completely parallel devices is redundant. Reduce redundancy can by use of streaming-conveyor devices with consistent implementation of algorithms. In these devices, calculate of the median is reduced to the execution pairwise sequence comparison and permutation of numbers. Analysis methods of sorting shows that the most appropriate method for streaming-conveyor implementation of median filtering is insert sort method, feature of which is small time of result formation [2]. Based on this method, we developed a modified algorithm of median filtering, which is oriented on VLSI implementation [3]. This algorithm is implemented based on simultaneous execution of N identical basic operations. Based on the hardware implementation, the basic operation is realized by the one processor element (PE). The basic operation of algorithm of the median filtering is carried out in two stages. In the first step compares the number of B_j and the number of his supplement A_j, that is stored in PEj (j = 1, 2, ..., N), with the new number of B_H and number of his supplement A_H and the results of this comparison are formed by the formulas:

$$PB_j = \begin{cases} 0, \text{ when } B_H < B_j \\ 1, \text{ when } B_H \geq B_j \end{cases} \quad (1)$$

$$PY_j = \begin{cases} 0, \text{when } A_{H'} \neq A_j \\ 1, \text{when } A_{H'} = A_j \end{cases} \phi \quad (2)$$

where PBj i PYj - information on the outputs of the comparison scheme (comparator), respectively, numbers and digits of supplement. In the second stage, by the results for each comparison PEj determined the number B_j* and the number of his supplement A_j*, which will be stored there. Definitions for each PEj number B_j* and his numbers

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supplement A_j* when the number of devices will be pre-sorting, so that the maximum is stored in PE_1, and the minimum - in PE_N, occurs by the formulas:

$$B_j^x = \begin{cases} B_H, \text{ when } y_j \wedge \overline{PB_j} \wedge PB_j \vee \overline{PB_{j-1}} \wedge PB_{j-1} \wedge PB_j \wedge y_{j-1}=1 \\ B_{j-1}, \text{ when } PB_{j-1} \wedge \overline{y_{j-1}} = 1 \\ B_{j+1}, \text{ when } y_{j-1} \wedge \overline{PB_{j+1}} \vee PB_{j+1} \wedge PY_j = 1 \\ B_j, \text{ when } \overline{PB_j} \wedge \overline{PY_j} \wedge y_{j-1} \vee PB_j \wedge y_{j-1} = 1 \end{cases} \quad (3)$$

$$A_j^x = \begin{cases} A_H, \text{ when } y_j \wedge \overline{PB_j} \wedge PB_j \vee \overline{PB_{j-1}} \wedge PB_{j-1} \wedge PB_j \wedge y_{j-1}=1 \\ A_{j-1}, \text{ when } PB_{j-1} \wedge \overline{y_{j-1}} = 1 \\ A_{j+1}, \text{ when } y_{j-1} \wedge \overline{PB_{j+1}} \vee PB_{j+1} \wedge PY_j = 1 \\ A_j, \text{ when } \overline{PB_j} \wedge \overline{PY_j} \wedge y_{j-1} \vee PB_j \wedge y_{j-1} = 1 \end{cases} \quad (4)$$

where -$Yj=PY_0 \vee PY_1 \vee PY_2 \vee \ldots \vee PY_{j-1}$, $PY_0=0$.

Scheme of the conveyor-streaming median filtering device, in which median is calculating based on the insertion sort method is shown in Fig. 1, where Pr - register; PE - processor elements; TI - input for tact impulses.

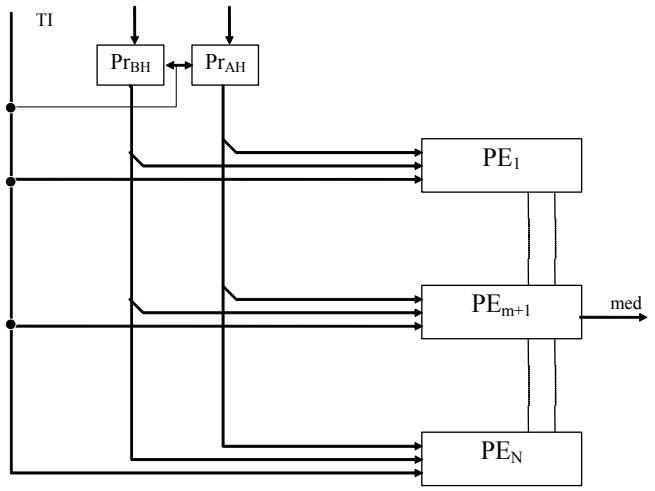

Figure 1. Algorithmic scheme of the one-dimensional median filtering device, which based on the insertion sort method

In each tact of work in registers Pr_{BH} and Pr_{AH} is recorded respectively new number B_H and the number of his supplement A_H.. Numbers B_H and A_H fed to the inputs of all PE. Scheme PEj shown in Figure 2, where KM - commutator; CS - comparison scheme; CCS - control commutator scheme. In each PEj using diagrams CS_{Bj} and CS_{Aj} performed comparing numbers B_j and A_j with numbers B_H and A_H, according to the formulas (1) and (2) and are formed their results. Result of compare from the output of the CS_B and CS_A processor elements PE_{j-1}, PE_j and PE_{j+1} one coming to the inputs of the control commutator scheme PEj, where control commutator signals KM_{Bj} and KM_{Aj} forming according to formulas (3) and (4) . Depending on this signal on the commutator output KM_{Bj} (KM_{Aj}) can come either B_H (A_H), or B_j (A_j), or B_{j-1} (A_{j-1}), or B_{j+1} (A_{j+1}).

The peculiarity of the considered structures is the ability to change size of the filtering "window" through serial connection required numbers of PE. At the same time, filtering does not depend on the size of the "window", but depends on the execution time of basic operations, which is:

$T_1=t_{Pr}+t_{CS}+t_{KM}+t_{CCS}$,

where t_{Pr}, t_{CS}, t_{KM}, t_{CCS}, - the response time respectively by the register, comparison scheme, commutator, and control commutator scheme.

The detailed scheme of the developed and patented median filter device can be seen in the next section.

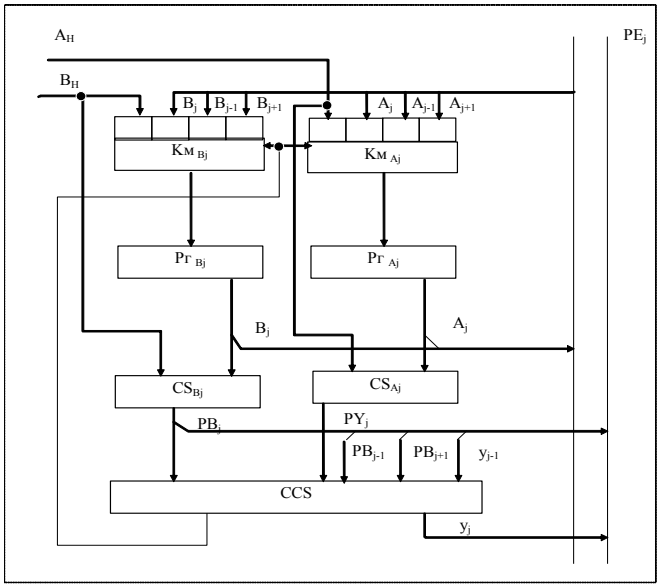

Figure 2. Scheme of the processor element of median filtering device, which based on the insertion sort method

The hardware cost of the median filter device based on the insertion sort method equals:

$$W_1 = N\left(2\left(W_{KM}+W_{Pr}+W_{CS}\right)+W_{CCS}+2W_{Pr}\right)+2W_{Pr},$$

where W_{KM}, W_{Pr}, W_{CS}, W_{CCS} - hardware costs for implementation of device respectively by the commutator, register, comparison scheme, and control commutator scheme.

III. MEDIAN FILTER DEVICE WITH FILTER WINDOW SIZE BASED ON THE INSERTION SORT METHOD

Based on the above method, median filter device in the filtering window size m was developed and received a patent for an invention [5]. Similar devices [6,7,8] have several disadvantages, which makes it necessary to develop new image processing techniques in real time. For example median filtering device [6] contains $2m+1$ registers where $(2m+1)$ - number of elements of sorting in a given filtering window, $1{,}5(m^2-m)$ comparison of nodes, each consisting of comparison scheme and two schemes "AND-OR". However, this device for its realization requires large hardware cost and has a low speed, which is determined by the time of work $(2m+1)$ comparison scheme and $(2m-1)$ elements "AND-OR"

Closest to the proposed device is the median filter device [7] containing m registers, where m - window size, m adders, $(m^2-m)\backslash 2+m-1$ nodes of comparison, decoder and

ISSN: 2278 – 1323

multiplexer. However, this device has a low speed execution median filtering which determined by the period of receipt of data, depending on the time of operation of the register, comparator, adder, decoder and multiplexer and is calculated as follows:

$$t_f = t_{Pz} + t_{CS} + t_{SYM} + t_D + t_M,$$

where t_f - filtration period, t_{Pz} - the time of recording in the register, t_{CS} - the operation time of comparison scheme, t_{SYM} - the operation time of adder, t_D - the operation time of decoder, t_M - the operation time of multiplexer.

In FIG.3 is a block diagram of the proposed median filter device in FIG. 4 shows the node comparison scheme, where: 1 - information input; 2 - input register; 3 - node of comparison; 4 - registers; 5 - comparison node ; 6 - out of median; 7 - commutator; 8 - comparison scheme.

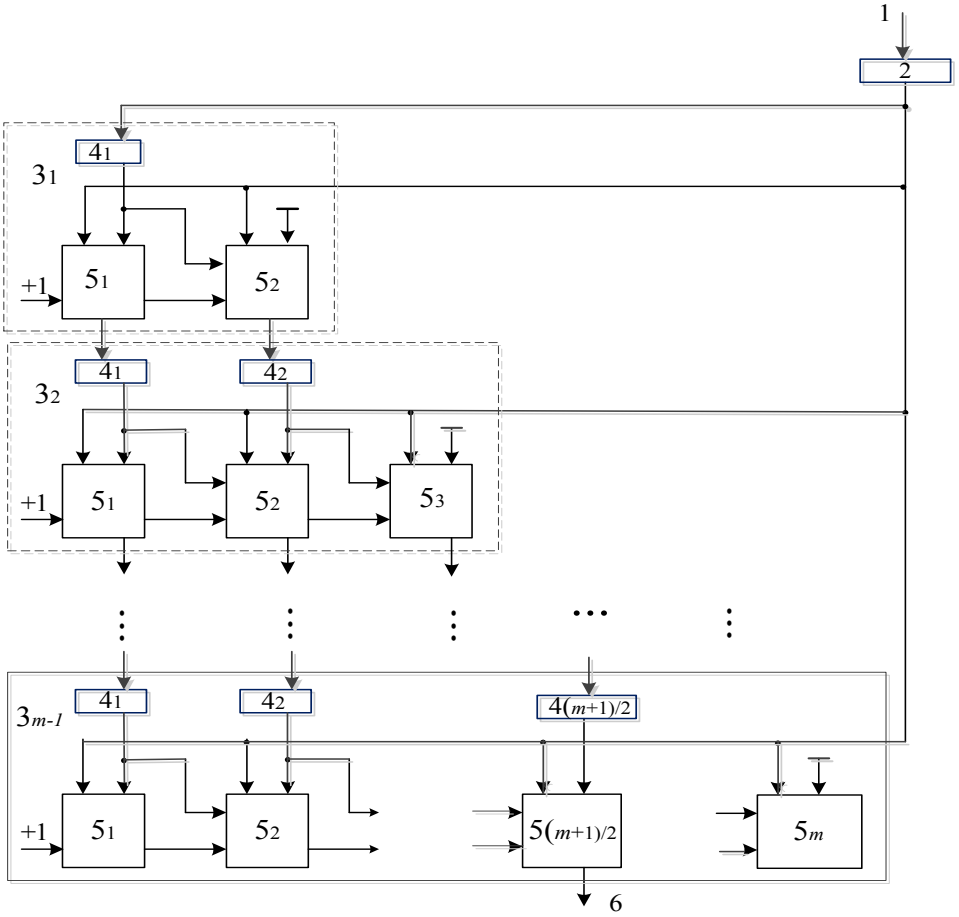

Figure 3. Scheme of the median filtering device with the filter window of size m

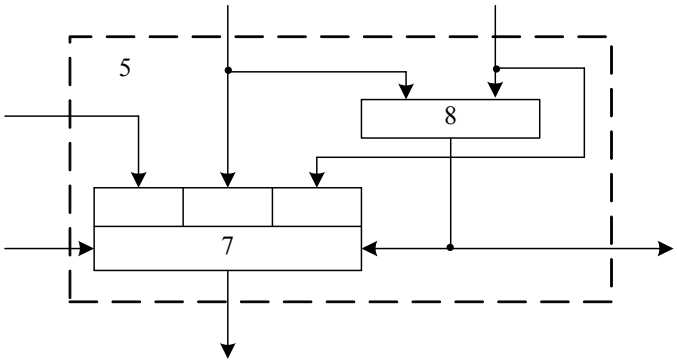

Figure 4. Scheme of node of comparison in proposed device

ISSN: 2278 – 1323

This device provides performance of median filtering with tact:

$$t = t_{Pz} + t_{CS} + t_{KM},$$

where t_{Pz} - t_{Pz} - the time of recording in the register, t_{CS} t_{CS} - the operation time of comparison scheme, t_{KM} - the operation time of commutator.

IV. MEDIAN FILTERING ON THE BASIS OF THE BITWISE COMPARISON METHOD

One of the median filtering algorithms on the basis of the bitwise comparison method is algorithm, where median is calculated sequentially bit from bit, begin from high bit. Calculation each bit of median, implements in two steps.

In the first step we calculate *i*-t*h* value, where *i=1,2,...n*, bit of median as:

$$y_i = \begin{cases} 1, when \sum_{j=1}^{N} x_j^i \geq m+1 \\ 0, when \sum_{j=1}^{N} x_j^i < m+1 \end{cases} \quad (5)$$

where x_j^i - *i-th* rank of the *j-th* number.

In the next step, depending on the value of y_i is done modification next bits as follows:

$$x_{jm}^k = x_j^k \left(\overline{y_i} \overline{x_j^i} \vee y_i x_j^i \right) \vee \overline{y_j} x_j^i \quad (6)$$

where *k=i+1, ..., n.*

The structure of device that implements this algorithm is shown in Fig. 5, where MI_A - many inputs adder; SMR - scheme of modification bits.

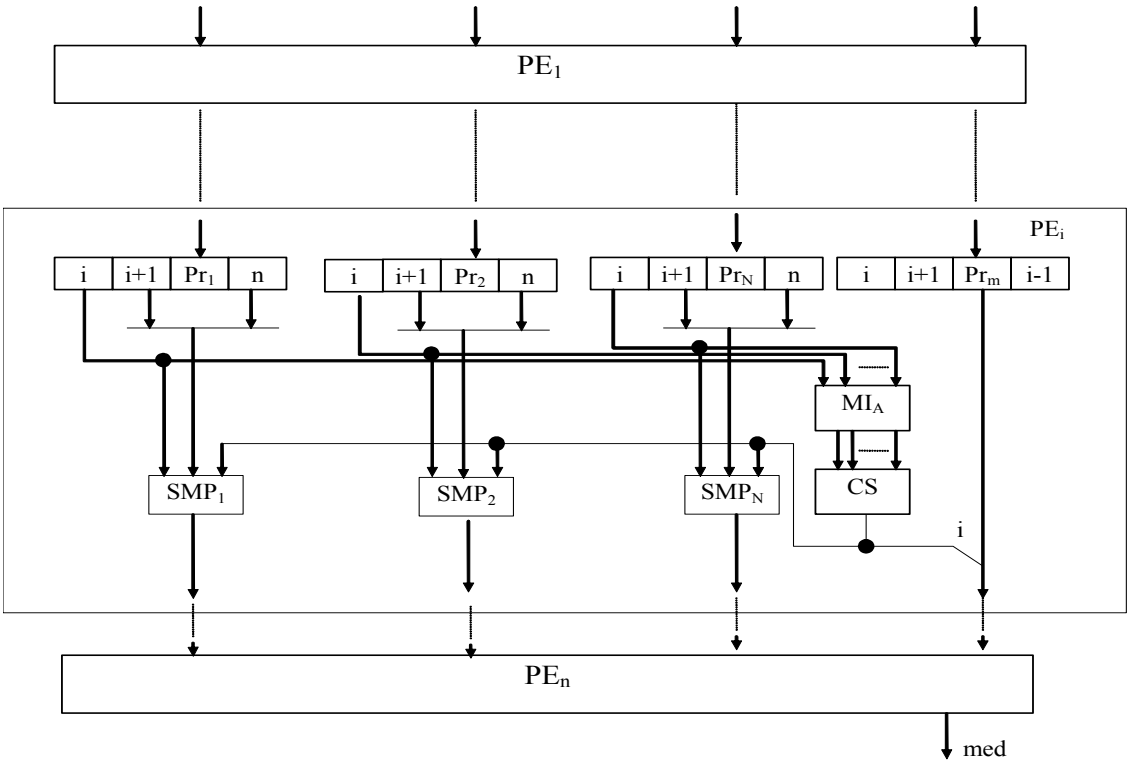

Figure 5. Structure of median filter with consistent calculation of median bits

The device consists of *n* identical PE, for each of them is calculated one bit of median y_i with the formula (5) and is modified next bit of numbers with the formula (6). Median value is obtained at the output PE*n* after passing through all the numbers of PE. The device works on the conveyor principle with tact, which is:

$$T_2 = t_{pz} + t_{BCM} + t_{CS} + t_{CMD},$$

where t_{BCM}, t_{CS}, t_{CMD} - the operation time according of one-bit N-inputs adder, of comparison scheme, and of scheme of modification bits. The hardware cost for implementing median filter is:

$$W_2 = n\left(N\left(W_{pr} + W_{CMD} \right) + W_{BCM} + W_{CS} + W_{Pr} \right),$$

where W_{BCM} *i* W_{CMD} - hardware implementation costs according for N-inputs adder, and for scheme of modifications of bits.

Another method of calculating median of the "window" size *N=2m+1* numbers are finding it as the number of A_{med},, for which *m* are integers greater than or equal A_{med}, and the same numbers less or equal to A_{med},. Calculate the median of this method is to perform similar operations *m+1*. Each operation involves determining the maximum number A_{pmax} in the "window", where *p=1,...,m+1*, and subsequent modification numbers in this "window." Calculate the maximum number of A_{pmax} performed by consecutive comparing the bits of all the numbers starting with the eldest.

For each comparison we obtain *i*-th bit of the maximum number, which calculation by the formula:

$$\overline{A_{p\max}^i} = \bigwedge_{j=1}^{N} \overline{x_j^i \wedge y_{jp}^i}, \quad y_{jp}^1 = 1, \quad (7)$$

where y_i^j - *j*-th bit of the *i*-th control element of *p*-th array.

Formation of the j-th bit *(i +1)-th* of control elements for *p*-th array is done as follows:

$$y_{(i+1)p}^j = (\overline{A}_{p\max} \vee x_j^i) \wedge y_{ip}^j. \quad (8)$$

ISSN: 2278 – 1323

After calculating maximum number, the array modification occurs, which is excluded this number from the further process calculations. This exception is made by inversion of the *j*-th bits of *n*-th control element:

$$y^{j}_{i(p+1)} = \overline{y^{j}_{np}}.$$

This filter (Fig. 6) is implemented at the *(m+1)* series-connected PE, each of which performs a calculation of the maximum number. A_{pmax}. PE is implemented on an array of identical cells *Nxn* comparison cell (CP) (Fig. 7).

Each column of cells $CP_{1i} - CP_{Ni}$ calculated according to the formula (7) the value of *i*-th bit maximum number of A^{i}_{pmax} and are formed according to formula (8) value *(i+1)*-th control element. CP is implemented on the basis of logic elements I, OR, I-No.

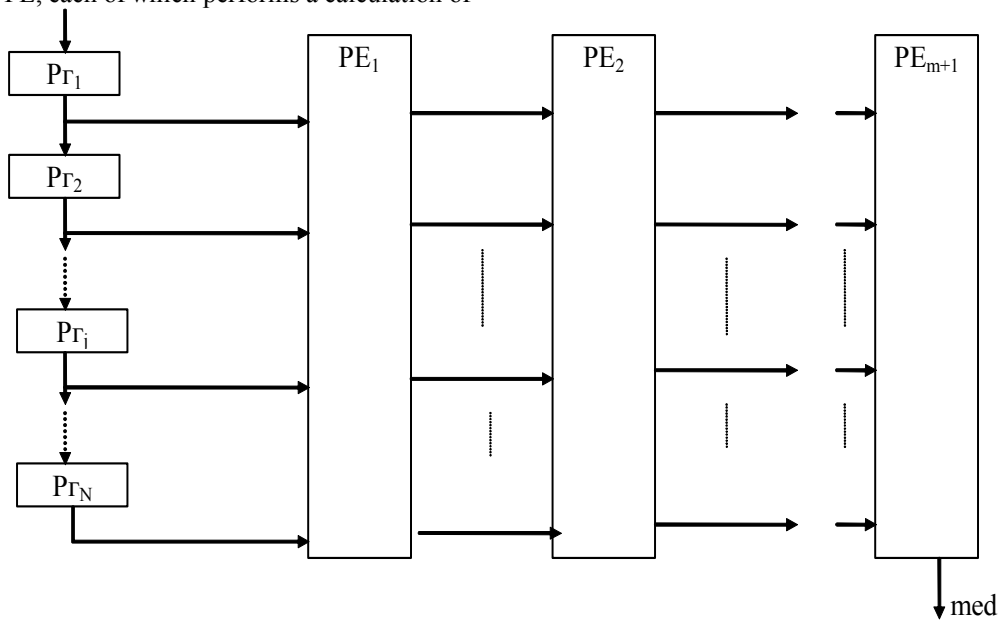

Figure 6. Scheme of median filter based on bitwise comparison

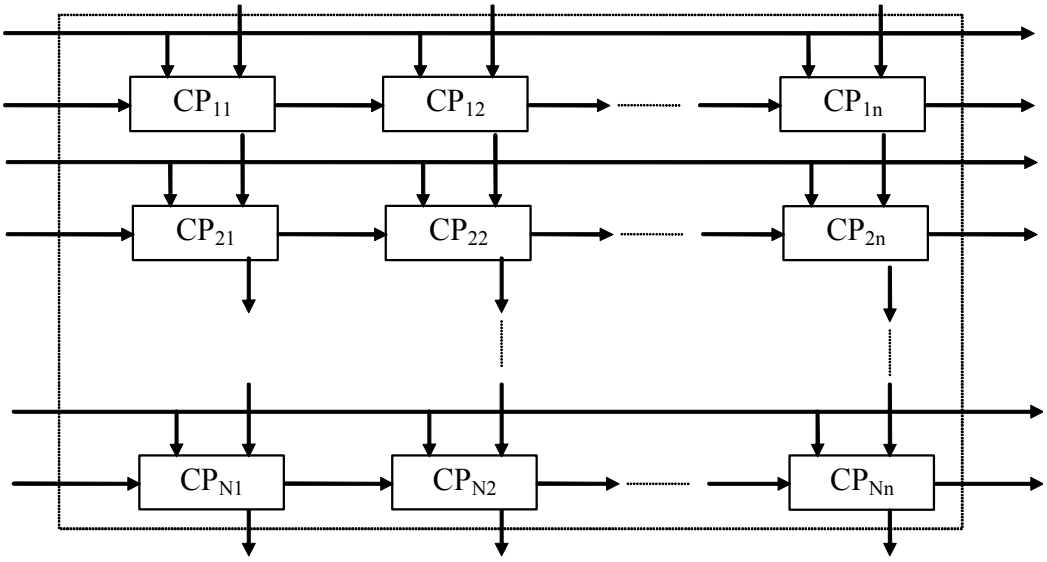

Figure 7. Scheme for PE of median filter based on bitwise comparison

Median filter can operate in asynchronous and synchronous modes. CP schemes for single-cycle and conveyor median filter devices are shown in Figure 8 a, b.

ISSN: 2278 – 1323

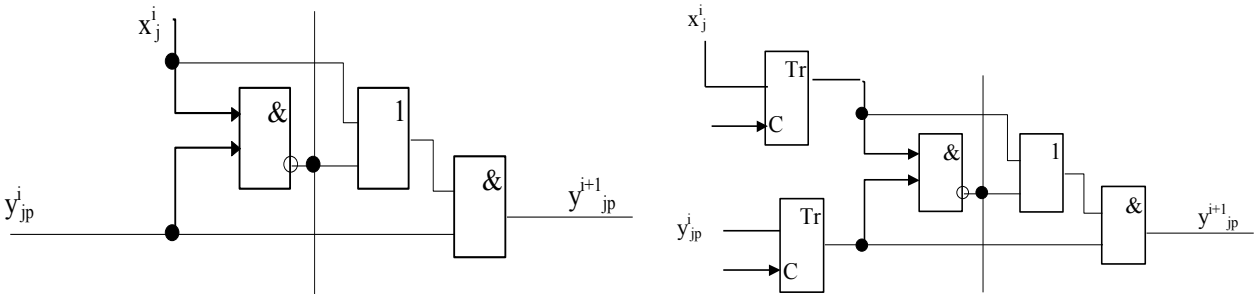

Figure 8. Cells comparison scheme: a) single-cycle unit; b) conveyor device

In asynchronous mode, median computation is done in one tact, equal to:

$$T_{30} = 3(m+1)nt_i,$$

where t_i - the operation time of logic element "I".

Hardware costs for single-tact's median filter is equal to:

$$W_{30} = 3(m+1)NnW_1,$$

where W_1 – hardware costs of the logical elements of type I, OR, I-NOT.

To ensure the operation of the median filter in the synchronous mode is required in each CP to include additional triggers (Fig. 8 B). In synchronous mode, median filter will operate on a conveyor principle with tact, equal:

$$T_{3k} = t_{Tr} + 3t_i,$$

where t_{Tr} - the operation time of trigger.

Hardware costs for such median filter are equal to:

$$W_{3k} = (m+1)Nn(W_{Tr} + 3W_1),$$

where W_{Tr} - hardware costs for the implementation of the trigger.

V. Evaluation for the Developed Structures of Median Filters.

The main components of the developed structures of median filter are registers, switches, comparator, and adder. The most appropriate is to implement developed structures in the form of VLSI. The unit of measurement for equipment it is advisable to logic gate, which is the element of next type: inverter, I, OR, and to assess temporal parameters - latency logic gate τ. To evaluate the performance of the developed structures of median filters used data on costs and latency of basic components that are listed in [4]. Based on these data for each of the structures we developed analytical expressions for calculating the cost of equipment and time calculation of median, which are listed in the *Table*, where n - digit numbers; $N = 2m + 1$ - the size of the "window".

For comparison of developed structures, introduced estimation of efficiency use of equipment, which defined as:

$$E = \frac{1}{WT},$$

where: W - equipment costs for median filter in valves logical gates; T - time for median calculation.

Table **Analytical expressions for evaluation of the main characteristics of the developed structures for median filter devices**

Type of structure	*The cost of equipment (logical gate)*	*The time of calculating the median (τ-gate)*	*Effectiveness*
Fig.1	$W_1=N(56n+20)+14n$	$T_1=(3log_2n+8)$	$E_1=1/(3log_2n+8)$ $[N(56n+20)+14n]$
Fig.3	$W_2=9Nn^2+10n^2+18N$	$T_2=(7log_2N+3log_2n+5)$	$E_2=1/(7log_2N+3log_2n+5)$ $[9Nn^2+10n^2+18N]$
Fig.6	$W_{3o}=1,5N^2n$ $W_{3k}=4N^2n$	$T_{3o}=1,5Nn$ $T_{3k}=6$	$E_{3o}=1/(1,5Nn)(1,5N^2n)$ $E_{3k}=1/24\ N^2n$

Graph of the dependence of the efficient use of equipment from the size of the "window" N for $n = 8$ are shown in Figure 9, where E1, E2 - effective use of equipment for the devices which are shown in Figure 1, Fig. 3; E3k, E30 - effective use of equipment for the device which shown in Fig. 6, respectively, for conveyor and single pulse modes.

The graph shows that the most effective use of the equipment by the structure conveyor device, such is shown in Figure 6.

ISSN: 2278 – 1323

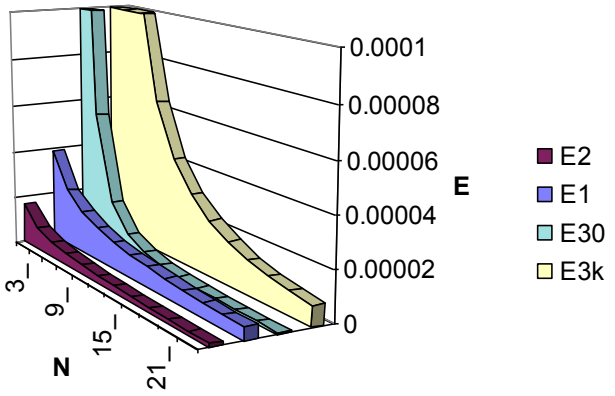

Figure 9. Graph of the effective use of equipment depending on the size of the window

VI. CONCLUSION

Modularity, regularity, locality ties and parallelism are the features of algorithms and VLSI structures for median filter, developed in the article.

The application of pipelining and parallel processing in the design of VLSI structures of median filter achieves high performance.

Developed and patented median filter device exceeds examined analogues in runtime of operations median filtering with window size *m*.

Among the considered structures and devices for median filter, fastest and most efficient use of the equipment is the conveyor structure of the device where median is determined by the method of the bitwise comparison as the number of A*med*, for which a "window" of size *N* is *N/2* numbers greater or equal A_{med} and the same number smaller, or equal to A_{med}.

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