

Design and Analysis of 5GHz Frequency, Low-Phase-Noise, Parasitic Compensated LC Voltage Controlled Oscillator

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Abstract—Firstly, in this design a cross coupled topology with switched biasing technique so that it can work in high frequency region.

Secondly, phase noise generated by the voltage controlled oscillator has been reduced by sizing the active devices, because the impact of physical parameter of device is large on the specification of any radio frequency integrated circuit.

The proposed methodology is verified through design in a standard 0.18 μm CMOS process supplied by Tanner’s EDA simulation software tool. Several designs of voltage control oscillator circuits have been implemented for a comparison and verify that the switched biasing does improve frequency and phase noise performance. These results are then compared

Simulation results have provided improvement from -114.3 dBc/Hz to -139.6 dBc/Hz at a 1 MHz offset frequency from the 5 GHz carrier when switched biasing. The relative increase in voltage control oscillator’s phase noise performance translates in higher modulation accuracy when used in a transceiver, therefore this increase can be regarded as significant. The power consumption of the simulated VCO is around 746mW

Keywords: CMOS, Cross-coupled, phase noise, Tanner EDA, VCO

I. Introduction

A PLL is a control system, where phase is the variable of interest. The block diagram of a PLL is shown in Fig. 1.1. The circuit is called a phase-locked loop because the feedback operation in the loop automatically adjusts the phase of the output signal F_{out} to follow the phase of the reference signal F_{ref} . The prescaler (Frequency Divider in Fig.) divides the VCO frequency (and phase) by a division modulus of N .

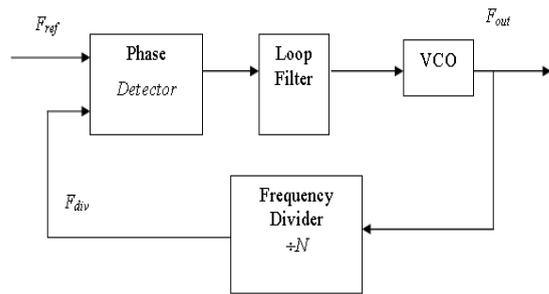


Fig 1. Phase Locked Loop

A. Voltage Controlled Oscillator

VCO is an electronic circuit designed to be controlled in oscillation frequency by a voltage input. The oscillator requires a tank circuit. A parallel resonance tank comprises of inductance (L) and capacitance (C). The principle operation of the VCO is by means of the controlled operation of the LC tank circuit. An oscillator can be described as a positive feedback system and it amplifies its own noise at a selected frequency ω_0 , as shown in Fig. 1.1.1.

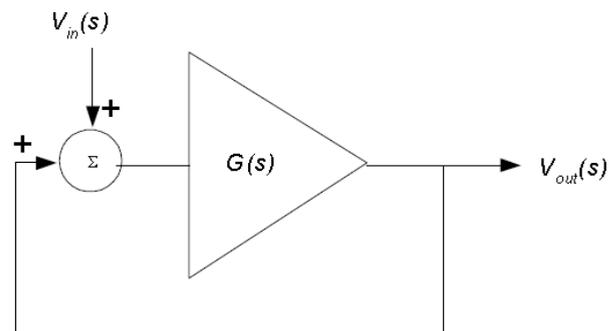


Fig. 1.1 Feedback diagram of an Oscillator

The transfer function of the oscillator is,

$$A_0 = \frac{V_{out}(s)}{V_{in}(s)} = \frac{G(s)}{1-G(s)} \quad 1.1$$

From equation (1.1), it can be concluded that the closed loop gain will approach infinity under the following

conditions: (1) the open loop gain is equal to unity, i.e. $G(S) = 1$, and (2) the total phase shift of the loop is equal to 0° , i.e. $\angle G(S) = 0^\circ$, which are called the Barkhausen's Criteria. In an environment with the existence of noise at all frequencies, the Barkhausen's Criteria is satisfied only with the noise at a specific frequency ω_0 . When the oscillation is properly started, the noise signal at frequency ω_0 is amplified and increased till the amplifying devices are saturated. Hence, the stable oscillation is maintained. In order to ensure the startup of the oscillation in presence of temperature and process variations, the small signal loop gain is typically chosen to be 2-3 times of the required value.

In most applications, it is required that the oscillator to be tunable, where the output frequency is a function of a control input. Thus, a VCO can be described by

$$\omega_{out} = \omega_{fr} + K_{vco} v_c \quad 1.2$$

Where, ω_{fr} is the free running frequency of the VCO, v_c is the control voltage of the VCO and K_{vco} is the gain of the VCO specified in rad/s/V. A voltage signal with magnitude of V_m can be described as

$$v_{out}(t) = v_m \cos(\theta(t)) \quad 1.3$$

Where, $\theta(t) = \int \omega_{out} dt + \theta_0$. Substituting equation (1.2) into equation (1.3), the sinusoidal voltage output signal of a VCO is given by,

$$v_{out}(t) = v_m \cos(\omega_{fr} t + K_{vco} \int v_c dt + \theta_0)$$

Where, K_{vco} is assumed to be linear.

B. Phase Noise

The noise produced by an oscillator is important in practice because it may severely damage the performance of communication receiver system. Phase noise refers to the short term random fluctuation in the frequency (or phase) of an oscillator signal.

$$\mathcal{L}\{f_m\} = 10 \log \left[\left[\left(\frac{f_0}{2Q_L f_m} \right)^2 + 1 \right] \times \frac{FkT_0}{P} \times \left(\frac{f_c}{f_m} + 1 \right) \right]$$

The equation describes the dependence of phase noise on the noise factor which ultimately depends on output noise spectral density generated by circuit.

II. Topology of VCO

The topology used for the proposed VCO is a cross coupled topology. Since the full exploitation of differential operation lowers undesirable common-mode effects such as extrinsic substrate and supply noise amplification and

upconversion. The rise and fall time symmetry is also incorporated to further reduce the $1/f$ noise up conversion.

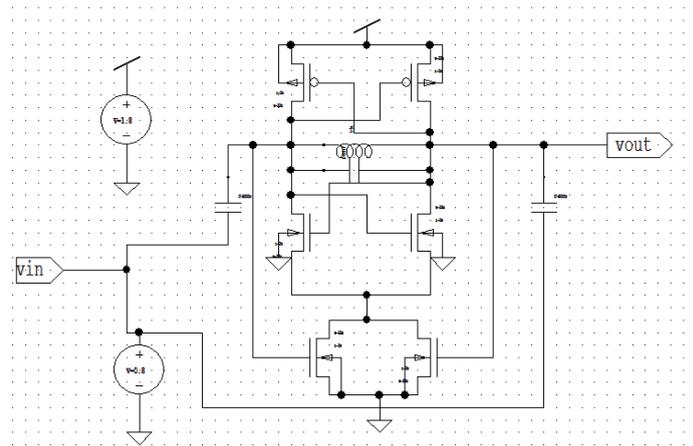


Fig. 2 cross coupled LC VCO

III. Result

A. Transient Analysis Result

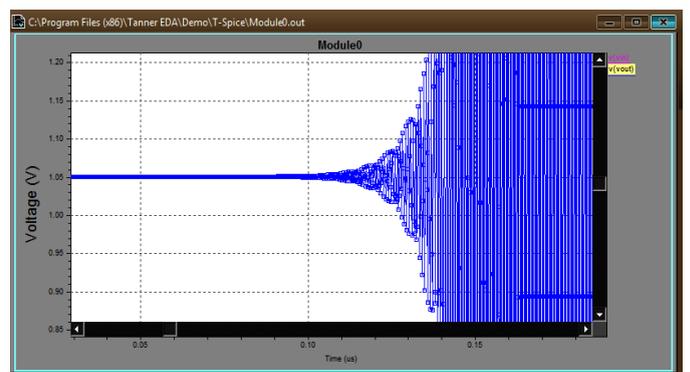


Fig 3.1 transient output of proposed LCVCO simulated through Tanner's EDA

B. Noise Analysis Result

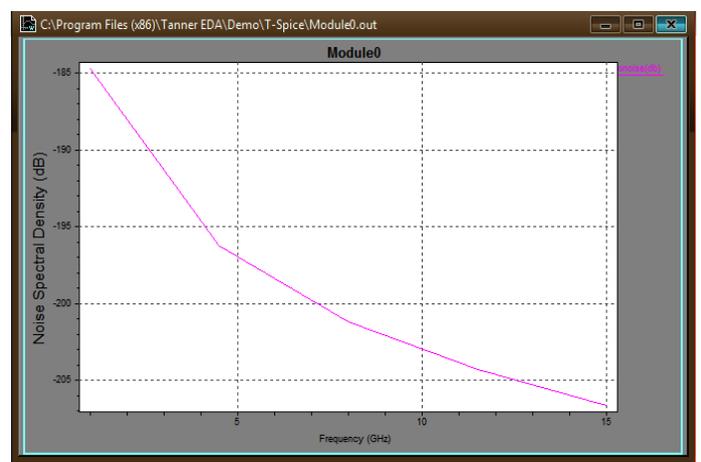


Fig 3.2 noise spectral density output of proposed LCVCO simulated through Tanner's EDA

C. phase noise Result

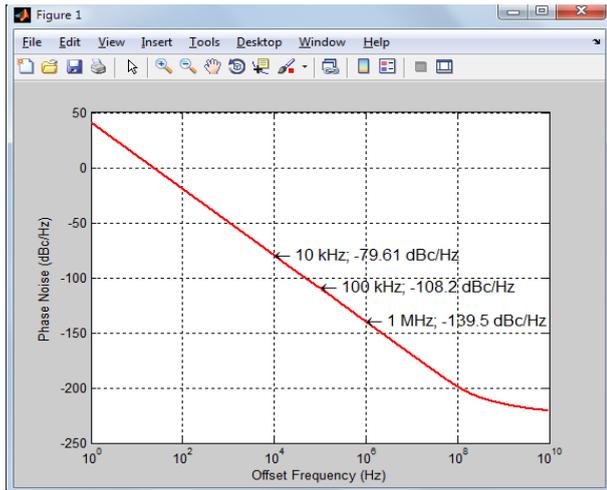


Fig 3.3 Phase noise computed through MATLAB

IV. conclusion

The LC VCO has been designed with $.18\mu\text{m}$ technology that shows a -139.5dBc/Hz of noise at offset frequency of 1MHz .

References

- [1] Seyed Reza Hadianamrei, MasoudSabaghi, MaziyarNiyakanLahiji, Mehdi Rahnama, " Noise Phase CMOS Quadrature VCO with Superharmonic Coupling Using Cross-Couple Pair Low", Circuits and Systems, 2011, 2, 281-285 doi:10.4236/cs.2011.24039, Scientific Research, October 2011.
- [2] Nisha Gupta "Voltage-Controlled Ring Oscillator for Low Phase Noise Application"International Journal of Computer Applications (0975 – 8887) Volume 14– No.5, January 2011.
- [3] Chunhua WANG, Guanchao PENG, Minglin MA, Zhan LI "A New Low-Power CMOS Quadrature VCO with Current Reused Structure" RadioEngineering, vol. 20, no. 1, April 2011
- [4] To Po WANG , Cheng-Yo Chiang "A Low-Power low phase noise wide tuning range k-band VCO in $0.18\mu\text{m}$ CMOS" IEICE Electronics Express, Vol.8, No.11, 780–787, 2011
- [5] Ge Yu " A study of two wideband CMOS LC-VCO structures" B.A.Sc., The University of British Columbia, 2009
- [6] Chih-Hsiang Chang and Ching-Yuan Yang "A $0.18\text{-}\mu\text{m}$ CMOS 16-GHz Varactorless LC-VCO with 1.2-GHz Tuning Range" IEEE Asian Solid-State Circuits Conference November 12-14, 2007
- [7] S. Gribaldo, R. Boudot, G. Cibiel, V. Giordano, O. Llopis "Phase noise modelling and optimization of microwave SiGe amplifiers for sapphire oscillators applications" 19th European Frequency and Time Forum, Besançon : France (2005)
- [8] Ali Hajimiri and T.H. Lee, "A general theory of phase noise in electrical oscillator," IEEE Solid-State Circuits, vol.33, pp. 179-194, Feb.1998.
- [9] H. T. Friss, Fellow, IRE, "Noise Figure of Radio Receiver", proceedings of IRE, 1994

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