Resetting 2-Order Sigma –Delta Modulator in130 nm CMOS Technology

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ABSTRACT-In current scenario high-resolutionADC architecture based on a resetting modulator required high gain operational Transcoductace Amplifier (OTA)and quanitizerin low-voltage nanometer-scale CMOSprocesses because of good speed and calibration-free response are becoming more popular in communication system. Proposed work achieves such high resolution, despite poor component matching using Folded cascodeOTA and two different 1bit and 1.5 bit quantizerwithswiched capacitor Modulator design toreduced thermal noise and a possible optimization of power consumption.Above Quantizeris& OTA in Resetting modulator designed and simulated using H-SPICE having very low power consumptionin 130nm TSMC CMOS technology.

Index Terms :ADC, high-resolution, Resetting ∑Δ modulator,Quantizer,Comparator,D flip-flop.

I. INTRODUCTION

In recent years, high-resolution analog-to-digital conversion based on sigma-delta (Σ-Δ) modulation has become common in many measurement applications including seismic, biomedical and harsh environment sensing. Oversampled sigma-delta modulation has gained much popularity in analog to digital conversion application for their good performance in high frequency, low consumption, low supply voltage and low silicon area occupation. Aggressive device scaling in modern CMOS technology enables high-speed conversion, but high-resolution is hard to achieve[1]. Nyquist-Rate CMOS ADC forlow Power consumption & good dynamic performance achieved without using a input sample/hold amplifier (SHA) by distributing the sampling operation inside the first pipeline stage[3]. Pipelined ADC using open-loop residue amplification to reduse error and power[2].

A resetting converter, also known as single-shot or incremental [4] converter, is essentially a ADC in which the modulator is reset after a pre-determined number of clock cycles. Another type of resetting ADC, known as an extended counting converter uses reuseable hardware and uses high-resolution, compact, and low-power ADC both employs a first order resetting modulator.

ADC architecture based on a resetting modulator achieves high resolution, despite poor component matching .A resetting is the modulator reset after a predetermined number of clock cycles.Resetting removes the memory of the modulator and enables the converter to function as a Nyquist converter. In this way resetting ADCs incorporate the advantages of a modulator in a Nyquist-sampling ADC.

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Desired characterstics of adc can be achive by Figure (1).Here the whole circuit is splitted into three designings, designing of modulator,designing of 10b cyclic ADC and designing of digital filter.For modulator and cyclic ADC we need high gainOTA,So here target design is OTA.

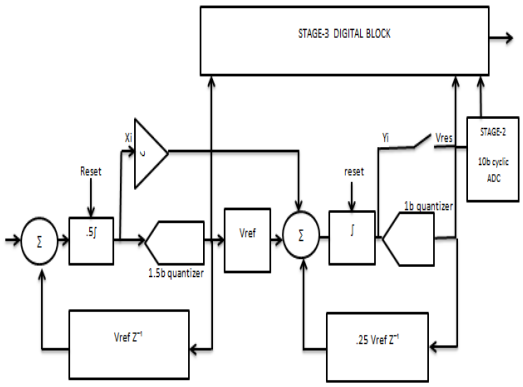

Figure (1):Block diagram of reseting ADC

Stage 1 of the figure(1) is the 2nd order ∑Δ modulator and taken modulator is resetting modulator.

RESETTING MODULATOR

To understand 2nd order ∑Δ modulator it is important to understand the working and benefits of 1st order ∑Δ modulator.

Fig. 2 shows an example of a first order resetting ∑ΔADC which is reset after ' N' clock cycles. Since the average of the digital outputs Di(i=1 to N) is the digital estimate of the input Vin the estimate improves as N increases

$$Vin = Vref \sum Di/N \quad (1)$$

Resetting modulator architectures for high absolute accuracy, including very high linearity , negligible dc offsetwithhigh OSR have been used for low-frequency (<.5 MHz) or DC input signal applications [14]. Here a resetting ADC with large bandwidth is demonstrated. High bandwidth, low OSR incrementalconverters are analyzed in [2].

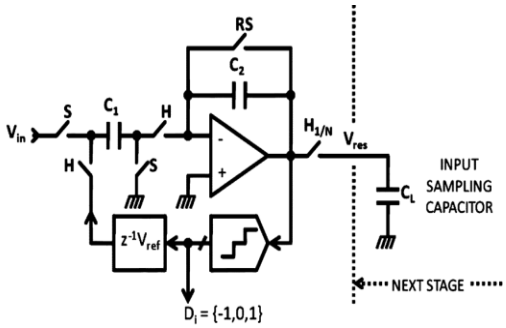

Figure (2):Firstorder resetting ∑Δ modulator with OSR=N

A resetting ∑Δ modulator can replace one or more of the front-end stages of a pipeline ADC. Fig. 2 shows an exampleof a first-order ∑Δ resetting modulator. As with a conventional ∑Δstage, capacitors c1,c2and the op-amp form an integrator.The input signal is sampled onto capacitor c1 and later integrated onto feedback capacitor c2. In each integrating stepi(i=1 to N)the output of op-amp is quantized to Di by the 1.5 b sub-ADC.Di which has a value -1 , 0, or 1, ismultipliedbyVrefto form the DAC feedback of the ∑Δ modulator. A reset switch across feedback capacitor,C2, controlled by clock RS, periodically resets the integrator. In the example shown in Fig. 2, clock RS goes high once every N clock cycles, resetting themodulator,and thus this resetting ∑Δ modulator has an OSR of N.

This final integrator output, Vres, is passed onto a load capacitor,C_L,before reset, through a switch controlled by clock H1/n.

The load capacitor,C_L, is the input sampling capacitor of the next pipeline stage, which quantizes the residueVres of resetting modulator stage.

A good RC-settling match between sampling of the inputsignal onto the capacitors $C_1 - C_4$ and sampling of the input bythe sub-ADC.Without an active front-end S/H, any RC-settlingmismatch between the input signal sampling onto the capacitors $C_1 - C_4$and sub-ADC sampling of the input, can cause an incorrectdecision by the sub-ADC, and this decision error can belarge for a high

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frequency input signal. To avoid such errorsan active front-end S/H is often used, especially in the case ofhigh-resolution converters.

II. PROPOSED ADC ARCHITECTURE

The proposed architecture (Fig. 1) is a pipeline of a secondorderresetting modulator (stage 1) and a 10 b cyclic ADC (stage2).While a first-order resetting modulator achieves astage-gain proportional to the number of integrating clock cycles . A second-order resetting modulator isused in stage 1 to achieve a large effective stage-gain inonly five integrating clock cycles. Such a front-end can typicallyreplace the first two stages of a conventional pipeline ADC. Thisfront-end second-order modulator incorporates all the advantagesof a first-order modulator namely,low required op-amp gain, lower settling error, large toleranceof capacitor mismatch, and the elimination of the need for anactive front-end S/H and lower noise due to oversampling.

The front-end modulator samples and modulates theinput at five times the effective conversion-rate. After every five samples, the residue at theoutput of the front-end is passed to the second-stage cyclicADC and the modulator is reset. The cyclic ADC thenquantizes the residue while the front-end processes thenext 5 samples.

IIICIRCUIT DETAILS

FRONT-END MODULATOR

The SC implementation of the second-order resetting front-end (stage 1 of the ADC) is shown in Figure. 3.

The first and second integrators are implemented using op-amps A1 and A2 respectively.The outputs of first integrator and second integrator are 1.5 b and 1 b quantized to ai and bi, respectively by the two sub-ADCs shown.Both op-amps are implemented as folded cascade OTA.

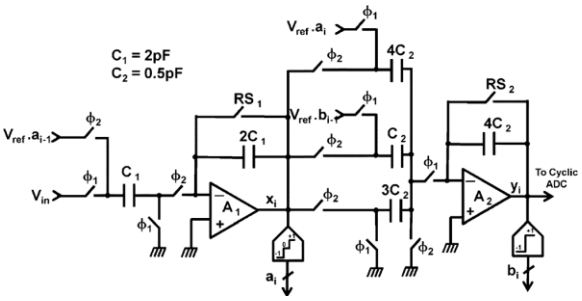
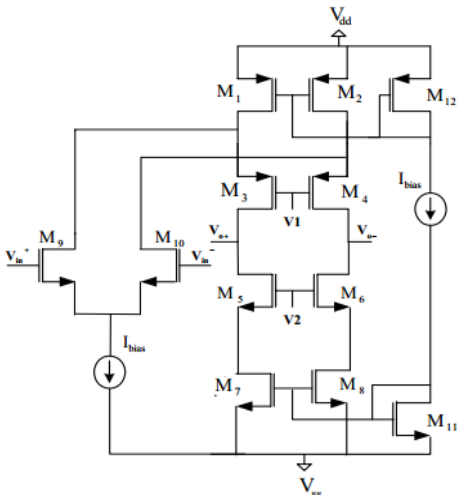


Figure (3):ADC architecture.

FOLDED CASCADE OTA

Folded Cascode OTA has found a broad use because of itsreduced thermal noise and a possible optimization of power consumption.Cascode OTA is shown in Figure 4. The input stage provides the gain of the amplifier.Folding about the cascode node will increase input and output swing range.For a folded OTA bandwidth performance is high.



Figure(4): Folded cascade OTA

QUANTIZER (1bit and 1.5bit)

Figure 5 shows the 1bit quantizer used in this design. The Quantizer consists of a one bit comparator followed by a D flip flop. M1 and M4 are the discharge-current-controllingtransistors which are connected to

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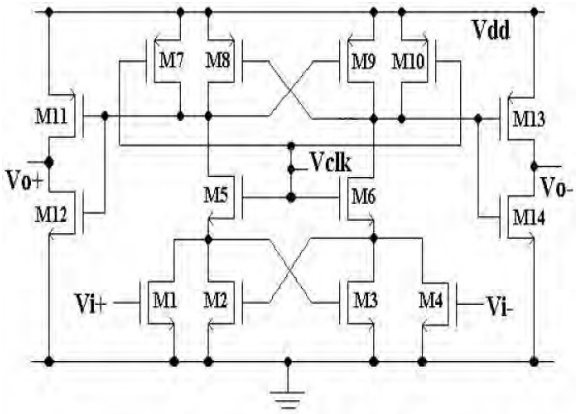
a feedbacknetwork formed by M2 and M3; M5 and M6 aretransfer gates for strobing; M8 and M9 formanother regenerative feedback; M7 and M10 areprecharge transistors; M11-M14 formed twoinverters which act as buffers to isolate the latchfrom the output load and to amplify thecomparator output.



Figure(5): Schematic of latched type comparator

D Flip Flop is presented in the figure 6. When the clock signal is high the transistors M6and M8 are cut off and the transistors M2 and M4 areturned on.

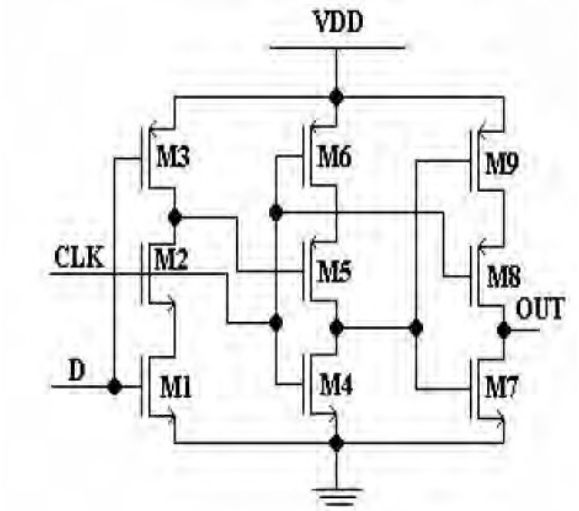


Figure (6):Schematic of D Flip-Flop.

The voltage on M4 drain node is beingpulled to ground and hence forces the transistorM7 cut off. The output node is thereforedisconnected to either positive rail or the groundand the output therefore is being latched to theprevious value. On the other hand, the transistorsM1-M3 formed a clock-buffered inverter. Whenthe clock signal is high, the drain voltage of thetransistor M2 is the output of this inverter.

Similiarly we can also design 1.5bit quantizer as shown in figure(7)

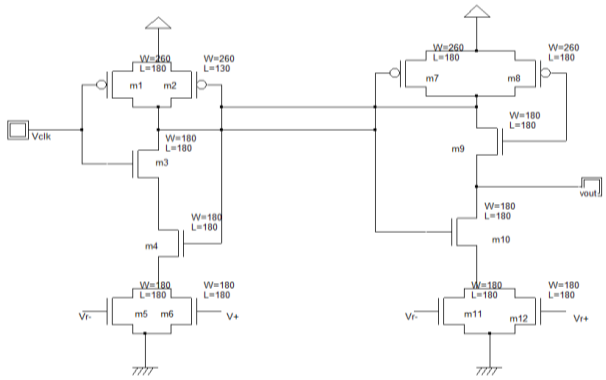


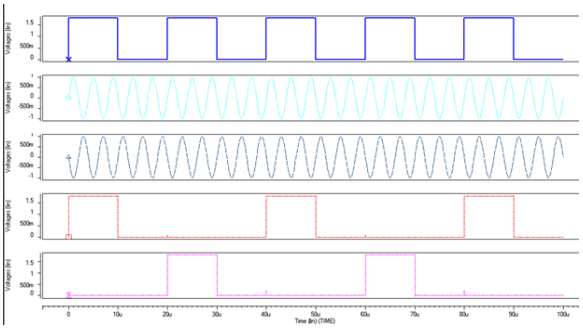
Figure (7):Schematic of 1.5bit Quantizer.

IV.MEASUREMENT RESULT

Designing of overall circuit in 130nm technology is done

TABLE1: Power Chart

CIRCUIT	POWER(w)
Folded cascade OTA	~10octto
Quantizer(1bit)	16.28n
Quantizer(1.5bit)	.011m
Reseting modulator	.1m



Figure(8):Waveform of 1bit Quantizer

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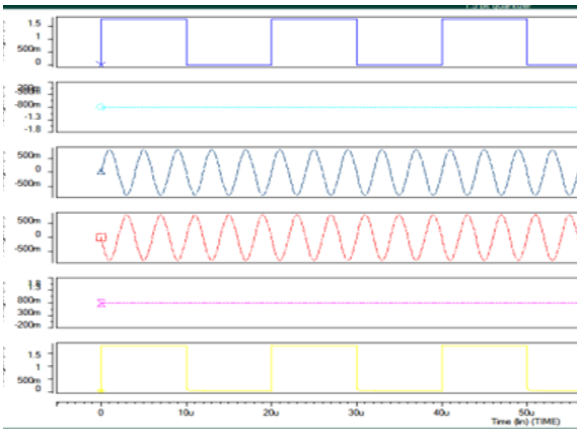
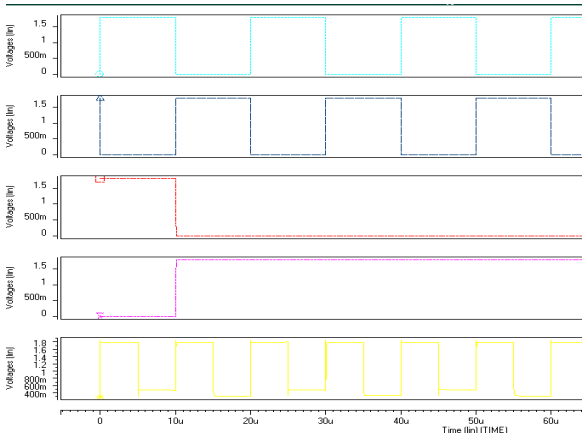


Figure(9):Waveform of 1.5bit Quantizer



Figure(10):Waveform of Resetting sigma-delta modulator

TABLE 2: List of parameters of transistor in 1bit Quantizer

S.N.	Device Parameter	Value
1	M1	W=260nm L=130nm
2	M2	W=260nm L=130nm
3	M3	W=260nm L=130nm
4	M4	W=260nm L=130nm
5	M5	W=260nm L=130nm
6	M6	W=260nm L=130nm
7	M7	W=130nm L=130nm
8	M8	W=130nm L=130nm
9	M9	W=130nm L=130nm
10	M10	W=130nm L=130nm
11	M11	W=130nm L=130nm
12	M12	W=130nm L=130nm
13	M13	W=130nm L=130nm
14	M14	W=130nm L=130nm

TABLE 3: List of parameters of transistor in D flip flop

S.N.	Device Parameter	Value
1	M1	W=2600nm L=130nm
2	M2	W=130nm L=130nm
3	M3	W=130nm L=130nm
4	M4	W=2600nm L=130nm
5	M5	W=2600nm L=130nm
6	M6	W=130nm L=130nm
7	M7	W=2600nm L=130nm
8	M8	W=2600nm L=130nm
9	M9	W=130nm L=130nm

TABLE 4: List of parameters of transistor in 1.5bit Quantizer

S.N.	Device Parameter	Value
1	M1	W=260nm L=130nm
2	M2	W=260nm L=130nm
3	M3	W=130nm L=130nm
4	M4	W=130nm L=130nm
5	M5	W=130nm L=130nm
6	M6	W=130nm L=130nm
7	M7	W=260nm L=130nm
8	M8	W=260nm L=130nm
9	M9	W=130nm L=130nm
10	M10	W=130nm L=130nm
11	M11	W=130nm L=130nm
12	M12	W=130nm L=130nm

V.CONCLUSION

This paper proposes a swiched capacitor resetting sigma delta modulator in ADC.Explanations are presented about resetting modulator.Power analysis is done for each component as Quantizer, Folded

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cascade OTA,and Resetting modulator in 130nm technology.

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