A Novel Approach to design High Speed MAC Unit

Mr. Yogesh Kumar[1],Mr. Kanak Kumar[2], Mr. Santosh Yadav[3], Mr. Abhishek Gupta[4]

Digital Communication [1,2,3], Embedded Systems and VLSI Design[4]

Department of Electronics & Communication

M.tech-IV^th semester[1] , Professor[2,3], M.tech-2012 pass out and Software Engineer[4]

Millennium Institute of Technology[1,2,3]
Gyan Ganga Institute of Technology and Science and Tata Consultancy Services[4]

Rajeev Gandhi Technical University, Jabalpur, Madhya Pradesh, India[1,2,3]
Rajeev Gandhi Technical University, Jabalpur, Madhya Pradesh, India and TCS Pune[4]

Abstract: **- Today in digital technology the ever increasing demand in enhancing the ability of processors to handle the complex and challenging processes has resulted in the integration of a number of processor cores into one chip. Still the load on the processor is not less in generic system. This load is reduced by supplementing the main processor with Co-Processors, which are designed to work upon specific type of functions like numeric computation, Signal Processing, Graphics etc. in which MAC Unit is most dominant Co-Processor and work as heart of digital signal processors. Faster Operations are of extreme importance in MAC Unit. The speed of MAC Unit depends greatly on the multiplier; after deep study and analysis we found that the efficiency of Urdhva Triyakbhyam-Vedic method for multiplication is much better in the comparison to other conventional multipliers, which strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermedUrdhvaiate products. This Sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time. Many researchers and scientists have done intensive research upon this multiplier at different level, and introduced so many architectures to further enhance the speed of conventional Vedic multiplier. We have seen that out of these CSA based Vedic multiplier architecture, proposed by Abhishek Gupta, provides much better result in terms of speed. In this paper, after a gentle introduction of this Sutra, we have represented the digital circuitry for this CSA based Vedic multiplier. Then we have proposed digital hardware for MAC Unit using this proposed multiplier. After this we have provided comparative results of Vedic multiplier, proposed by Abhishek and proposed design for MAC unit shows improvement of speed over the conventional designs of MAC unit.**

Keywords: **- Vedic multiplier, Urdhva Triyakbhyam sutra, Carry Save Adder (CSA), MAC Unit.**

I. INTRODUCTION

We have entered in the digital domain where the digital signal processing is of main concern. The performance of DSP is mainly dependent upon the MAC unit. So by optimizing the MAC unit we can optimize performance of the Digital Signal Processors, and in MAC unit Multiplication is the main operation where our proposed design of MAC unit can be very useful. Multiplication is the most time consuming amongst the basic mathematical calculation. With these considerations, it is always important to have fast and efficient mechanism to implement mathematical functions. As a student in India, Vedic Mathematics is a name which is heard many times with reference to the techniques for solving mathematics problem mentally. One of the main purposes of Vedic mathematics is to transform the tedious calculations into simpler, orally manageable operation without much help of pen and paper. Any ordinary human can perform mental operations for very small magnitude of numbers and hence Vedic mathematics provides techniques to solve operations with large magnitude of numbers easily. Vedic mathematics provides more than one method for multiplication operations. For each operation there is at least one generic method provided along with some methods which are directed towards specific cases simplifying the calculations further. [11, 29] has described the Vedic mathematics thoroughly. Vedic mathematics provides algorithms to simplify the mathematics and hence is perfect solution for the problem stated. After a thorough and comparative study we have found that Vedic multiplier designed by [4] is better than other available multipliers.

Before designing our proposed Arithmetic unit is highly required to elaborate the working of the Vedic multiplier:-

As per [29] Urdhva Triyakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise". To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (5498 × 2314). The conventional methods already know to us will require 16 multiplications and 15 additions. An alternative method of multiplication using Urdhva Triyakbhyam Sutra is shown in following figure. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one

of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero.

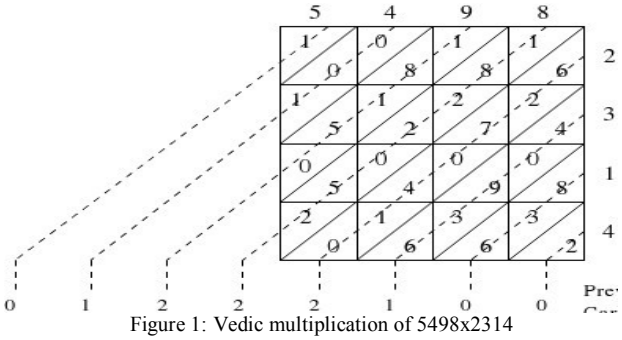

Figure 1: Vedic multiplication of 5498x2314

After a thorough study we have found that [4] has introduced a new approach to design the architecture of Vedic multiplier, As if we do not concern the vedic multiplier there are two popular methods to perform multiplication operation first one is Wallace due to its high speed because of its unique addition tree structure and second one is Booth which takes less area to perform multiplication by the combination of these two techniques a high speed multiplier has been designed named as Modified Booth Wallace Multiplier. This paper has also used the combination of Urdhva Triyakbhyam sutra with unique addition tree structure similar to Wallace for multiplication. Here [4] has used conventional Vedic multiplier for design of 2x2 bit multiplier and for higher level multiplier [4] has replaced the Conventional Adder which is required during the Partial Product generation with unique addition tree structure similar to Wallace addition tree structure and found that our proposed design is better than conventional Vedic multiplication hardware in terms of speed.

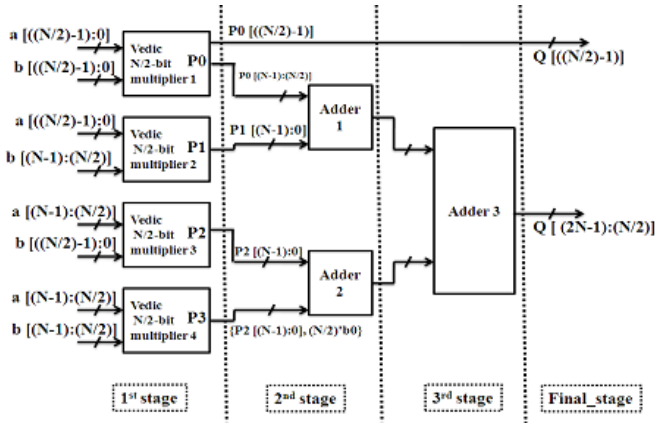

Figure 2: NxN bit Vedic multiplier architecture [4]

II. PROPOSED MAC UNIT

Our Proposed NxN bit MAC Unit is shown in the following:-

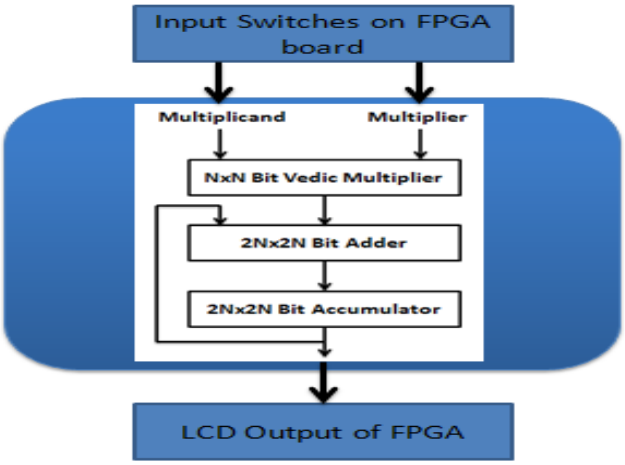

Figure 3: Block diagram of MAC Unit [35]

Here multiplier and multiplicand are the two N bit inputs of our MAC Unit. And other sections of the design are self-explanatory. We have compared various different popular adders and found that XILINX CORE IP adder is providing the better speed in comparison to other adders. We have also compared the various Multipliers and found that Vedic Urdhva Triyambakam is the better multiplier in comparison to other conventional Multipliers. Now here a basic question arises that why we have not used Multiplier of XILINX CORE IP, the answer is simple is if we put clock in that XILINX CORE IP multiplier then its SET-UP and HOLD-TIME gets increased in comparison to our proposed Vedic Multiplier.

III. COMPARATIVE RESULTS OF PROPOSED VEDIC MULTIPLIER FOR MAC UNIT

To show the efficiency of proposed Vedic multiplier for MAC unit, it has been implemented and compared with other popular multiplier structures based on different multiplication algorithms on the same platform of target FPGA, which has been used to implement these popular multiplier structures. Comparison tables are shown below:-

In the following given table which target FPGA has been used belongs to Virtex 2P (family), XC2VP2 (device), FG 256 (Package), -7 (speed grade).

Maximum Combinational Path Delay (in ns) for different multipliers at eight bit level						
Karatsuba [19]	Vedic Karatsuba [19]	Modified Booth-Wallace [21]	Vedic with partitioning [21]	Conventional Vedic [19]	Vedic with CSA [12]	Vedic multiplier [4]
31.029	18.695	15.815	15.685	15.418	13.07	11.886

Table 1: Comparative table

In the following given table which target FPGA has been used belongs to Spartan 3 (family), XC3S50 (device), PQ 208 (Package), -4 (speed grade).

Maximum Combinational Path Delay (in ns) for different multipliers at eight bit level			
Array [13]	Booth [13]	Conventional Vedic [13]	Vedic multiplier [4]
32.01	29.549	24.16	19.467

Table 2: Comparative table

In the following given table the target FPGA used belongs to Virtex 2P (family), XC2VP2 (device), FG 256 (Package), -7 (speed grade).

Maximum Combinational Path Delay (in ns) for different multipliers at different bit levels							
N bit level multiplier	Karatsuba [19]	Vedic Karatsuba [19]	Modified Booth-Wallace [21]	Vedic with partitioning [21]	Conventional Vedic [21]	Vedic with CSA [12]	Vedic Multiplier [4]
4-Bit	---	---	---	---	---	8.405	8.387
8-Bit	31.029	18.695	15.815	15.685	15.418	13.070	11.886
16-Bit	46.811	27.81	36.071	23.063	22.604	18.580	15.718
32-Bit	82.834	49.864	---	---	35.76	---	20.574

Table 3: Comparative table

In the following given table the target FPGA used belongs to Spartan 3 (family), XC3S50 (device), PQ 208 (Package), -4 (speed grade).

Maximum Combinational Path Delay (in ns) for different multipliers at different bit levels				
N bit level multiplier	Array [13]	Booth [13]	Conventional Vedic [13]	Vedic Multiplier [4]
8-Bit	32.01	29.549	24.16	19.467
16-Bit	60.928	70.809	36.563	29.012

Table 4: Comparative table

By implementing the proposed Vedic multiplier for MAC unit on the same reconfigurable hardware as shown in [12], [13], [19] and [21], make the platform (hardware) independent, algorithmic, technique and approach based comparison. So by this it can be concluded that the algorithm and approach which has been proposed to design MAC unit using proposed Vedic multiplier, in this research work, is better in comparison to the other popular algorithms and approaches shown in [12], [13], [19] and [21].

IV. CONCLUSION

We have proposed a design for the NxN bit MAC Unit using a unique Vedic multiplier which provides better results with respect to the conventional MAC unit .This Proposed MAC Unit is very useful for designing the high speed digital signal processors. And thus the optimized designs can be made for FFT, FIR, IIR etc.

V. REFERENCES

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