Design and implementation of IP Core Based Architecture of Telecommand System on chip (SoC) on FPGA

Mr. Anjan d[1], Mrs.Ashwini.s.shivannavar[2], Dr. M. Z Kurian[3]

ABSTRACT*: *The emerging developments in semiconductor technology have made possible to design entire system onto a single chip, commonly known as System-On-Chip (SoC). As the complexity of the remotely located physical devices increases, the requirement for a greater telecommanding capability and efficiency arises. This is achieved by embedding pre-designed functions into a single SoC, which utilizes specialized reusable core (IP cores) architecture into complex chip. This papert is concerned with the design of telecommand and telemetry system for transfer of signals by the integration of Memory unit, telecommand and telemetry processor, EDAC unit (Error Detection And Correction). The results are analyzed using VIRTEX 4 FPGA devices. The IP core based architecture is implemented on FPGA device

Keywords*: *EDAC unit, telecommand, IP cores, Hamming code.

I. INTRODUCTION

A system on a chip (SoC) is an Integrated Circuit (IC) that integrates all components of a computer or other electronic system into a single chip. it is a collection of all components and subcomponents of a system on to a single chip. SoC design allows high performance, good process technology, miniaturization, efficient battery life time and cost sensitivities. This revolution in design had been used by many designers of complex chips, as the performance, power consumption, cost, and size advantages of using the highest level of integration made available have proven to be extremely important for many designs .As the complexity arises, are designers to start designs at higher abstraction levels.

The emerging technologies in the field of semiconductors, along with the use of the System-on- Chip (SoC) design, have made this possible. System development based on the use of a core-based architecture, where the reusable cores are interconnected by means of a standard on-chip bus, which is the most common way to integrate the cores into the SoC .This design methodology has been proven to be very effective in terms of development time and productivity since it reuses existing Intellectual Property (IP) cores. In a SoC design which uses multi-million gates the design and test engineers face various problems such as signal integrity problems, heavy power consumption concerns and increase in testability challenges.

The semiconductor industry has continued to make impressive improvements in the achievable density of very large-scale integrated circuits .In order to keep pace with the levels of integration available, engineers have developed new methodologies and techniques to manage the increased complexity inherent in these large chips. One such emerging methodology is system-on-chip design, wherein predesigned blocks called Intellectual Property(IP) blocks, IP cores or virtual components are obtained from internal sources or third parties and combined into a single chip. These reusable IP cores may inc1ude embedded processors, memory blocks, interface blocks and components that handle application specific processing functions. The corresponding software components are also provided in a reusable form which inc1ude real time operating systems, kernels, library functions and device drivers [5].

In the past, the concept of SoC simply implied higher and higher levels of integration .That is it was viewed as migrating a multichip System-on-Board (SOB) to a single chip containing digital logic ,analog/mixed signal and RF blocks . The primary drivers for this direction were the reduction of power ,smaller form factor and the lower overall cost .It is important to recognize that integrating more and more functionality on a chip has always existed as atrend by virtue of Moore' s Law, which predicts that for every 18-24 months the number of transistors on a chip will doubled .With the increasing integration of SoC design over years ,it has now become the driver for many other improvements in the integrated Circuits (IC) industry.

II. LITERATURE SURVEY

The work titled "Reconfigurable System-on-a-Chip Based Platform for Satellite On-Board Computing" Daixun Zheng August 2005. In this Phd work a generic System-On-a-Chip (SoC) computing platform for on-board applications is proposed. The SoC platform is built on a modular principle containing both space-specific and general functional blocks, which allows that to be easily tailored to satisfy different requirements of on-board subsystems or payloads. By making use of this design concept, an On-Board Computer (OBC) is selected as the reference design. The resulting of System-On-a-Chip On-Board Computer (SoC-OBC) design is get used. This is the first attempt to

Manuscript received May, 2014.

***Mr. Anjan D**, Mtech, Sri Siddartha institute of technology, ., Tumkur, Karnataka, India, Phone/ Mobile No9743774010*

***Mrs Ashiwini S Shivannavar**, Asst Prof, Sri Siddartha institute of technology, Tumkur,,Karnataka,India*

Dr. M. Z Kurian, , *HOD, Sri Siddartha institute of technology, Tumkur,,Karnataka,India*

ISSN: 2278 – 1323

implement a reconfigurable SoC-OBC which is totally integrated by the soft VHDL IP cores[1].

The paper titled "IP Core Based Architecture of Telecommand System-on-Chip (SoC) for Spacecraft applications" Manoj G , Rajesvari., Angelin Ponrani.M. in 2013.In this paper is concerned with the design of telecommand system for transfer of signals from ground station to space station by the integration of SRAM(Static Random Access Memory), ARM (Advanced RISC Machine) Processor, EDAC unit (Error Detection And Correction). The IP core based architecture using VIRTEX 4 FPGA device makes a trade-off between frequency and time delay with 48% increase in operating frequency and having a minimum timedelay of about 5% [5].

III. Design Methodology

In this paper an On-Board System (OBS) of a small Satellite is implemented in the form of a telecommand System-on-a-Chip (SoC). Soft intellectual property (IP) cores written in the hardware description language VHDL are used to build the system on-a-chip. The resulting subsystem is the integration of SRAM, PROCESSOR and EDAC Unit was designed. The Block Diagram of the design is shown in Fig. 1.

The telecommand input data is send from ground station to the space station it is given as input to the SRAM . In space applications it is weil known that in Low Earth Orbit (LEO) stored digital data suffers from SEUs. These upsets are induced naturally by radiation. Bit-flips caused by SEUs are a well-known problem in memory chips and error detection and correction techniques have been an effective solution to this problem. For the secure transaction of data between the CPU of the on board computer and its local RAM, the program memory has generally been designed by applying the Hamming code in the error detection and correction unit so that the errors can be detected and corrected and the resultant output will be a error free data. The resultant error free data is fed to the processor ,so that it will process the error free data and also it will collect all the on -board data signals and produce the resultant data output[5].

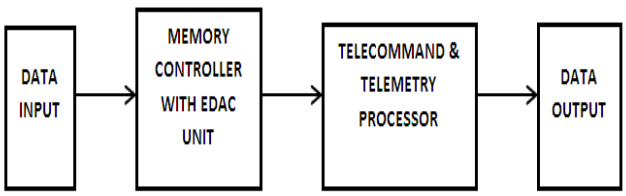

Fig. 1 Block diagram of SoC design

A. Design of SRAM

Static random-access memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The Dynamic RAM memory can be deleted and refreshed while running the program, where as Static RAM is not possible to refresh the programs. But it is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

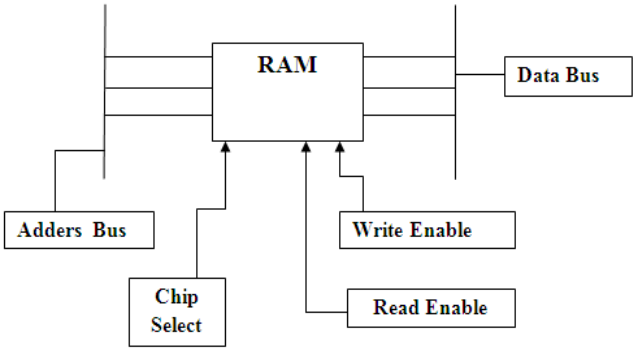

Fig2 Block diagram of 2K x32 bit SRAM

The basic architecture of a static RAM includes one or more rectangular arrays of memory cells with support circuitry to decode addresses, and implement the required read and write operations.The block diagram of 2k x 32 bit SRAM is shown in Fig.2. SRAM memory arrays are arranged in rows and columns of memory cells called wordlines and bitlines, respectively. Each memory cell has a unique location or address defined by the intersection of a row and column, which is linked to a particular data input/output pin. The total size of the memory, the speed at which the memory must operate, layout and testing requirements, and the number of data inputs and outputs on the chip determines the number of arrays on a memory chip. Memory arrays are an essential building block in any digital system. The aspects of designing an SRAM are very vital to designing other digital circuits. The majority of space taken in an integrated circuit is the memory. Consider an Nxn SRAM array where 'N' indicates the number of bytes and 'n' indicates the byte size. The size of an SRAM with m address lines and n data lines is 2/\m words, or 2/\ m x n bits [5]

B. Design of EDAC Unit

Error Correction Codes (ECC) and error detection and correction (EDAC) schemes have been implemented in memory designs to tolerate faults and enhance reliability. Extra check bits (parity bits) have to be stored along with the information bits, so the hardware overhead includes the encoding decoding circuit and the memory space for check bits. ECC can protect the memory from attacks of hard and soft errors. The modified Hamming Code and Hsiao Code are the most widely used Single-Error Correctable and Double-Error Detectable (SEC-DED) codes[5].

Hamming code error detection and correction methodology is used for error free communication in communication system. The transmitted and received data between source and destination may be corrupted due to any type of noise. In order to find the original transmitted data we use Hamming code error detection and correction technique. In hamming code error detection and correction technique to get error free data at destination, we encrypt information data according to even and odd parity method before transmission

of information at source end. Hamming codes are still widely used in computing telecommunication and other applications. lt is also applied in data compression and block turbo codes. Because of the simplicity of Hamming codes they are widely used in computer memory.

A linear block code takes k data bits and produces an n-bit block. In many applications, systematic codes that preserve the original k data bits and simply add n-k parity bits are preferred. A given linear block code can be described by its generator matrix G. Given a block of k data bits, the n bits codeword is obtained by multiplying the data block by the generator matrix. As an example, the generator matrix for an SEC Hamming code for $k = 8$ and $n = 12$ is shown in (1). The last four columns define the added parity bits. The generator matrix is used to encode the data block

$$G = \begin{bmatrix} 1&0&0&0&0&0&0&0&1&1&0&0 \\ 0&1&0&0&0&0&0&0&1&0&1&0 \\ 0&0&1&0&0&0&0&0&0&1&1&0 \\ 0&0&0&1&0&0&0&0&1&1&1&0 \\ 0&0&0&0&1&0&0&0&1&0&0&1 \\ 0&0&0&0&0&1&0&0&0&1&0&1 \\ 0&0&0&0&0&0&1&0&1&1&0&1 \\ 0&0&0&0&0&0&0&1&0&0&1&1 \end{bmatrix}. \quad (1)$$

To decode a codeword, the parity check matrix H is used. This matrix when multiplied by a codeword will be an all zero vector if there are no errors. If there an error, the value of that vector, will usually called syndrome, will serve to detect the error and correct it. The H matrix of the SEC Hamming code previously considered is shown in (2). It can be observed that all columns in the matrix are different. This means that any single-bit error will produce a different syndrome, and therefore the error can be corrected

$$H = \begin{bmatrix} 1&1&0&1&1&0&1&0&1&0&0&0 \\ 1&0&1&1&0&1&1&0&0&1&0&0 \\ 0&1&1&1&0&0&0&1&0&0&1&0 \\ 0&0&0&0&1&1&1&1&0&0&0&1 \end{bmatrix}. \quad (2)$$

The structure of the encoder and decoder can be explained using the G and H matrixes. Encoding is simply computing the multiplication of the input data block by the G matrix. This requires a number of XOR gates for each column in G that is proportional to the number of ones in that column. Decoding starts by multiplying the H matrix by the codeword. This requires a number of XOR gates for each row in H that is proportional to the number of ones in that row. Then, the obtained syndrome must be checked against every column in H and if there is a match; that is the bit in error that is then corrected. Each of those checks requires an $n - k$ input AND gate. The encoder for the Hamming code used as an example is illustrated in Fig. 3. The data bits (di) are the inputs and the parity check bits (ci) the outputs[2].

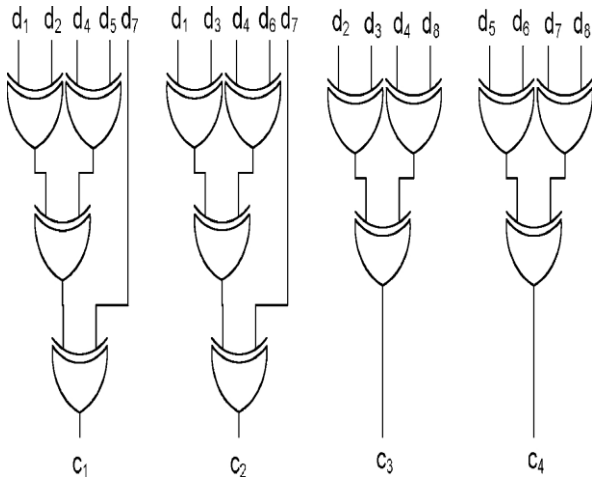

Fig.3. Encoder for the SEC Hamming code with k =8 [2].

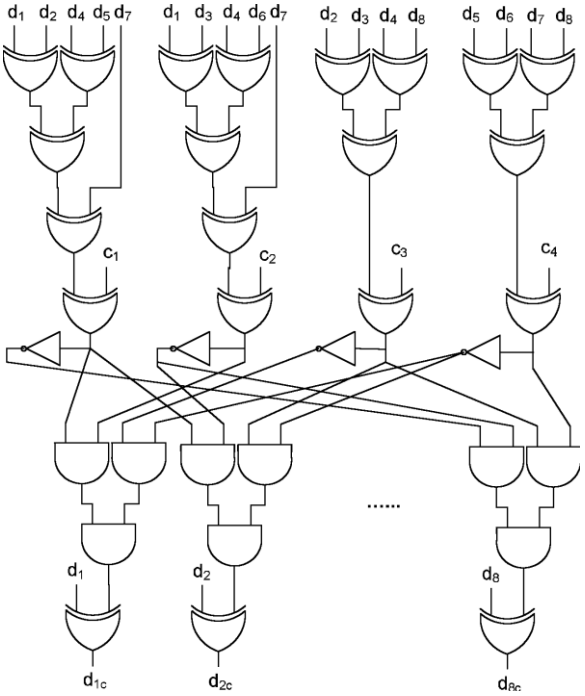

Fig. 3.Structure of the decoder for the SEC Hamming code with k = 8.[2]

The structure of the decoder is shown in Fig. 3. In this case, the data bits (di) and the parity check bits (ci) are the inputs, and the outputs are the corrected data bits (dic). It can be observed that the complexity and delay is larger in the case of the decoder as it is normally the case for most ECCs.

C. Design of Processor

In spacecraft application requirement, the star topology is selected, it is simple to implement and it has less complexity and it satisfies all the requirements of TC-TM systems. The PAN coordinator and FFD's are wireless devices and they are configured as star topology. The demodulator, decoder and PAN coordinator is TC uplink part, whereas PAN coordinator, formatter, modulator form TM down link. Both transceiver and antenna is parts of RF

system which is interfaced with TC and TM systems. The TC uplink part is used for commanding and ranging the satellite and TM down link is used for receiving health parameter and payload data from the subsystems of the satellite and transmitted to ground station. The PAN coordinator is interfaced with both TC and TM systems. The FFD's are interfaced with other subsystems of the satellite. The figure 1 shows ZigBee based wireless Satellite architecture.

In PAN coordinator, received command is converted into ZigBee format and it is broadcasted in wireless mode to all the FFD's in subsystems and intended FFD receives a wireless command in ZigBee format. It is decoded and converted as pulse or level or data command and it is executed in the subsystem end. Each FFD can execute any number of commands as required by the subsystems. In this fashion commands are distributed to subsystems through FFD's in wireless mode. The FFD's receives different heath parameters and payload data from respective subsystems and transmits to PAN coordinator in wireless mode using ZigBee data frame format in round robin fashion. The PAN coordinator intern formats and modulates and sends data through down link to ground station. In our design, PAN coordinator and FFD's are main powered.

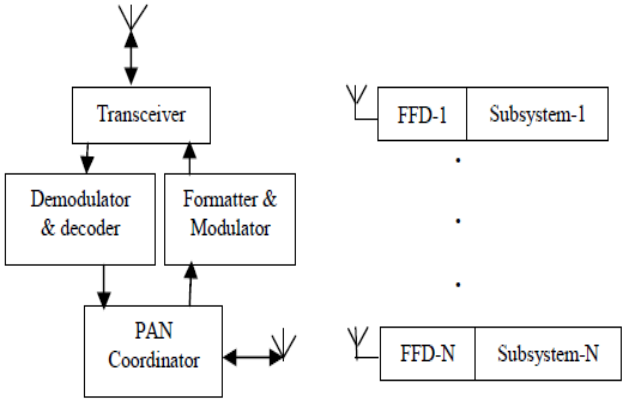

Fig 4. Telecommnd and Telemetry processor

IV. Results And Discussions

Table 1 shows synthesis report which gives information of the cell usage, device utilization constraint, timing summary. The device utilization gives information of the total hardware utilized. In this the integration of SRAM, EDAC unit and the processor is done so the data input is fed to the SRAM ,due to some radiations in the space the data stored in the SRAM gets flipped .It is passed to the EDAC unit in order to detect and correct the errors. From EDAC unit it is passed to the processor and it will process the data and provides the desired output

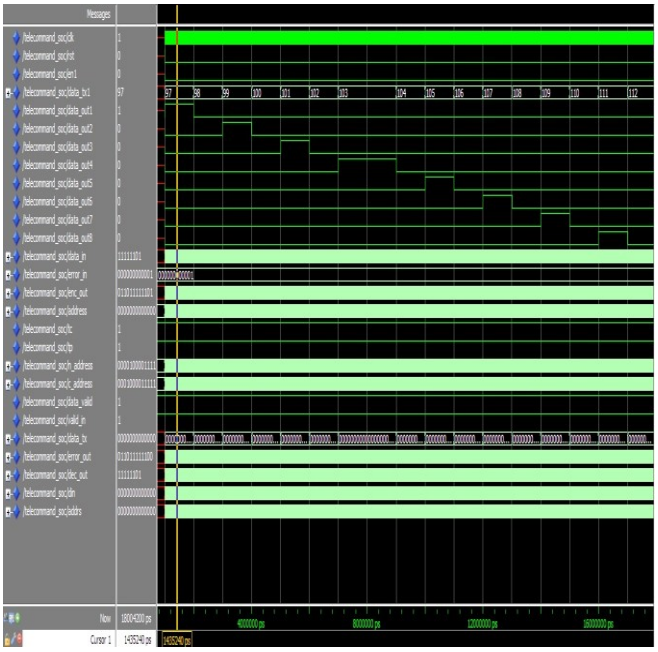

Fig 5. Simulation Results

LOGIC UTILIZATION	AVAILABLE	USED	UTILIZATION (%)
NUMBER.OF.SLICE REGISTERS	10,944	315	2
NUMBER.OF.SLICE LUT'S	10,944	134	1
NUMBER OF BONDED IOBS	320	1	1

Table 1 Xilinx Device Utilization Summaries

V. Conclusion

This paper proposes a summary on system on chip and IP core based design technology. The primary focus in SoC verification is on checking the integration between the various components. Rather than implementing each of these components separately, the role of the SoC designer is to integrate them onto a chip to implement complex functions in relatively short time. Since IP cores are pre-designed and pre--verified, the designer can concentrate on the complete system without having to worry about the correctness or performance of the individual components. The conventional telecommand system is designed with SRAM,EDAC unit and Processor and they are integrated to form a SoC design. The simulation of each system is done separately and then integrated to produce final output.

ACKNOWLEDGMENT

The satisfaction and euphoria that accompany the successful completion of any task would be incomplete without mention of the people who made it possible and support had been a constant source of encouragement which crowned my efforts with success.

I am deeply indebted and would like to express my sincere thanks to our beloved Principal **Dr. K.A.Krishnamurthy**, for providing me an opportunity to do this paper.

My special gratitude to **Dr. M.Z.Kurian**, HOD, Department of E&C, S.S.I.T for his guidance, constant encouragement and whole hearted support.

My sincere thanks to my guide **Mrs. Ashwini.S.Shivannavar**, Department of E&C, S.S.I.T for her guidance, constant encouragement and whole hearted support.

REFERENCES

[1] Daixun Zheng "Reconfigurable System-on-a-Chip Based Platform for Satellite On-Board Computing" .pdf. (August 2005)

[2] Pedro Reviriego, Salvatore Pontarelli, Juan Antonio Maestro, and Marco Ottavi "A Method to Construct Low Delay Single Error Correction Codes for Protecting Data Bits Only" Ieee Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 32, No. 3, March 2013

[3] Mr.Anjan.D, Mrs.Ashwini.s.shivannavar, Dr. M. Z. Kurian.National Conference on VLSI Signal Processing, Communication and Soft Computing (NCVCS-14) -2014

[4] P.N.Ravichandran, Sunil,Satish Sharma, H.S.Vasudevamurthy, M.Vanitha, P.Lakshminarsimhan, International Conference on Advances in Recent Technologies in Communication and Computing page no274-278 2009

[5] Rajesvari., Manoj G, Angelin Ponrani.M)"IP Core Based Architecture of Telecommand System-on-Chip (SoC) for Spacecraft applications "International Conference on Signal Processing, Image Processing and Pattern Recognition"-2013

