Performance Analysis Of Double Edge triggered D flip flop

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Abstract— **For low power VLSI circuits applications power consumption is a crucial. This paper proposed a new Double Edge Triggered D-Flip Flop (DETFF) which is suitable for low power applications. The proposed DETFF having minimum number of clocked transistors than existing designs. In that proposed design the transmission gates are replaced by NMOS to reduce the power. Simulation using SPICE and a 180 nm CMOS technology shows that this DETFF has ideal logic functionality, a simpler structure, lower lowest average power and least delay than existing designs. Further, the average power and the PDP are improved by 65.61% and 25.85% when compared with existing design respectively, which showing that proposed design is appropriate for low power and high performance applications.**

Index Terms— DETFF, power, delay, PDP .

I. INTRODUCTION

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability,power considerations were mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed in VLSI design. One of the primary driving factors has been the remarkable success and growth of the class of wireless communications systems (personal digital assistants and personal communicators) which demand high-speed and complex functionality with low power consumption. Many digital circuits are used synchronous circuits for designing because it reduce the complexity of circuit design.

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. During recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data. Power dissipation is an important parameter in the design of VLSI circuits, and the clock network is responsible for a substantial part of it (up to 50%). When the supply voltage is decreased the speed of the logic circuits might be diminished due to reduction in effective input voltage to the transistors.

Mostly without accurate power prognostication and enhance tools the design for low power issues can't be overcome . So calculate the power dissipation in digital circuit it necessary to used certain tools during the design to meet the power constraints to avoid the costly redesign effort. Edge triggered flip-flops are most used synchronous digital circuits. D-type flip-flop's is the basic building blocks in modern VLSI systems and it showing benefaction a important part of the total power dissipation in digital system[12]. In synchronous VLSI circuits the total clock related power consumption is done by the power

consumption in the clock circuits, clock buffers, and the flip-flops [3]. There are many factor where the Power consumption is dependent, as $P = \alpha C V^2 f$ [5] here the power is proportional to the square of the voltage.

To reduce power consumption the voltage scaling is the most effective way . Also voltage scaling is associated with threshold voltage scaling which can be create leakage power to increase exponentially. By using double-edge triggered flip-flops (DETFFs), the clock frequency can be significantly reduced ideally, cut in half while preservative the rate of data processing. The DETFF design is valuablet saving energy both on the distribution network (by halving the frequency) and flip-flops. It is preferable to reduce circuits' clock loads by minimizing the number of clocked transistors.

The main courtesy has been in improving the performance of the VLSI circuits. That paper is prearrange in that manner the Unit II clarify the conformist DETFF circuits and new proposed DETFF circuit. And unit IV is talk over nominal simulations along with analysis. Comparing new proposed design and conformist designs in terms of average power, delay and PDP in unit V. Paper ends in unit VI with the deduction .

II.DOUBLE EDGE TRIGGERED FLIP-FLOP IMPLIMENTATION

Double Edge Triggered Flip Flop's can be implemented in various ways for reduced of power consumption and minimum delay by using transmission gates such designs are having clock signal internal and external as well. Few contructional unit are studied as:

CONTRUCTIONAL UNIT OF DOUBLE EDGE TRIGGERED FLIP-FLOP

The DET flip flop proposed in [1] is exposed in figure 1. This flip-flop is basically a Master Slave flip-flop structure. having two data paths. The upper data path consists of a Single Edge Triggered flip-flop implemented using transmission gates. This works on positive edge. The lower data path consists of a negative edge triggered flip-flop implemented using transmission gates. Both the data paths have feedback loops connected such that, whenever the clock is stopped, the logic level at the output is retained. This flip flop has 20 transistors. In these 20 transistors, 10 transistors are clocked transistors.

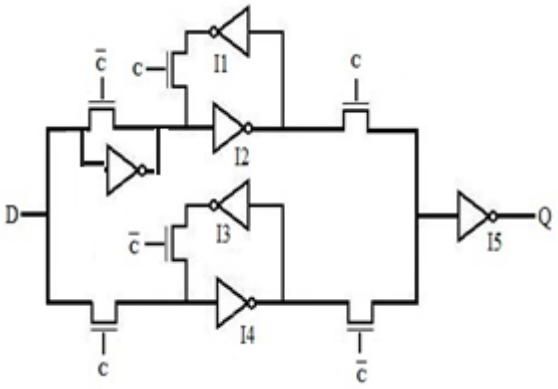
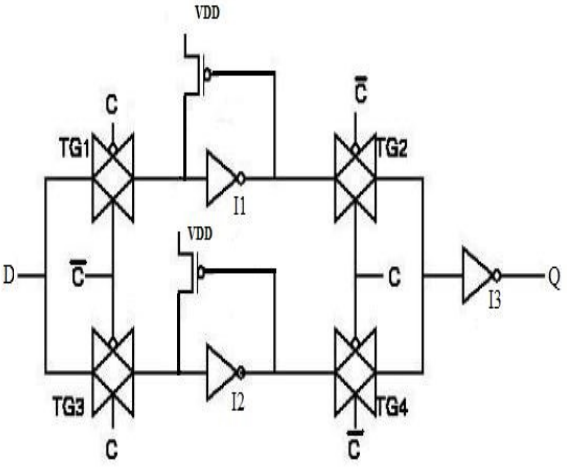


Fig.1: Proposed DEFET in [1]

DET flip-flop proposed in [2] is shown in figure 2. This flip flop is similar to figure1 except that feedback has been changed. On rising edge the upper data path is triggered and on falling edge lower data path is triggered. In the fig. 2 an inverter and a PMOS transistor are used to hold the logic level when the Transmission gate is closed. When the data value high, the inverter is switch the signal to low, so will be make the PMOS transistor which pull the data up to the high. When value of data is low then the inverter switch the signal to high, which will isolate the data from VDD and keep the value low. for high output, this type of flip-flop is give static functionality since a PMOS transistor connected to VDD is used in the feedback network, but the static functionality for low output is not provided by this flip-flop. That will make the circuit to behaving like a dynamic circuit.



III PROPOSED TECHNIQUE

The proposed Double Edge Triggered Flip-Flop (DETFF) design is exposed in Fig. 3. The contructial unit of flip-flop is a Master Slave flip flop which consists of two data paths. The proposed flip-flop's operation is same to that of figure 1, but number of clocked transistors is reduced from 10 to 6 by replacing the transmission gates by using n-type pass transistors.The designed circuit using 6 clocked transistors and total 10 transistors . Inverter shown in figure is made by using sub-circuit design. Also W/L ratio is adjusted for making the transistors working in saturation regio. Basically, n-type pass transistors give weak high but in figure 3, the n-type pass transistors is followed by an inverter, which results in strongly high. So the proposed DETFF is free from threshold voltage loss problem of pass transistors in figure 3. Therefore the feedback network of figure 1 is distorted by replacing the p-type pass transistor by n-type pass transistor since, the area incurred by NMOS is less than that of PMOS transistor in order to compensate the mobility constraint of NMOS and PMOS transistors. Thus the proposed Design has become more efficient in terms of area, power and speed which showing better performance compare to conformist designs.

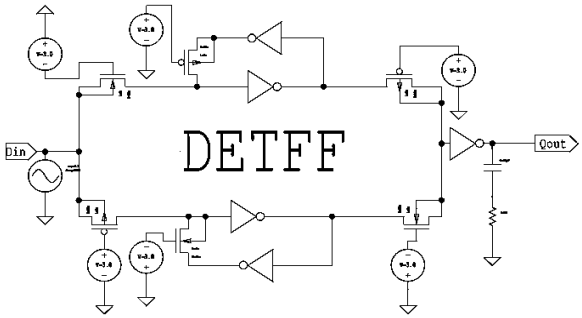


Fig 3: Proposed DETFF

IV TRANSIENTANALYSIS

To assess the performance, different flip-flop structures examine in that paper are designed using 180-nm CMOS technology. All simulations are done by using TSPICE simulation tool. Transient Analysis for Proposed circuit is absolute in fig 4:

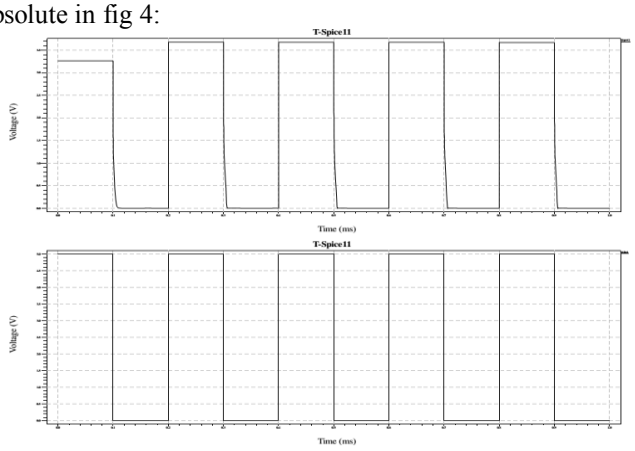


Fig 4: Output waveform for proposed DETFF

Delay Calculation**:** From the fig 4 we can calculate the delay between input and output.

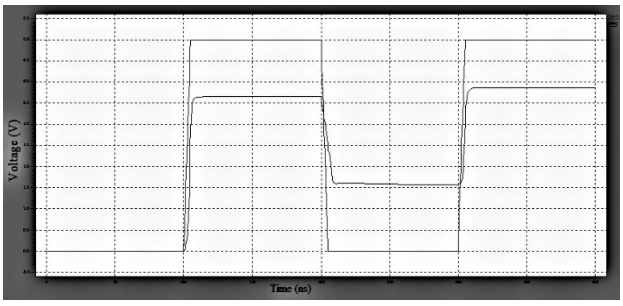


Fig 5: Output waveform showing delay between input and output

Power Calculations:For calculating power for the proposed design Power Analysis is used in Tanner EDA tool. The output simulation file gives following results:

Power Results:

- Average power consumed -> 4.500620e-006 watts
- Max power 2.736614e-005 at time 8.06113e-006

Min power 1.454874e-012 at time 3e-009 This shows that average power consumption for proposed design is 4.5 µW.

V COMPARISON OF PERFORMANCE

The performance of the proposed DETFF is calculated by comparing the average power, delay and power delay product (PDP) for DETFF1, DETFF2 and proposed DETFF. Generally, for low power portable systems a PDP-based comparison is appropriate in which the battery life is the primary index of energy efficiency.

TABLE1: Performance comparison at 1MHz

Flip Flop's	Average Power (µW)	Delay (µs)	PDP (aJ)
DETFF [1]	1.509	10.72	16.17
DETFF [2]	7.45	11.09	82.63
PROPOSED DETFF	4.5	3.49	15.705

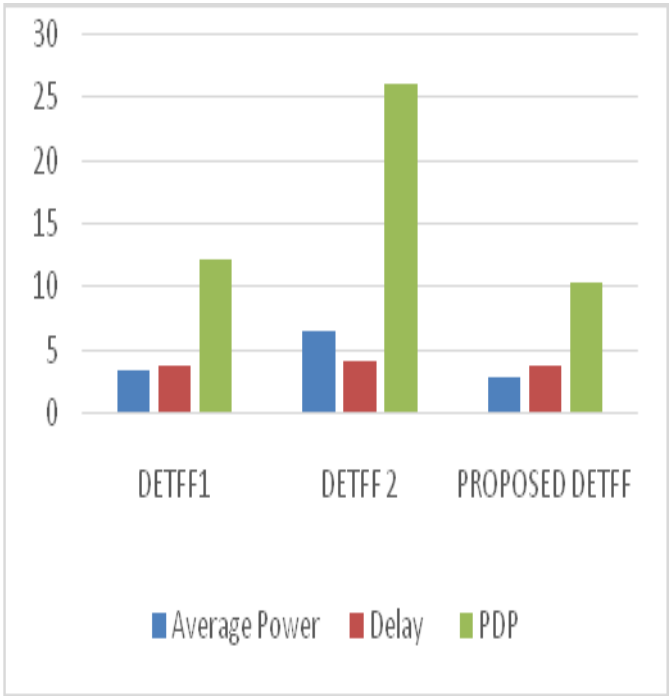


Fig6: Output Performance comparison at 1MHz

TABLE 2: Performance comparison at 10MHz

Flip Flop's	Average Power (µW)	Delay (µs)	PDP (aJ)
DETFF1	3.12	3.72	12.09
DETFF 2	6.40	4.09	26.18
PROPOSED DETFF	2.75	3.72	10.23

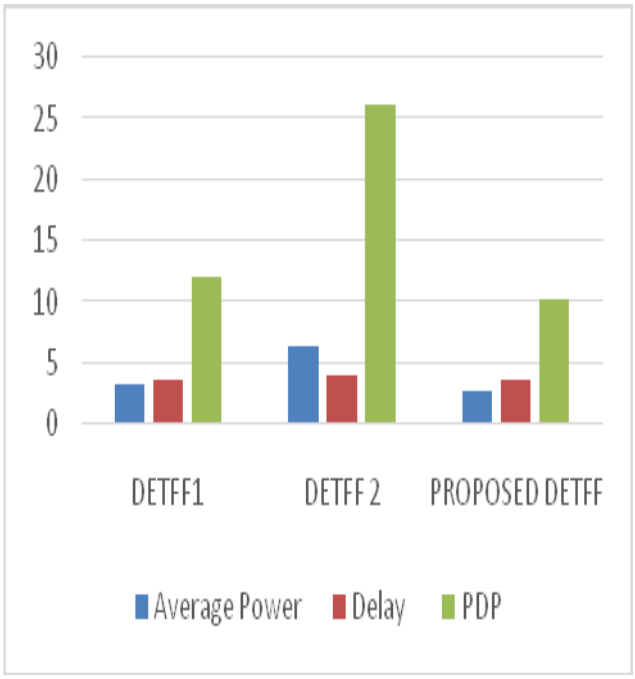


Fig7: Output Performance comparison at 10MHz

VI CONCLUSION

In that paper, the performance parameters including Power consumption, Delay and Power Delay Product are analysed and compared. The DET flip-flops are simulated with different clock frequencies ranging from 1MHz to 10GHz. Simulation results show that the proposed DETFF has improvement of 65.61% in terms of average power when compared with DETFF2. The proposed design also has an improvement of 65.61% and 25.85% in terms of power delay product (PDP) as compared to DETFF1 and DETFF2 respectively. The proposed design has minimum average power and lowest PDP than existing designs. Therefore the proposed design is suitable for low power and high performance applications.

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