"Power Reduction in CMOS Technology by using Tri-State Buffer and Clock Gating"

Renuka Jaiswal[1], Ranbir Paul[2], Vikas Ranjan Mahto[3]

M.Tech Scholar,Department of ECE,Chouksey Engg College,Bilaspur,Chhattisgarh,India[1]
Astt.Prof,Department of ECE,Chouksey Engg College,Bilaspur,Chhattisgarh,India[2]
Faculty,Department Of EEE,O P Jindal Institute of Technology,Raigarh,Chhattisgarh, India[3]

Abstract— In this research paper we have implemented different type of clock gating techniques and proposed technique to reduce power. All the techniques are performed at different technology with temperature, voltage and frequency variation and their Dynamic, static and total power has been computed, In this we are applying clock gating techniques on a 8 bit Arithmetic logical unit (ALU).here we had compared different clock gating techniques i.e with out clock gating, and gate based, latch based ,mux based ,flip flop based ,positive level sensitive latch based ,T-FF based, double gated based, negative latch based with our proposed clock gating technique.In this research paper by using tri state we are making a new design that will save more power and area.

I. INTRODUCTION

In recent years, the demand for power-sensitive designs has grown significantly. This tremendous demand has mainly been due to the fast growth of battery-operated portable applications such as notebook and laptop computers, personal digital assistants, cellular phones, and other portable communication devices. Semiconductor devices are aggressively scaled each technology generation to achieve high-performance and high integration density. Due to increased density of transistors in a die and higher frequencies of operation, the power consumption in a die is increasing every technology generation. Supply voltage is scaled to maintain the power consumption within limit.

However, scaling of supply voltage is limited by the high-performance requirement. Hence, the scaling of supply voltage only may not be sufficient to maintain the power density within limit, which is required for power-sensitive applications. Circuit technique and system-level techniques are also required along with supply voltage scaling to achieve low-power designs.

A. CLOCK SIGNALS

Clock signals are synchronizing signals that provide timing references for computation and communication in synchronous digital systems. Traditionally, the demand for high performance was addressed by increasing clock frequencies with the help of technology scaling. However, in deep sub-micron generations, the increasing trend in clock frequency has slowed down and instead higher performance is obtained by increasing parallelism at the architectural level. A very clear example of this trend is the recent move towards multi-core architectures for processors. With the continuing increase in the complexity of high-performance VLSI system-on-chip (SOC) designs, the resulting increase in power consumption has become the major obstacle to the realization of high performance designs. Such increase in the complexity of synchronous SOC systems increases the complexity of the clock network and hence increases the clock power even if the clock frequency may not scale anymore. Hence, the major fraction of the total power consumption in highly synchronous systems, such as microprocessors, is due to the clock network. In the Xeon Dual-core processor, a significant portion of the total chip power is due to the clock distribution network. Thus, innovative clocking techniques for decreasing the power consumption of the clock networks are required for future high performance and low power designs.

B. ELECTRONIC DESIGN AUTOMATION (EDA or ECAD)

It is a software tools for designing electronic systems such as printed circuit boards and integrated circuits. The tools work together in a flow and analysis required design & its outcome that connects the chip designers to work in all abstraction levels of semiconductor chip.The EDA is formally known as Engineering Design Automation which has been become a part of necessary part of the design automation tools. To reduce the design time for a system, Many EDA tools are introduced with lot of feature involve, in the market. As most important chip design parameter are Area, Power and Performance. Area is calculated at most in terms of gate count or transistor count or the final chip area including transistor and interconnects with routing conductor.

The optimization is done with the routing/placement/positioning algorithm to get the optimized results. Next is the Performance of the design it is the logic levels, gain, working frequency, temperature analysis, reliability, etc. These two can be separately deal in the each & every abstraction level of design to make it optimized. But power is the parameter which is the dependant on many factors like area, routing cost, logic implementation and many more.

Since Power is divided into two types i.e. static power (power dissipated when circuit is in OFF state), Dynamic power (power dissipated when circuit is switching from one state to another or ON state).So, power management has become a serious problem to overcome. This report deals with Power management aspects used by the EDA tools and its

ISSN: 2278 – 1323

optimization problem, which integrates with the process to device development and includes chip architects, circuit and logic designers along with EDA developer to have an automated Environment promising the optimization of power management techniques.

A spectrum of circuit techniques including transistor sizing, clock gating, multiple and dynamic supply voltage are there to reduce the dynamic power. Clock gating is one of the popular techniques for reducing clock power . The existing clock gating solutions are based on masking the local clock signal using masking logic gates (NAND/NOR) .

II. DYNAMIC POWER REDUCTION TECHNIQUES

Though the leakage power increases significantly in every generation with technology scaling, the dynamic power still continues to dominate the total power dissipation of the general purpose microprocessors. Effective circuit techniques to reduce the dynamic power consumption include transistor size and interconnect optimization, gated clock, multiple supply voltages and dynamic control of supply voltage. Incorporating the above approaches in the design of nano-scale circuits, the dynamic power dissipation can be reduced significantly. Other techniques such as instruction set optimization, memory access reduction and low complexity algorithms are also there to reduce the dynamic power dissipation in both logics and memories.

A.TRANSISTOR SIZING AND INTERCONNECT OPTIMIZATION

The best way to reduce the junction capacitance as well as the overall gate capacitance is to optimize the transistor size for a particular performance. Sizing techniques can be mainly divided into two types.

- Path-based optimization.
- Global optimization.

In path-based optimization, gates in the critical paths are upsized to achieve the desired performance, while the gates in the off critical paths are down sized to reduce power consumption.

In global optimization, all gates in a circuit are globally optimized for a given delay.

B.CLOCK GATING

Clock gating is an effective way of reducing the dynamic power dissipation in digital circuits. In a typical synchronous circuit such as the general purpose microprocessor, only a portion of the circuit is active at any given time. Hence, by shutting down the idle portion of the circuit, the unnecessary power consumption can be prevented. One of the ways to achieve this is by masking the clock that goes to the idle portion of the circuit.

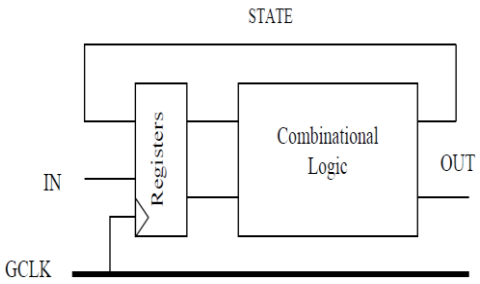

Figure 1 Single clock, flip-flop-based FSM

This prevents unnecessary switching of the inputs to the idle circuit block, reducing the dynamic power. The input to the combinational logic comes through the registers, which are usually composed of sequential elements, such as D flip-flops (Fig. 1).

A control signal (f_a) is used to selectively stop the local clock (LCLK) when the combinational block is not used. The local clock is blocked when f_a is high. The latch shown in Fig.2 is necessary to prevent any glitches in f_a from propagating to the AND gate when the global clock (GCLK) is high. The circuit operates as follows.

The signal f_a is only valid before the rising edge of the global clock. When the global clock is low, the latch is transparent, however, f_a does not affect the AND gate. If f_a is high during the low-to-high transition of the global clock, then the global clock will be blocked by the AND gate and local clock will remain at low. Power saving using gated clock technique strongly depends on the efficient synthesis and optimization of dedicated clock-stopping circuitry.

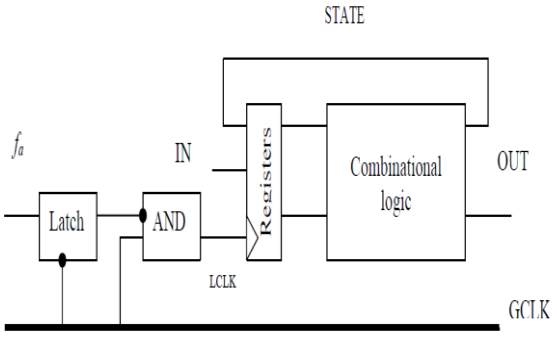

Figure 2 Schematic diagram of gated clock design

Effective clock gating requires a methodology that determines which circuits are gated, when, and for how long. Clock-gating schemes that either result in frequent toggling of the clock-gated circuit between enabled and disabled states, or apply clock gating to such small blocks that the clock-gating control circuitry is almost as large as the blocks themselves, incur large overhead. This overhead may result in power dissipation to be higher than that without clock gating.

III. PROBLEM FORMULATION

As CMOS technology scales further beyond 45 nm power management and power optimization continues to play a crucial role not just because of the stringent power budgets, but also because of reliability considerations, and of

packaging and cooling costs as well. Process technologists have the biggest role in coming up with device solutions to optimize dynamic power and, most importantly, to suppress wasteful leakage power.

A. POWER-AN EDA PERSPECTIVE

To reduce static and dynamic power a number of techniques like body biasing, power-gating, parallel processing under reduced VDD, and other creative techniques have been proposed.

It reliably reflects what was considered, at that time, the most relevant power management issues for the design community around the concurrent process technologies of the time. In addition, the literature of those dates reflects the same concentration of theoretical and algorithmic research on those identical power management topics. In the earlier dates, there was a significant lag between power management research and the release of the EDA tools because the whole concept of synthesis and design automation was still in its infancy. In fact, early literature on dynamic power estimation and on calculating dynamic power at the synthesis stage dates back to the late 1980s and early 1990s.

B. CHRONOLOGY OF EDA POWER TECHNIQUES

YEAR	NAME OF TECHNIQUE	DESCRIPTION
2006	Top-Down Multi Voltage synthesis Logical Power Domains	In this Selected functional blocks are run at different supply voltages at logical power domain. At the logic level a power domain contains: 1) A set of logic gates that correspond to the (regular) physical gates of this power domain. 2) The nets driven by these logic gates 3) A set of special gates such as level shifter cells, state retention cells, isolation cells, power switches, always-on cells, or multi-rail hard macros (such as, I/Os, memories, and so on) that correspond to the physical implementation of these gates in this power domain.
2004	Multi Vdd, MTCMOS Power network Analysis/Synthesis	In MTCMOS a high-Vth sleep transistors are used for power gating to reduce leakage power.
2003	Multi-Vth Leakage power optimization	In this multi-threshold voltage is assigned to reduce leakage. The NBTI-degradation rate varies with different initial threshold voltage assignment, and therefore motivates the co-optimizations of leakage reduction and NBTI mitigation.
2002	1-Pass leakage power optimization, Behavioral level power optimization	In this an algorithm uses device-level models for leakage to pre characterize a given register-transfer level module library. This is used to estimate the power consumption of a circuit due to leakage.

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2001	Full chip power analysis Hierarchical Rail Analysis	In this build a full-chip physical prototype early at RTL to identify problems early then achieve design closure before partitioning by optimizing die size, resolving signal integrity issues by meeting power requirements. Maintain the design closure throughout the design process
2000	Physical Clock Gating	Turn off entire block disabling all functionality by suspending clocks selectively.
1998	Dual Vth Leakage power optimization Static Rail Analysis	Basic idea is to utilize the timing slack of non-critical paths to assign high Vth to gates on those paths to decrease the leakage
1997	RTL Clock Gating	When there is no activity at a register "data" input, no need to clock the register and clock can be gated to switch it off. So power will be saved.
1996	Dynamic power optimization At RTL level	An algorithm is used to locate, a design functional unit that may perform unnecessary computation and modify it to save the dynamic power.

IV. INTRODUCTION TO CLOCK GATING

Clock power is a major component of microprocessor power mainly because the clock is fed to most of the circuit blocks in the processor, and the clock switches every cycle. Thus the total clock power is a substantial component of total microprocessor power dissipation.
Clock-gating is a well-known technique to reduce clock power. Because individual circuit usage varies within and across applications, not all the circuits are used all the time, giving rise to power reduction opportunity. By AND-ing the clock with a gate-control signal, clock-gating essentially disables the clock to a circuit whenever the circuit is not used, avoiding power dissipation due to unnecessary charging and discharging of the unused circuits. Specifically, clock-gating targets the clock power consumed in pipeline latches and dynamic-CMOS-logic circuits (e.g., integer units, floating-point units, and word-line decoders of caches) used for speed and area advantages over static logic.

Effective clock-gating, however, requires a methodology that determines which circuits are gated, when, and for how long. Clock-gating schemes that either result in frequent toggling of the clock-gated circuit between enabled and disabled states, or apply clock-gating to such small blocks that the clock-gating control circuitry is almost as large as the blocks themselves, incur large overhead. This overhead may result in power dissipation to be higher than that without clock-gating.

A. *NEW APPROACH FOR CLOCK GATING*

Our Research introduces a new design that will save more power and area. The new Gated Clock Generation Circuit is shown in below figure using tri state buffer and NAND gate with bubbled input respectively. This circuit saves power in such a way that even when Target device's clock is ON, the controlling device's clock is OFF and also when the target device's clock is OFF then also Controlling device's clock is OFF. This way we can save more power by avoiding unnecessary switching at clock net .

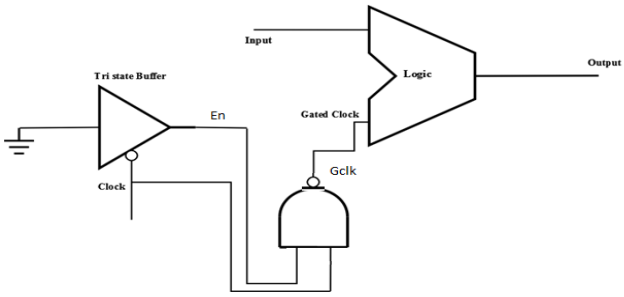
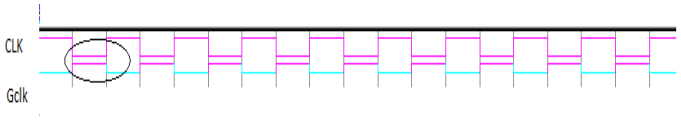


Figure: Clock gating based on TRI state buffer



To understand the working of circuit , an input signal named Clk is provided to the NAND and tri-state buffer. When clk turns to '1' at that time En output is '0' , and NAND gate with negedge clock will produce output ='1' which goes to the first clock generation logic that generates clock for controlling device. In first logic we have an TRI gate which have Global Clock as an input at the other input of ground. This logic will generate a clock pulse that will drive the controlling latch when 'x' turns to '1'.In the next clock pulse, when CLK turns to '0' our second clock generation logic which is an NAND gate which has EN and Global clk at its input and when Gen goes '1' it generates clock pulse that goes to the target device. Since GEN is '1' the NAND will produce '1' thus OR will produce at CClk constant HIGH until En turns to '0'. This

way GClk will be running and CClk will be at Constant '1' state that means latch will hold its state without any switching.

B. PROPOSED CLOCK GATING

Table 1: Comparison of power for Proposed Tristate Buffer clock gating technique with voltage variation

Voltage	90nm Technology			65nm Technology			45nm Technology		
	Dynamic	Static	Total	Dynamic	Static	Total	Dynamic	Static	Total
1.14	0.072	0.027	0.098	0.204	0.026	0.204	0.202	0.015	0.207
1.2	0.073	0.028	0.101	0.213	0.033	0.243	0.204	0.019	0.222
1.26	0.075	0.029	0.104	0.214	0.096	0.310	0.206	0.019	0.226

Table 2: Comparison of power for Proposed Tristate Buffer clock gating technique with frequency variation

Frequency	90nm Technology			65nm Technology			45nm Technology		
	Dynamic	Static	Total	Dynamic	Static	Total	Dynamic	Static	Total
10G Hz	1.312	0.034	1.346	1.690	0.0339	2.029	2.011	0.056	2.017
7G Hz	0.812	0.031	0.695	1.045	0.0248	1.023	1.346	0.049	1.015
5G Hz	0.664	0.030	0.694	1.026	0.256	1.281	1.013	0.038	1.051

Table 3: Comparison of power for negative latch based clock gating technique with temperature variation

Temperature	90nm Technology			65nm Technology			45nm Technology		
	Dynamic	Static	Total	Dynamic	Static	Total	Dynamic	Static	Total
25	0.072	0.027	0.098	0.209	0.206	0.415	0.206	0.019	0.225
50	0.073	0.031	0.104	0.209	0.205	0.464	0.209	0.029	0.208
75	0.073	0.035	0.108	0.209	0.316	0.525	0.209	0.055	0.263

C. COMPARISION GRAPH OF DIFFERENT CLOCK GATING TECHNIQUES

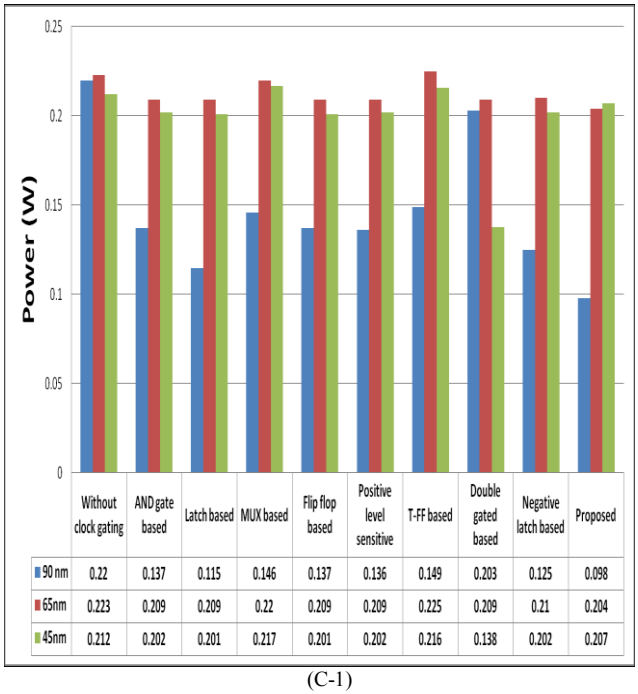
C-1 (REFER PAGE 6) Comparison of dynamic power for various clock gating techniques at different technologies operating at 1.14 voltage

C-2 (REFER PAGE 6) Comparison of dynamic power for various clock gating techniques at different technologies operating at 1.2 voltages

C-3 (REFER PAGE 6) Comparison of dynamic power for various clock gating techniques at different technologies operating at 1.26 voltage

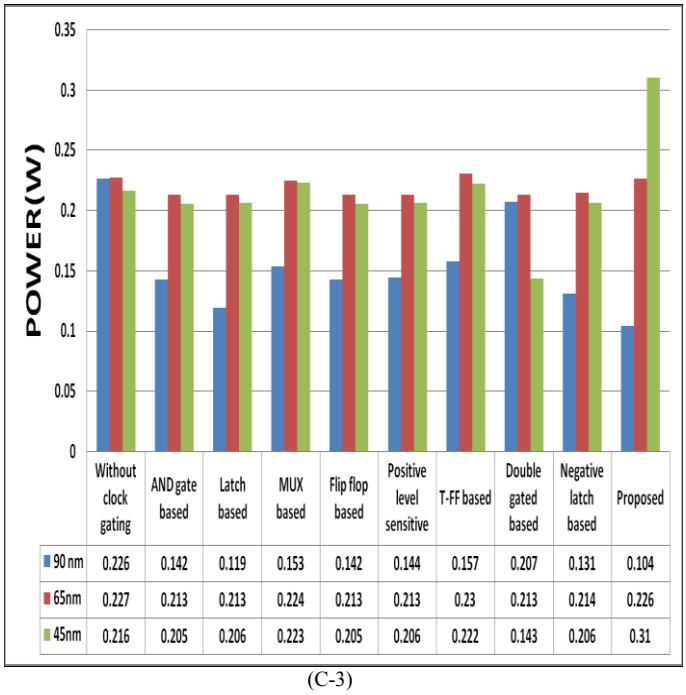
C-4 (REFER PAGE 6) Comparison of dynamic power for various clock gating techniques at different technologies operating at 10GHz frequency

ISSN: 2278 – 1323



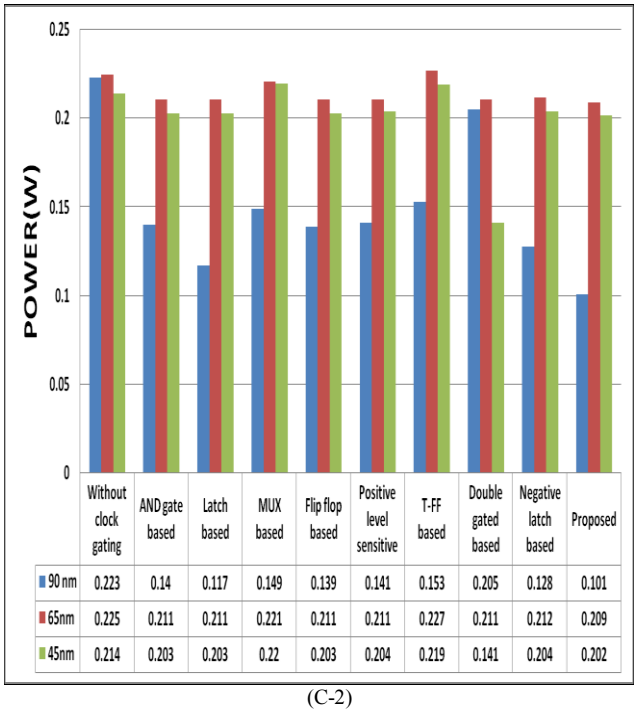
	Without clock gating	AND gate based	Latch based	MUX based	Flip flop based	Positive level sensitive	T-FF based	Double gated based	Negative latch based	Proposed
90 nm	0.22	0.137	0.115	0.146	0.137	0.136	0.149	0.203	0.125	0.098
65nm	0.223	0.209	0.209	0.22	0.209	0.209	0.225	0.209	0.21	0.204
45nm	0.212	0.202	0.201	0.217	0.201	0.202	0.216	0.138	0.202	0.207

(C-1)



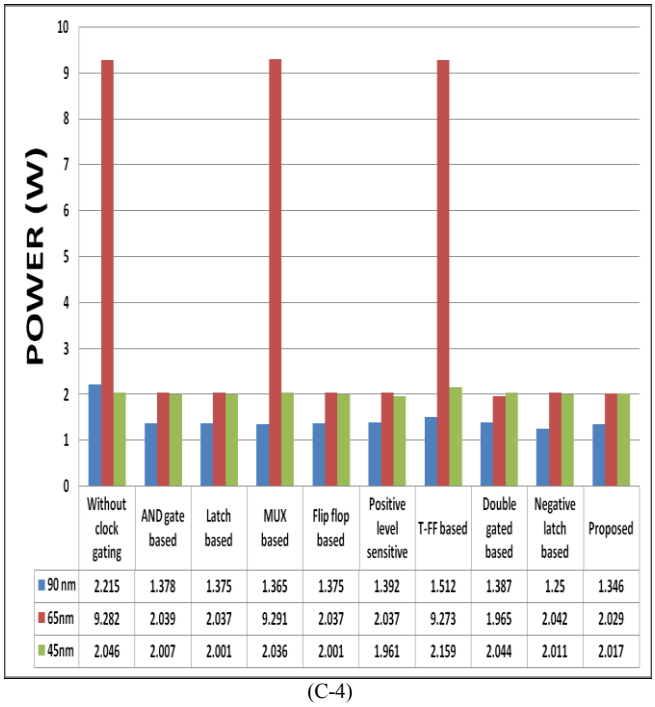
	Without clock gating	AND gate based	Latch based	MUX based	Flip flop based	Positive level sensitive	T-FF based	Double gated based	Negative latch based	Proposed
90 nm	0.226	0.142	0.119	0.153	0.142	0.144	0.157	0.207	0.131	0.104
65nm	0.227	0.213	0.213	0.224	0.213	0.213	0.23	0.213	0.214	0.226
45nm	0.216	0.205	0.206	0.223	0.205	0.206	0.222	0.143	0.206	0.31

(C-3)



	Without clock gating	AND gate based	Latch based	MUX based	Flip flop based	Positive level sensitive	T-FF based	Double gated based	Negative latch based	Proposed
90 nm	0.223	0.14	0.117	0.149	0.139	0.141	0.153	0.205	0.128	0.101
65nm	0.225	0.211	0.211	0.221	0.211	0.211	0.227	0.211	0.212	0.209
45nm	0.214	0.203	0.203	0.22	0.203	0.204	0.219	0.141	0.204	0.202

(C-2)



	Without clock gating	AND gate based	Latch based	MUX based	Flip flop based	Positive level sensitive	T-FF based	Double gated based	Negative latch based	Proposed
90 nm	2.215	1.378	1.375	1.365	1.375	1.392	1.512	1.387	1.25	1.346
65nm	9.282	2.039	2.037	9.291	2.037	2.037	9.273	1.965	2.042	2.029
45nm	2.046	2.007	2.001	2.036	2.001	1.961	2.159	2.044	2.011	2.017

(C-4)

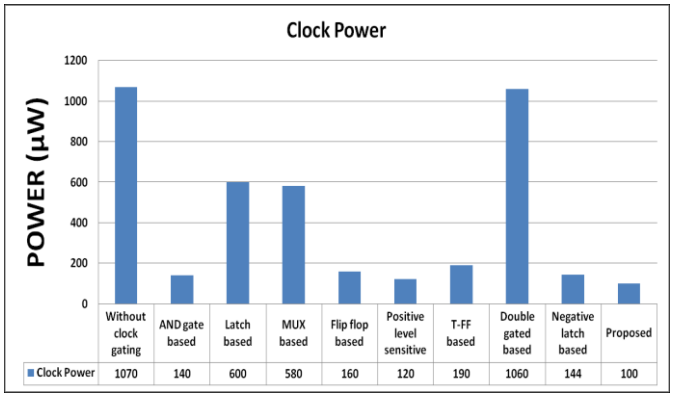
V. CONCLUSIONS

In this research finally we have a new design that will save more power and area.. This circuit saves power in such a way that even when Target device's clock is ON, the controlling device's clock is OFF and also when the target device's clock is OFF then also Controlling device's clock is OFF. This way we can save more power by avoiding unnecessary switching at clock net.

The key contribution of this thesis is to develop a new clock gating technique with low area overhead and improved performance of the digital circuit. The increase in dynamic power consumption makes the system unreliable, so to

control the dynamic switching power various techniques are studied and analyzed to reduce it. A New tri state based clock gating technique is proposed with low area overhead. Comparative analysis shows that the proposed technique impacts on the dynamic power reducing up to 3 folds in compare to conventional one. All the analysis are done on a 8 bit ALU with process variation parameters.

In our technique the clock power has been reduced to 100 µw where as the different power of different clock gating techniques are as follows:-



Hence it can be concluded from this research that the clock power in our technique is least as compared to other different clock gating techniques.

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AUTHOR DETAILS

Renuka Jaiswal[1]

Renuka Jaiswal received the undergraduate degree in Electronics & Communication with honours from Dr C V Raman University Bilaspur ,Chhattisgarh, India and Pursuing her Master's degree in Digital Electronics from the Chouksey Engineering College,Bilaspur,India.

Ranbir Paul[2]

Ranbir Paul received his graduate & post graduate degree in Electronics & Communication.Presently he is working as Asst.Prof in Chouksey Engineering College Bilaspur.

Vikas Ranjan Mahto[3]

Vikas Ranjan Mahto received the undergraduate degree in Electrical Engineering from MPCCET Bhilai.He has served in the different organizations & Academic Institutions like JKIE,LCIT,Spectrum Coal & Power Ltd,Dr C V Raman University Bilaspur,CREW(P)Ltd,BALIC etc.

Presenrly he is working as Faculty of Electrical & Electronics Engineering Deptt in O P Jindal Institute of Technology Raigarh.
His Prime area of Research is "Computational Applications of Electrical Machines."

