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Low-Power VLSI Implementation in Image Processing using Programmable CNN

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Abstract

The low power CMOS implementation is based on a combination of MOS transistors operating in di erent modes: weak and strong-inversion. We propose, MOS transistors operating in the lateral bipolar mode.This combination has enabled a VLSI implementation of a simpli ed version of the original CNN model with the main characteristics of low-power consumption, program-mability, and embedded photo sensors to process images directly projected on the chip. For VLSI implementations of CNN's .It is usual to consider simpli ed versions of the Chua-Yang model in order to reduce circuit com-plexity.Several applications of CNN's in solving image processing tasks such as noise removal, edge and corner detection, hole lling, connected component detection, etc. To obtain low-power consumption and to directly process the small currents from the sensors we use MOS transistors operating in weak inversion for all the di erential pairs .in such a way that only local matching between transistors belonging to each di erential pair is required. Due to their better matching properties, MOS transistors operated in the lateral bipolar mode are used for the distribution of the values de ning the programmable parameters (templates A and B, and the o set I), as well as the values that limit the range of the cell output and input. As in other CNN implementations integrated photo sensors are used to allow a parallel and direct input of the images to be processed by the network. The approach considered in and uses a Darlington phototran-sistor in order to provide the appropriate current levels required by the MOS circuitry operating in strong inver-sion. Software proposed to be used is MATlab and VHDL.

Keywords: VHDL, MATLAB, Verilog.

I. Introduction

The cellular neural network (CNN) as proposed by Chua and Yang, is a special type of analog nonlinear processor array. Due to their continuous-time dynamics and parallel processing features, analog CNN circuits are very e ective in real time. image processing applications such as noise removal, edge detection and feature extraction . The regularity, the parallelism and the local connectivity found in CNN circuit architecture make it suitable for VLSI implementations. Motivated by the above facts we have implemented the CNN structure using analog CMOS circuits. One of our major goals is the design simplicity. To achieve this goal, the design is reduced to the design of few type of CMOS trans-conductance elements . One can easily adapt this realization to various types of applications by just choosing the appropriate trans-conductance parameters according to the predetermined coupling coe cients between the neighboring cells. The coe cients may be either chosen according to a computer simulation or chosen based on the prominent kernels for image processing . Another important motivation for using CMOS trans-conductance elements in the require-ment of adaptability. In order to achieve programmable coupling coe cients, the trans-conductance parameters are adjustable with extreme voltage sources. In the implementation of xed function CNNs that performs one or a related set of processing function using xed coe cients, the number of transistors is reduced further by merging appropriate transistors in the multi-input trans-conductance sub-circuit as explained in Section .

II. Background Behind the Project

Models of neural networks are receiving widespread attention as potential new architectures for computing systems. The models we consider here consist of highly interconnected networks of simple computing elements. A computation is per- formed collectively by the whole network with the activity distributed over all the com-puting elements. This collective operation results in a high degree of parallel computation and gives the network the potential to solve complex problems quickly. Neural network models have demonstrated functions such as associative memory, adaptive learning from examples, and combinatorial optimization. Several applications of CNNs in solving image processing tasks such as noise removal, edge and corner detection, hole lling, connected component detection, etc., have been reported in several publications . Various analog VLSI implementations of CNN building blocks have been previously implemented and tested which can serve to build CNNs under di erent constraints concerning the size of the network, the kind of cell input and state (analog/digital), the power consumption, and the programmability features of the network. CNN circuits to perform specic processing tasks allow more compact VLSI implementations. Pro-grammable CNN circuits can either be used to perform di erent specic tasks on the input images, or they can be

sequentially congured to carry out compatible successive tasks.

II(a). Analog CMOS Realization of The Cell Circuit

Because of its simplicity, the CMOS trans-conductance element is chosen as the basic building block for the integrated realization of the CNN cell circuit . The linear CMOS trans-conductance element (voltage-to-current transducer) resembles in most respects that of the CMOS inverter but without the matching problems between PMOS and NMOS transistors and with the additional advantage of tunability . The transistor schematic and the input-output characteristic of this four-transistor trans-conductance element is shown in Fig. 1. It can be easily proven that when all transistors operate in their saturation region , the output current I0 =Ia-Ib equals

$$Iout = -gm + Lo$$

$$gm =2ke [Vg1+ Vg4 - (Vtn1 + Vtn3 + mod(VTp3) + mod(VTp4)] Io =gm/2[(Vtn3-Vtn1)+mod(Vtp4)-mod(Vtp2)+(Vg1-Vg4)]$$

are introduced for the trans-conductance Parameter and the o set current, respectively. Although the o - set current I,,E is not equal to zero due to the body e ect, it can be easily eliminated by an appropriate set-ting of I Ht in an n-well process and IhI in a p-well process

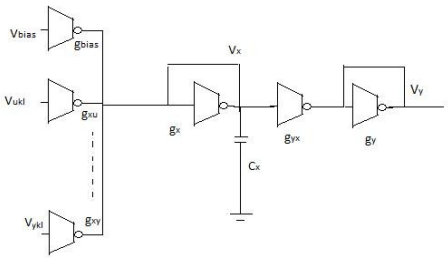

Figure 1: The cell-circuit realization with CMOS trans-ducers

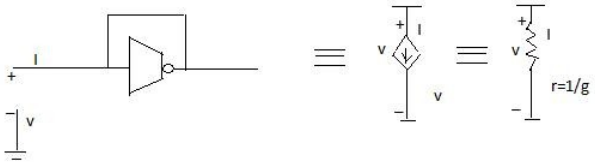

Figure 2: The circuit diagram

II(b). Schematic block diagram of a CNN cell

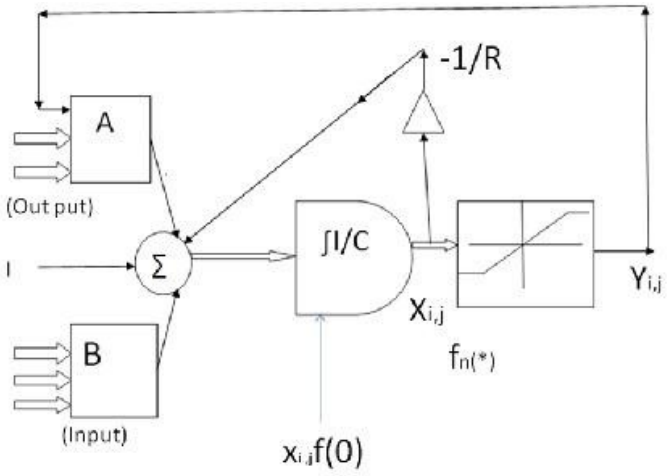

Figure 3: Schematic block diagram of a CNN cell

III. CMOS Implementation of The CNN Cells

Fig. shows a block diagram for the CNN cell model here considered. It includes a lossy integrator that has as inputs weighted contributions of the outputs and inputs of the set of m cells in a neighborhood of cell c. The basic di erence with respect to the original Chua-Yang model is the loss term, which depends on the cell output yc instead of on the internal cell state xc.2 Morever, a sigmoid-like function, instead of the conventional piecewise-linear function, is used to generate the cell output. Fig. 2 shows the proposed circuit implementation. As will be proved below in this section, the state equation of the cell c, belonging to a CNN with M rows and N columns, implemented by the circuit of Fig. 2 is

$$C(dVxc/dt)=-Iyc+Igc$$
$$= -Iyc(t)+$$
$$X$$
$$SA(n\ c)\ IA(n\ c)Iyn(t)=IL$$
$$+$$
$$X$$
$$SBn\ c\ IBn\ c\ (Iun\ IL=ILb)=IL + I$$

$$Iyc=IL*tanh[k(Vxc-VR/2UT)$$
$$1\ c\ MN; nNR(c);$$
$$IL\ \$\ h\$A0 : Iyn(t); IunIL[IL + IL]=ILB$$

where n denotes a generic cell belonging to the neigh-borhood NR(C) of cell C, with radius equal to R. In the present implementation a neighborhood of 3 *3 cells centred on c has been considered, i.e.

N1(c) = C-N-1,C-N,C-N+1,C-1,C,C+1,C+N-1,C+N,C+N+1

Vxc represents the state xc of the cell c; Iyc and Iuc represent the output yc and the input uc, respectively, of cell c; Il is a current that limits the cell output Iyc, and Ilb is a current limiting the input Iuc. The current I corresponds to the o set term, and its value, added to Il, is set by the external voltage VL1; Igc is the total current contribution of the neighborhood plus the o set term This simpli ed model is a particularization of the CNN model formalized. The VLSI implementations described in can also be identi ed as particular cases of such a model.

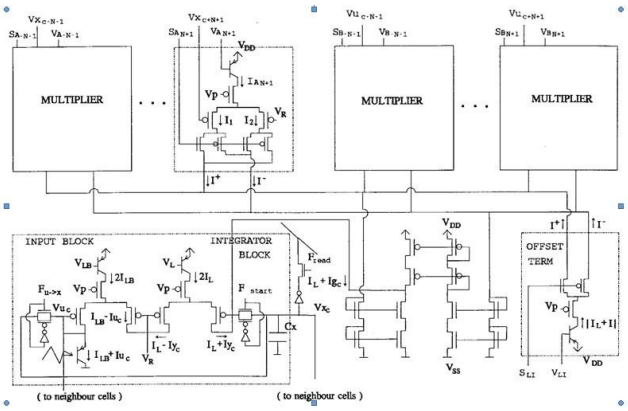

Figure 4: Circuits to implement the building blocks

of the feedback template A, obtained from the common external voltage VA . Other components of the feedback template and the components of the control template (B) are applied and multiplied in a similar way. Observe that the notation used for the templates re ects the fact that they are space invariant.

To obtain low-power consumption and to directly process the small currents from the sensors we use MOS tran-sistors operating in weak inversion for all the di erential pairs in Fig. , in such a way that only local matching between transistors belonging to each di erential pair is required. However, due to their better matching prop-erties, MOS transistors operated in the lateral bipolar mode are used for the distribution of the values de ning the programmable parameters (templates A and B, and the o set I), as well as the values that limit the range of the cell output and input. The cascade connected PMOS transistors biased by V p in Fig. 2, have been added to reduce the e ect of the low Early voltage of the lateral bipolar transistors Therefore, while working with current levels comparable to those in weak-inversion, the values of externally set parameters are better matched at least for the cells in a neighborhood. The MOS transistors implementing the current mirrors in Fig. 2 operate gen-erally in strong-inversion. They collect the outputs from all the multipliers and the current representing the o set term. As in other CNN implementations integrated photo sensors are used to allow a parallel and direct input of the images to be processed by the network. The approach considered in and uses a Darlington phototransistor in order to provide the appropriate current levels required by the MOS circuitry operating in strong inversion. We use a single bipolar phototransistor (of 30 2 30 m2 in the experimental prototype), which provides currents of between tens and hundreds of nano amperes under normal laboratory conditions.

Di erent cells communicate by voltage signals instead of currents and, without any explicit conversion, are processed as currents by the multipliers of neighbor cells. The total capacitance Cx used for integration at the output node of each cell is formed by the gate capacitance of transistors of the neighbor cells, in such a way that the capacitances of the remaining nodes are negligible compared with those used for integration. To build a whole CNN, instead of using multipliers or current sources to implement the border cells as is usually required, only the corresponding explicit capacitance must be added to the peripheral cells.

III(a). CMOS Image Sensors

The greatest promise of CMOS image sensor technology arises from the ability to exibly integrate sensing and processing on the same chip to address the needs of di erent applications. As CMOS technology scales, it becomes increasingly feasible to integrate all basic camera functions onto a camera-on-chip, enabling applications requiring very small form-factor and ultra-low power consumption.

III(b). Photodetection

The most popular types of photodetectors used in image sen-sors are the reverse-biased positive-negative (PN) junction photodiode and the P+/N/P pinned diode (see Figure 5). The structure of the pinned diode provides improved photo-responsively (typically with enhanced sensitivity at shorter wave- lengths) relative to the standard PN junction . Moreover, the pinned diode exhibits lower thermal noise due to the pas- sivation of defect and surface states at the Si/SiO2 interface as well as a customizable photodiode capacitance via the charge transfer operation through transistor TX. However, imagers incorporating pinned diodes are susceptible to incomplete charge transfer, especially at lower operating voltages causing ghosting artifacts to appear in video-rate applications.

photocurrent in a photodetector lies as a function of wave- length (typically in the 400700 nm range of visible light). It is typically combined with the transmittance of each color l- ter to determine its overall spectral response. The spectral response for a typical CMOS color image sensor fabricated in a modi ed 0.18-m process is shown in Figure 6. External QE can be expressed

as the product of inter- nal QE and optical e ciency (OE). Inter- nal QE is the fraction of photons incident on the photodetector surface that con- tributes to the photocurrent. It is a func- tion mainly of photodetector geometry and doping concentrations and is always less than one for the above silicon pho- todetectors. OE is the photon-to-photon e ciency from the pixel surface to the photodetectors surface. The geometric arrangement of the photodetector with respect to other elements of the pixel structure, i.e., shape and size of the aper-ture;length of the dielectric tunnel; and position, shape, and size of the pho- todetector, all determine OE.

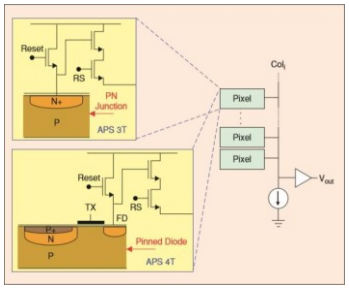

Figure 5: The Schematic of 3-and 4- T Active Pixel Sen-sors

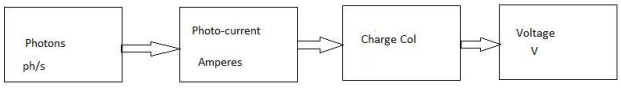

Figure 6: A block diagram of a path of image sensor

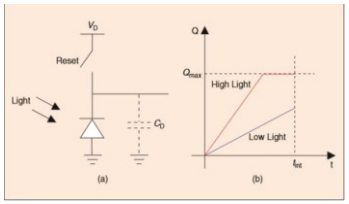

Figure 7: (a)A schematic of pixel operating in direct inte-gration,(b)Charge versus time for two photo-current val-ues

increases or decreases, due to the current jIgcj 0 IL, until it attains a value near VDD or VSS, respectively. This behavior should be taken into account for applications in which the cell outputs have to reach several times their limit values during the network evolution, as, for example, in a CCD (Table I, Section III). This fact has an observable in uence on the time response of the network but, as con rmed by simulation and experimentally, does not a ect its functionality. For these applications VR may be set to (VDD + VSS)=2, in that the cell states tend toward their two nal limit values or leave these two values at a similar rate.

III(c). Multiplier

In order to reduce the area, the required four-quadrant multipliers are implemented with two-quadrant ones together with switches controlled by the sign bit S of the corresponding programmable parameter. The output current for each multiplier can be derived by applying the translinear principle For the multiplier of the template component AN+1 (see Fig. 2), the following output current is obtained

(I+ -I-)AN+1=SAN+1(I1-I2)
=SAN+1(IAN+1/IL)*Iyc+N+1 .....(4) (I+-
I-)BN+1=SBN+1IBN+1(Iuc+N+1/ILB)
=SBN+1*(IBN+1/IL)(Iuc+N+1*IL/ILB)...(5)

Similar expressions are obtained for other components of the feedback template. The multiplier of a component of the control template, such as the BN+1, produces the output current.The currents IL and ILB can have the same value, but since the second one is used to limit the photosensor current (to 2ILB), it has been considered as a di erent parameter in order to independently adapt its value to the mean illumination level.

O set Term

(I+ - I)o set = SLI kI + ILk = I + IL::(6) The output current of the o set-term block in Fig. 2 is

IV. Simulation And Experimen-tal Results

A test chip with 8- 2 8 CNN cells based on the cir-cuits in Fig. 2 has been designed and integrated. An integration density of 10.7 cells per square millimeter has been obtained with 11 programmable parameters implemented in each cell (nine feedback parameters, one control parameter, B0, and the o set term I), using the 1.2 m CMOS-CAE process of AMS. The chip core is covered, except on the sensor areas, by the second metal layer, which is used to distribute the bias voltage VR. The integrated prototype has been successfully tested in di erent image processing tasks. Some examples are given in Table I, which shows the inputs captured by the sensors in the 8 2 8 CNN and the outputs measured from the network for three di erent tasks. Noise removal is applied as a prior step to each of these tasks. The gures included in the table are screen hard-copies from a PC with a data acquisition board used to read the signals from the chip onto which the input image is being projected. The power consumption per cell can easily be estimated in terms of the total number of current

units for a given template con guration . In practice, an increase is observed due to the vertical leakage current of the lateral bipolar transistors. With VDD = 5 V, a power consumption of between a few and tens of microwatts per cell is measured (depending on the network con guration) for unit currents ranging from 50 to 200 nA (12 W for a CCD with a current unit IL = 150 nA, 16 W for a border extraction with IL = 200 nA). The time required by the network to reach its nal state is also dependent on the speci c processing task. Measured response times are between a few microseconds and a few hundreds of microseconds for the above mentioned unit current range. The worst-case times correspond to tasks in which several cell state transitions take place before the nal output is obtained (as for example in the CCD, for which a time of about 150 s is required using a unit current of 150 nA, while a border extraction takes 6 s with IL = 20

Image Loading

Figure 8: Image Loading

Border Extraction in Image Processing

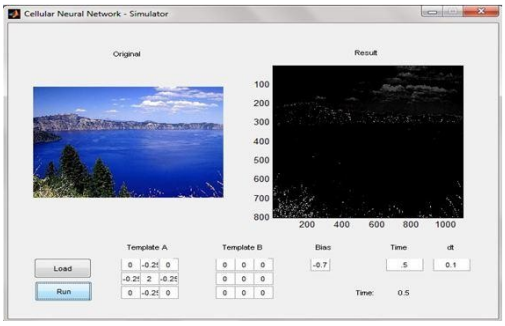

Figure 9: Border Extraction

Component Detection in Image Processing

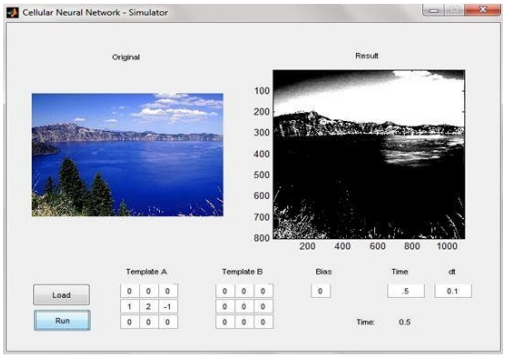

Figure 10: Component Detection

Shadow Creation in Image Processing

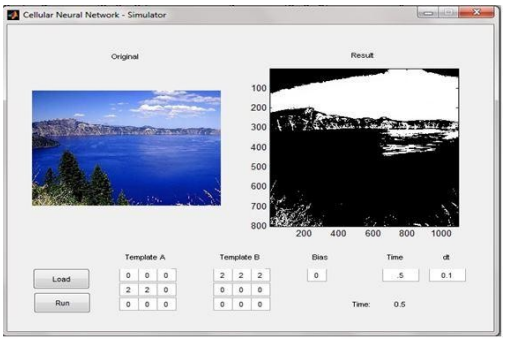

Figure 11: Shadow Creation

RTL Viewer on Quartus

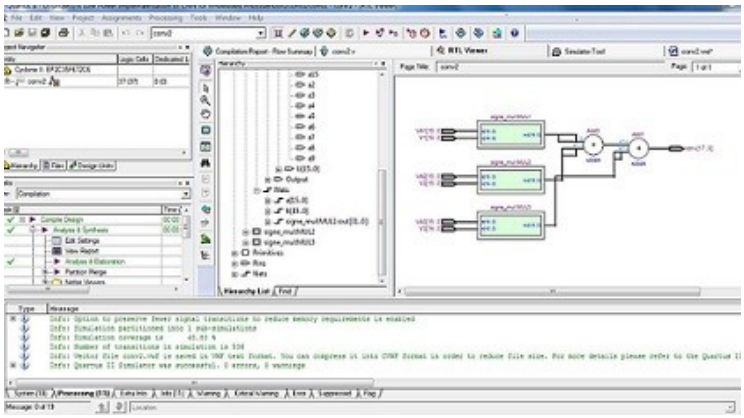

Figure 12: RTL Viewer

d) Lateral bipolar transistors are used to distribute the programmable parameters and the current units in order to reduce the e ect of process parameter variations between neighbor cells.

A CNN prototype has been designed, integrated, and successfully tested for di erent image processing tasks. Using a 1.2- m CMOS process an integration density of 10.7 cells per square millimeter is obtained. The lateral bipolar transistors occupy a 25The focal plane approach adopted here, given the resulting cell density, is useful
to implement single-chip CNN's capable of processing relatively simple images, for example written characters. To process complex images, several CNN chips (without sensors) may be interconnected directly, provided an appropriate I/O scheme and bu ering are used. In this case, a trimming phase would be required in order to match the lateral bipolar transistors between di erent chips by means of the bias voltages of their gate terminal

V. Conclusion

An analog CMOS implementation of a CNN has been presented, with the following features: 1) Embedded image sensors for direct capturing of input images, thus exploiting the potential advantage of CNN's for parallel image processing. 2) Low-current operation, which allows the use of small photo sensors and reduces power consumption. 3) The parameters de ning the processing task the CNN is to carry out are modi able by means of external signals, which enable di erent processing tasks to be performed on the same or di erent input images.

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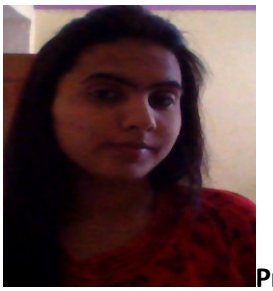

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