Implementation on combined CIC filter and 64 taps using compensation Filter in mat lab

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***Abstract*: This paper describes design and FPGA implementation of integrated CIC filter architectures, with applications in 64 taps for compensation filter. And comparing these up sampling and down sampling for simulation result, using some parameters like resource utilization and performance. The CIC filter architectures are modeled using Verilog HDL to verify the correct operation. The programmable logic synthesis and simulation were performed using the tools provided by Xilinx Inc. (ISE 12.2 and Modelsim6.3c) with a Virtex-4 as target device. However, designing CICcompensating filters for sample rate conversion systems.**

Index terms: CIC FILTER, FPGA, COMPENSATION FILTER.

I.INTRODUCTION

The Cascaded integrator comb filters do not require any multiplier circuits and hence are very economical for implementation in hardware and the problems with cascading faced by the accumulate .A functional model of the CIC compensation filter is developed using the MATLAB program. A CIC filter consists of an equal number of stages of ideal integrator filters and comb filters. when the number of stages is large and different rate change factor because its highly symmetric structure of a integrated CIC filter allows efficient implementation in hardware; CIC filter frequency response have a narrow band and does not have wide, flat pass band. To overcome the magnitude droop, a CIC filter that has a magnitude response that is the inverse of the FIR filter can be applied to achieve frequency response correction. Such filters are called "compensation filters".where the sampling rate must be change, CIC filter are utilized to increase or decrease the sampling rate. Up-sampler and down sampler are used to change the sampling rate of digital signal in multi rate DSP systems.This rate conversion need to production of undesired signals associated with aliasing and imaging errors. The appropriate number of cascaded integrator and comb filter pairs by frequency response may be tuned selected.

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II.RELATED WORK

Cascaded integrator comb [1], are filters used for realizing large sample rate and number stages changes in digital systems. CIC filters are consisting of only adders and a delay element without multipler used hence its filter great popular. It is a great advantage when aiming at low power consumption. So the multirate filters are frequently used in digital down converter and digital up converters. CIC filter is that is passband is not flat, This problem can be overcome through the use of compensation filter. Cascaded integrator-comb (CIC) digital filters are computationally efficient implementations of narrowband lowpass filters and are often embedded in hardware implementations of decimation and interpolation in modern communications systems[1].

The role of a multi rate filter and Signal Processing for Communicating Systems in Decimation and Interpolation is to suppress aliasing, and to remove imaging respectively. the performance of the system for sampling rate conversion depends mainly by filter characteristics. since an ideal frequency response is not achievable, the choice of an appropriate specification is the first step in designing a proper filter for Decimation and Interpolation filters, and for multirate filters, additional efficiency may be achieved by cascading several stages, each of them consisting of a sub-filter and down-sampler for Decimation and an up-sampler and sub filter for Interpolation. The efficiency of multi rate filters is greatly improved by simplifying arithmetic operations. This is achieved by without a multiplier with a small number of shifters-and-adder. Multirate signal processing refers to systems which allow sequences which arise from different sampling rates to be processed together[2].

Sample rate conversion (SRC) is the process of changing the sampling rate of a data stream from a specific sampling rate (e.g. the input/output hardware rate) to another sampling rate (e.g. the application rate).. Most high quality SRCs currently available on the market employ a digital filter that provides the required quality by up-sampling the data to a very high sampling rate followed by down-sampling to the required output sampling rate. The digital filters have also emerged as a strong option for removing noise, shaping spectrum, and minimizing intersymbol interference in communication architectures.The Cascaded Integrator Comb (CIC) filter is a digital filter which is employed for multiplier-less realization[3].

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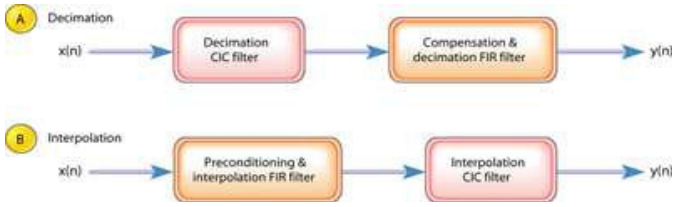
III.COMPESENATE FILTER



Fig(a): CIC COMPESENATE FILTER

CIC filters are well-suited for antialiasing filtering prior to decimation as shown in Figure 1a and for anti-imaging filtering for interpolated signals as in Figure 1b. Both CIC filter applications are very high—data-rate filtering, such as hardware quadrature modulation and demodulation in modern wireless systems and delta-sigma A/D and D/A converters. Because their frequency-magnitude-response envelopes are $\sin(x)/x$-like, CIC compesenate filters are typically either followed or preceded by higher performance linear-phase lowpass tapped-delay-line FIR filters whose tasks are to compensate for the CIC filter's non-flat passband. That cascaded-filter architecture has valuable benefits. For example, with decimation, you can reduce computational complexity of narrowband lowpass filtering compared with if you'd used a single lowpass finite impulse response (FIR) filter. In addition, its operates at reduced clock rates minimizing power consumption in high-speed hardware applications.

IV.PROPOSED WORK

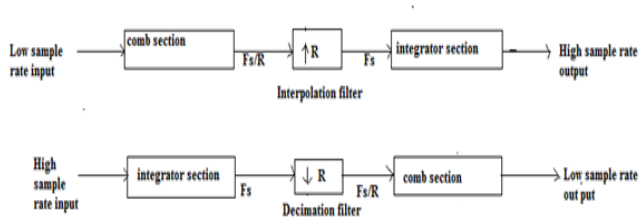


Fig (b): combined interpolation filter and decimation filter(multi rate filter)

Figure1 shows, Up sampling by a factor R is the process of inserting R-1 zero valued samples between original samples in order to increase the sampling frequency. The output sample rate or frequency increases by a factor R. Upsampling by R adds to the original signal R-1 undesired spectral images which are centered at multiples of the original sampling rate. insert sampling rate used when a narrowband signal will be combined with a signal that requires a higher sampling rate . low sampling rate or frequency input to comb section in decreases frequency Fs/R.finally increased frequency goes to integrator section. To get output High sampling frequency or rate. Down sampling by a factor R is a process where every R_{th} sample is retained while the R-1 samples in between are discarded. The output sample rate hence decreases by a factor of R. Decimation is a process where anti-aliasing filtering precedes the downsampling process. high sampling rate or frequency input to integrator section in increases frequency Fs.it depends only on rate change decimation factor R,hence frequency reduced factor Fs/R.finally reduced frequency goes to comb section. It is delay version signal to get output lower sampling frequency or rate.

V.IMPLEMENTATION AND RESULTS

Simulation Results:

- From the above results it can be seen that all the results are triggered at positive edge of clock pulse. when neg edge reset='0', all the outputs are zeros.
- When reset = 0. At that time nd is update value of signal is 1. If 8 bit valued counter from '00000000' to '00000011' then count increments up to three clock phase, counter increments by one, interpolator filter operation performed. Positive edge pulse rdy operation is done. Finally interpolator filter output obtained.
- When neg edge reset = 1. If 8 bit valued counter from '00000000' to '00000011' then count increments up to three clock phase, counter increments by one, decimator operation performed. Finally interpolator filter CIC_output1 goes to decimation filte.Positive edge pulse rdy operation is done. Finally decimator output goes to CIC filter output performed.
- The combined simulated results are obtained as per requirements. obtained. Some of the simulation results of the decimator are shown in the following figures.

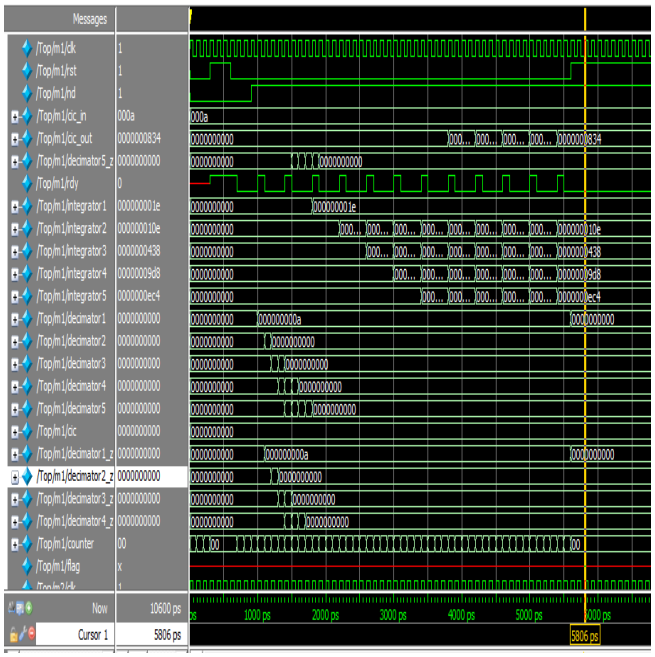


Fig (c) :Simulation interpolator

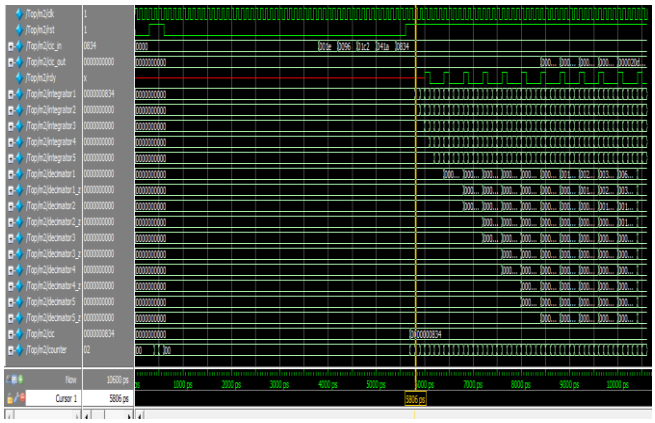


Fig (d) :Simulation on decimation

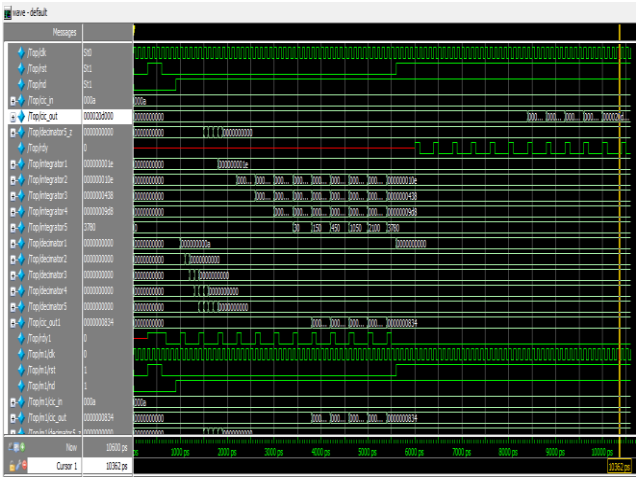


Fig (e) :Simulation of combined multirate filter

Table 1: Design summary on CIC combined filter
Device utilization summary for CIC combined filter
Number of stages = 5, down sampling rate = 2. And
Differential delay =1ns.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	1,689	10,944	15%
Number of 4 input LUTs	799	10,944	7%
Number of occupied Slices	1,108	5,472	20%
Number of Slices containing only related logic	1,108	1,108	100%
Number of Slices containing unrelated logic	0	1,108	0%
Total Number of 4 input LUTs	836	10,944	7%

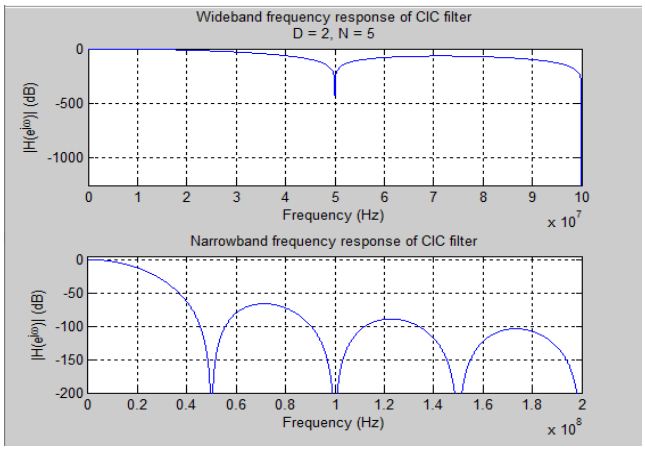


Fig (f) :wideband and narrow band CIC Filter

Note that the A FIR filter that has a magnitude response inverse of the CIC filter operates at low frequency (fS/*R)*. For single rate compensation filters to avoid aliasing, the cutoff frequency (fC) is, at most, half its output frequency: fC ≤(fS/*R)*/2. When the cutoff frequency is exactly (fS/*R)*/2, as the case shown in the compensation filter has an inverse sinc response across its entire bandwidth, thus it is also called a "wideband compensation filter"

In a multirate compensation filter, a decimation compensation filter with a rate change factor of 2 has input sampling rate fS/*R* and output sampling rate (fS/*R)*/2. To avoid aliasing, the compensation filter must have a cutoff frequency that is no more than half of (fS/*R)*/2, that is, (fS/*R)*/4.

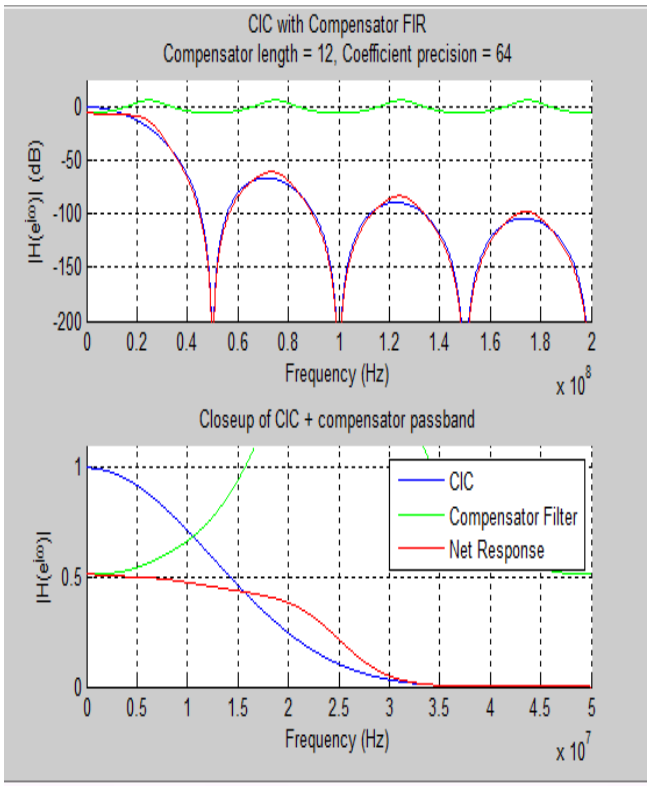


Fig (g) :CIC and Compensatator Filter

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The efficient modification in the frequency response of CIC compensation filter. The Compensation filter design consist of FIR filter as cascade after CIC filter. A FIR filter that has a magnitude response inverse of the CIC filter can be applied to achieve frequency response correction . As proposed filter has only sixty four coefficients so less computation is required. The decimation factor of the CIC filter is M. The performance of the compensation filter depends on the value of which is obtained by minimizing corresponding error function. Filter coefficient can control the desired pass band droop of the overall decimation filter. The resulting structure is multiplier less and exhibits small pass and droop in comparison to CIC filter.

VI.CONCLUSION

This paper present combined cic filter and application 64 taps using compesenator filter. Cic filter are used extensively multirate digital signal processing.compesente filter exactly achived by correctness of frequency response result in mat lab. Integrated cic filter resource utilization in FPGA.different rate change factor R, number stages increses N,delay D. The resulting structure is multiplier less and exhibits small pass band droop in comparison to CIC filter, Simulated result compare decimator and interpolator filter.

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