A Novel Test Path Selection Based on Switching Activity and Its BIST Implementation

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***Abstract*-This paper describes a longest test path selection based on gate delay and probabilistic approach by considering a path delay in a digital circuit. Various methods on longest test path selection are adopted such as longest transition path, segment coverage and heuristics. Preprocessing of Circuit Under Test (CUT) is done for reducing test time and to achieve low power consumption using BIST implementation. Accumulation of small delay defects on a path is identified by computing probability of particular path to meet the delay constraint. Thus the probability is estimated based on gate delay of each path in a digital circuit. Longest path selection approach is mainly chosen to trace out all the logical elements in the circuit. Delay occurs in the circuit due to various factors such as gate delay, interconnect delay, etc. In proposed method longest test path delay is selected from circuit switching activity which is caused mainly due to gate delay.**

***Index Terms*-path correlation, test path selection, BIST, upper and lower bound, path delay, probability.**

I INTRODUCTION

Process variation in CMOS technology causes various faults to occur in the VLSI circuits. These faults may be classified as struck at faults and delay faults. Various models have been designed to handle struck at faults. But the challenging criterion is to design a fault model for delay faults. Delay faults are classified as transition faults and path delay faults. Transition fault occurs due to unwanted transients in the circuit such as power supply variation and alpha-particle radiation. Path delay fault occurs due to delay defect in a particular path of a circuit. Transition fault model accounts for localized faults (delays) at the input and output of each gate. But path delay fault model takes the sum of all delays along a path into effect. There may be a case where the gate delays of individual faults are within specified limits, but the cumulative effect of all faults on a path may cause an incorrect value to be latched at the primary output, if the total delay exceed the functional clock period.

Path delay fault increases exponentially with respect to number of inputs in a circuit. So, all paths cannot be tested to find path delay fault, since it requires more testing time. Therefore, the critical path in the circuit is identified for testing the whole circuit to meet the delay constraint. Critical path is the longest path in the circuit.

Objectives of this work are to identify the longest path based on the number of transitions in each path from primary input to primary output. Also, the paths that have closer transitions to the longest path are also taken using segment coverage approach. Heuristics is applied to remove paths that no longer reach the primary output. These pre-processing are done in CUT and then implemented in BIST (Built-In-Self-Test).Testing is done in both normal mode and test mode and hence errors occurring during normal mode are estimated. Path delay faults are analyzed using probabilistic approach. Probability value shows that the delay of the circuit meets the specified clock period and that there is no delay failure in the particular paths. To do the pre-processing work, the number of paths in the circuit is identified by tracing from primary input to primary output. All paths reaching the primary output must be considered for testing.

This paper presents a novel BIST approach to find longest test path selection based only on gate delay transition and probabilistic approach by considering a path delay in a digital circuit.

The remaining part of the paper is organized as follows. Section II presents the previous work. Section III presents path selection strategy. Section IV presents proposed BIST architecture. Section V presents probabilistic analysis. The results are presented and discussed in Sections VI. Finally, conclusions are found in Section VII.

II PREVIOUS WORK

Statistical Static Timing Analysis (SSTA) technique is used to estimate the timing behavior of the circuit in order to capture small delay defects [1]. Also in [1] the probability is found by considering the gate and wire delays. In [2], the longest testable path in a circuit is selected by assuming the circuit as directed graph. In [3] the K longest paths are selected for testing. It is assumed that the circuit does not contain only one longest path. Such path selection leads to effective testing for timing analysis. In [4] the false paths in the circuit re eliminated from path list in order to reduce the unwanted testing process. False paths are the paths that cannot be sensitized under any input vector and hence including false path in circuit timing calculation may lead to unrealistic results. In [5] the probability is computed using the mean and standard deviations of path delays. Normal distribution is used

for computing the probability value by considering the circuit delay as an area. Various conditions for computing joint probability distributions are provided in [5].

In [6] the statistical timing analysis is performed to calculate the circuit timing behavior by considering spatial correlations into account. Finding the delay distribution of one critical path at a time is not enough. So, spatial correlation between the paths are taken into account to find the maximum if path delay faults and so as to compute the probability of delay failures. In [7] the propagation time of each delay path is computed and the clock period is set to 110% of the longest delay path in the circuit. In [8] the lower bound on number of tests is performed in order to locate delay faults in combinational circuits. Two pattern tests are applied and the number of rising and falling transitions is computed based on the type of gates. In [9] and [10] the BIST implementation for the delay fault testing is done to ensure the correct working of circuit in functional mode. In [11] the longest path is selected based upon the maximum delay among all the paths. In this paper the modes in the circuit are controlled by separate pin and the implementation is done successfully.

III PATH SELECTION STRATEGY

A path is said to be testable if the rising/falling transitions in a path can propagate from the primary input to the primary output associated with the particular path. To check the transitions along the path the two pattern tests are applied using scan based test vector generation. Two pattern test contains two vectors $\{V_1,V2\}$ in which the V_1 vector initializes the circuit and V_2 vector allows the input to propagate to the primary output. On applying the two pattern test into the circuit, the numbers of rising and falling transitions are found on each path [8]. The Fig.1.shows the flow chart to compute the number of rising and falling transitions from primary input to primary output.

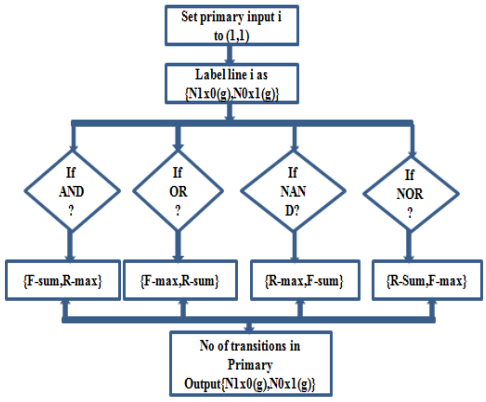

Fig.1.Flow chart to compute transitions in circuit.

Initially all the inputs are set to have one rising and one falling transitions. The label $N_{1X0}(g)$ represents the number of falling transitions and $N_{0X1}(g)$ represents the number of rising transitions of the particular gate. Then depending upon the type of gate the numbers of transitions are computed.

A. Longest transition Path

The top longest path is found by counting the number of transitions occurring in each path of the circuit. The paths from primary input to primary output are alone considered for testing. First, all paths are traced out and then the longest transition path is identified by applying the two pattern test to the CUT(Circuit Under Test).The upper and lower bond on number of transitions are computed in each path to find the longest transition path.

B. Segment Coverage

Segment coverage is done to cover certain paths that reach the primary output with lesser transitions compared to longest transition path. There are several paths to reach the same primary output. Using this segment coverage procedure, only certain paths are selected in the basis of number of transitions that are closer to the longest path transitions. Doing so, will add some paths that are to be tested to ensure testing in an efficient manner.

TABLE I

PATHS IN S298 BENCHMARK FROM PI TO PO.

PATH NAME	PATH TRACE FROM PI TO PO
P11	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g96 - g89 - g86 - g16 - i155 - g66
P12	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g88 - g86 - g16 - I155 - g66
P21	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g96 - g95 - g92 - g17 - I158 - g67
P22	g0- i229 - g130 - g28 - g27 - g53 - g44 - g14 - g96 - g83 - g97 - g92 - g17 - i158 - g67
P23	g0- i229 - g130 - g28 - g27 - g53 - g44 - g14 - g96 - g85 - g97 - g92 - g17 - i158 - g67
P24	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g84 - g97 - g92 - g17 - I158 - g67
P31	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g96 - g68 - g101 - g98 - g18 - I210 - g117
P32	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g100 - g98 - g18 - I210 - g117
P33	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g70 - g101 - g98 - g18 - I210 - g117
P41	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g96 - g77 - g106 - g102 - g19 - I213 - g118
P42	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g74 - g104 - g105 - g102 - g19 - I213 - g118
P43	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g75 - g104 - g105 - g102 - g19 - I213 - g118
P44	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g61 - g57 - g56 - g15 - g64 - g63 - g112 - g108 - g105 - g102 - g19 - I213 - g118
P51	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g109 - g110 - g107 - g20 - i235 - g132
P61	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g115 - g113 - g21 - T238 - g133
No path	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g115 - g113 - g21 - g114 - g115
No path	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g79 - g116 - g113 - g21 - g114 - g115
No path	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g80 - g116 - g113 - g21 - g114 - g115
No path	g0 - i229 - g130 - g28 - g27 - g53 - g44 - g14 - g50 - g26 - g53 - g44 - g14
No path	g0 - i229 - g130 - g28 - g43 - g39 - g13 - g40 - g42 - g39 - g13

C. Heuristics

Three heuristics approach are made to refine the path selection. First, the path that cannot be the longest one at any cost is deleted from the path list. Second, the paths that are same as the longest path are removed from the path list. Third,

when two paths reaching same primary output, the path with higher transition is selected.

Table I shows the number of paths from primary input to primary output in s298 benchmark circuit. Table II shows the selected path for testing based on the path selection strategy mentioned in section III. This is the process done in prior on the CUT.

TABLE II

SELECTED PATHS BASED ON PATH SELECTION STRATEGY

PATH SELECTION STRATEGY	PATHS
TOP LONGEST	P44
SEGMENT COVERAGE	P11,P22,P31,P44,P51,P61
HEURISTICS	No path(removed)

In the Table I, the paths P11 and P12 reach the same primary output. Now based on the maximum number of transitions, anyone path is deleted and only one path to each the certain primary output is selected for testing.

In the Table II, it is shown that the longest path in selected first and then the segment coverage and heuristics are approached. This helps in removing the unwanted paths to be tested and to ensure low testing time. This pre-processed circuit is taken as a CUT in BIST implementation.

IV PROPOSED BIST ARCHITECTURE

Built-In-Self-Test in the on chip testing circuitry that minimizes the hardware overhead. The proposed BIST architecture is made to function in two modes namely normal mode and test mode. As mentioned in previous section, the CUT is the pre-processed one. During the test mode, the circuit is tested with all possible vectors and it is memorized. Then, during the normal mode the test vectors are applied and the circuit now operates in at-speed functional clock period. So, the stored test mode responses are used to compare the results of test mode and normal mode. The fault injection is done in CUT during the normal mode of operation.

The basic BIST architecture consists of a BIST controller, CUT, response analyzer and an error counter. In this paper the CUT itself is made with changes to have lower testing time and to ensure low testing power consumption. Fig.2.shows the architecture of BIST controller. The output response on test mode is stored in BIST controller when the output of CUT is DEMUXed. Then change the mode to normal mode.

The online input is applied in at-speed to the CUT. Now the output of the CUT is DEMUXed to the response analyzer and at the same time the BIST controller reads the stored response to the response analyzer. The two output responses of CUT are compared and the number of errors identified. This should be done with minimum test vectors. In this paper the errors are identified by applying 20 vectors to the s298 benchmark circuit.

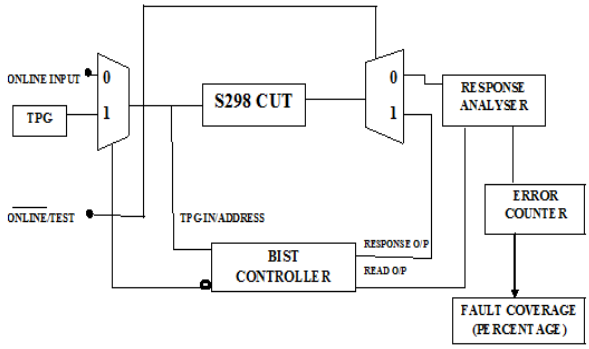

Fig.2. Proposed BIST architecture

V PROBABILISTIC ANALYSIS

The BIST architecture proposed in section IV deals with the errors occurring due to stuck-at faults in the circuit. But, due to process variation, there is a chance for a circuit where the path delay may exceed the functional clock period. So, testing should ensure that the delay of the circuit does not exceed the clock period and hence the path delay can be found. To find the path delay, the delay of each gate in the circuit should be calculated based on the logical effort of gate.

A. Gate Delay Computation

Gate delay is computed using the standard formula that contains logical effort, parasitic delay and non ideal delay. The input capacitance of each gate is computed by backtracking the circuit from primary output. The Fig.3. shows the c17 benchmark in which the gate input capacitance is found based on the load capacitance.

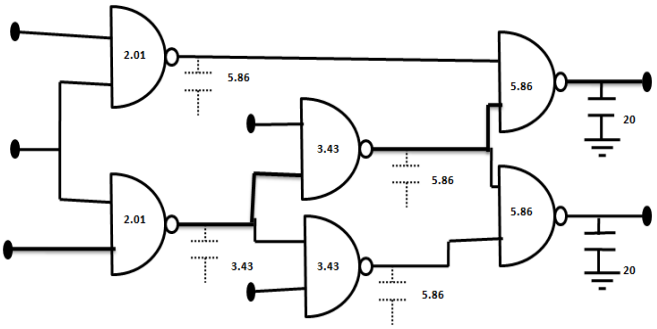

Fig.3.c17 benchmark with capacitance value

The capacitances are found as illustrated in Fig.3. by assuming the load capacitance as 20 units. Based on the capacitance value the gate delay is computed using the standard formula d=f+p+q, where f is the product of logical effort and electrical effort, p is the parasitic delay of the particular gate and q is the non-ideal delay. This delay represents the delay of individual gate.

B. Probability of Delay Failures

The probability of delay failure is estimated based on the mean delay of each path in circuit and the standard deviation from mean. Mean delay is the average of all gate delay in the particular path. Standard deviation is the deviated value from the mean value. Using these values the normal area is found by formula given in equation (1).

$$Z = \frac{x-\mu}{\sigma} \quad (1)$$

After computing the Z value, the probability is found for each and every path individually using the normal distribution table. The probability thus computed is only for single path to meet the delay constraint. If the probability value is more, there is a more chance for that path to meet the specified clock period without any delay. The delay probability is denotes as $d_1(p_1), d_1(p_2), \ldots . d_n(p_n)$, where n is the number of paths in the circuit selected for testing.

C. Probability of two paths

The probabilities for two paths are found by taking the joint probability distribution for the two random variables. In [5] it is stated that if two paths are normally distributed, then the mean and variance of the two paths are computed as given in equation (2) and (3).

$$Mean\ (Z) = Mean(X) + Mean(Y) \quad (2)$$

$$Var\ (Z) = Var(X) + Var(Y) + 2cov(X, Y) \quad (3)$$

Where *var (Z)* is the variance of the random variable Z that is obtained from the two variances X and Y and *cov(X, Y)* is the covariance of the two random variable X and Y. Using this mean and variance the joint probability for the two paths are calculated. The probability is denoted as $d_2(p_1p_2), d_2(p_1p_3)$,etc.

D. Probability of three paths

To compute probability of three paths mathematically, will require more time complexity. Hence the probability is computed based on the obtained values of Section V.B and V. C. This reduces time complexity. The equation (4) gives the formula for computing upper and lower bound of probability.

$$\begin{aligned}&\mathrm{Max}(d_2(p_1p_2)+d_2(p_1p_3)-d_1(p_1), d_2(p_1p_2)+d_2(p_2p_3)-\\ &d_1(p_2), d_2(p_1p_3)+d_2(p_2p_3)-d_1(p_3)) \le d_3(p_1p_2p_3) \le\\ &\mathrm{Min}(d_2(p_1p_2), d_2(p_1p_3), d_2(p_2p_3))\end{aligned} \quad (4)$$

The maximum value gives the upper bound and the minimum value gives the lower bound. The probability is estimated by taking the average between the upper and lower bound values. The probability computed, thus considers path correlation into account. So, joint probability is computed by taking the values of probabilities of each and every path that meets the delay constraints.

D. Probability of more than 3 paths

For more than three paths the probability computation will be more complex while considering path correlation into account. So, path abstraction is done to make the computation easier. It is done by making several paths in a circuit to be viewed as three paths and the probability computation for three Paths are applied as stated in section V.D. The probability of more paths to meet the delay constraint is computed using already computed values for single, dual and three paths.Fig.5. shows the path abstraction procedure [5] to reduce 4 paths to three paths.

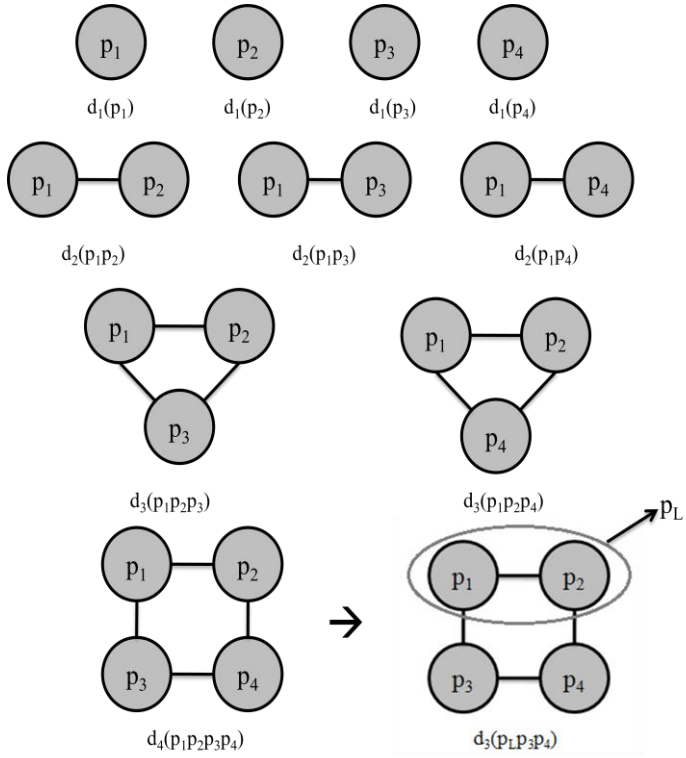

Fig.4.Path abstraction for four paths

In Fig 4. the probability for four paths is illustrated. By grouping method maximum number of paths are reduced as a single path as mentioned in section V.D.

In order to reduce time complexity of the circuit joint probability computation is adapted. Probability value determines the path delay of the circuit. Higher probability achieves reduced path delay.

VI RESULT ANALYSIS

The proposed technique is experimentally done in ModelSim simulator and the testing time and power are analyzed in Altera QuartusII 10.0. The computation probability is obtained through MATLAB software. It is proved that the proposed method with path selection has less testing time and less power consumption compared to the circuit without path selection method.

Table V, VI, VII and VIII represents the computed value for the path delay considering only the gate delay and the input test vector. The switching activity of each path is added to the mean delay of the path.

A. Simulation Results

The Fig.5 and 6 represents the simulation output with two modes of a BIST circuitry namely test mode and normal mode. It is shown that the number of faults occurred in the s298 benchmark circuit is reduced only by applying 20 test vectors using LFSR which generates 100 test vectors with different seeds. It is shown in Fig.7. Table IV shows the testing time and power for the s298 ISCAS'89 benchmark circuit with and without path selection approach. Fig.8. shows the graph of signature analyzer that represents the number of faults occurred before and after the path selection approach. High fault coverage of 66% is obtained for the input test vector 010 and it is shown in Table III.

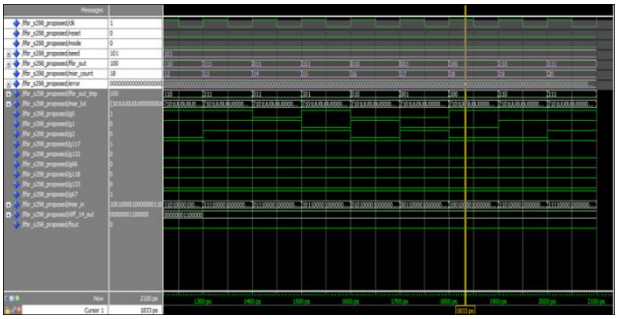

Fig.5.Operation of mode 0(Test Mode)

TABLE III

FAULT COVERAGE FOR VARIOUS LFSR SEED

LFSR Seed	Fault Coverage (%)
001	50
010	66
011	50
100	18
101	15
110	18
111	18

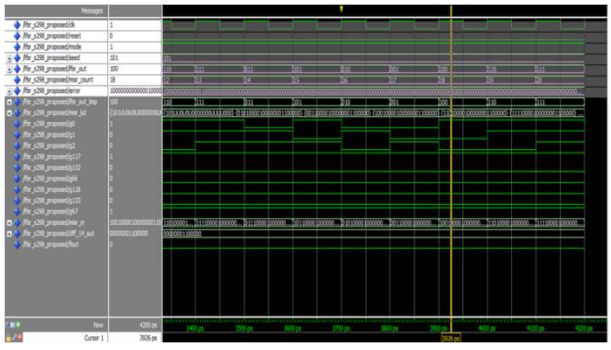

Fig.6.Operation of mode 1(Normal Mode)

TABLE IV

COMPARISON OF TEST TIME AND POWER

CIRCUIT	TEST TIME	POWER
S298 without Path Selection	7.847ns	41.29mW
S298 with Path Selection	6.582ns	29.68mW

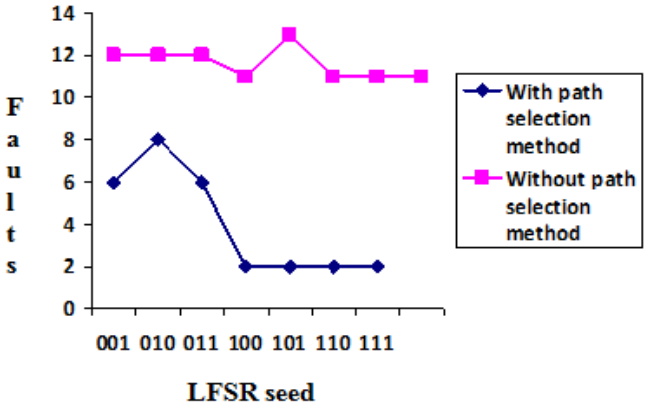

Fig.7.Comparison of faults with LFSR seeds of s298 benchmark circuit

TABLE V

PROBABILITY FOR ONE PATH

PATH	MEAN DELAY	S.D	VARIANCE	NORMAL REGION (Z)	PROBABILITY	CLOCK
P1	9.615	0.473	0.223	2.019	0.477	9.615*(110/100) =10.57
P2	8.434	1.312	1.721	1.628	0.447	
P3	8.434	1.312	1.721	1.628	0.447	
P4	8.434	1.312	1.721	1.628	0.447	
P5	8.813	1.607	2.582	1.093	0.362	
P6	8.813	1.607	2.582	1.093	0.362	
P7	8.813	1.607	2.582	1.093	0.362	

TABLE VI

PROBABILITY FOR TWO PATHS

PATH	MEAN	S.D	CO-VARIANCE	PROBABILITY
P1P2	18.049	1.880	0.769	0.449
P1P3	18.428	2.200	1.081	0.390
P2P3	17.247	2.926	2.130	0.408
P1P4	18.049	1.880	0.796	0.449
P2P4	16.868	2.623	1.721	0.447
P4P5	17.247	2.536	2.130	0.436
P5P6	17.626	3.213	2.582	0.362
P6P7	17.626	3.213	2.582	0.362

TABLE VII

PROBABILITY FOR THREE PATHS

Path	Probability
P1P2P3	0.4
P1P2P4	0.449

TABLE VIII

PROBABILITY FOR MORE THAN THREE PATHS

Path	Probability
P1P2P3P4	0.424
P1P2P3P5	0.424
P1P2P3P4P5	0.461
P1P2P3P4P5P6	0.411
P1P2P3P4P5P6P7	0.461

VII CONCLUSION

The proposed technique provides effective path selection based on the switching activity of the circuit path. The BIST circuitry approach in longest test path selection consumes less testing time, high fault coverage and low power for testing the circuit. Path selection based on probability is used to calculate the path delay. The probability of n path meeting the delay constraint is also calculated. Thus, the longest path delay is computed by considering the switching activity of each path.

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