Parametric Analysis and Comparison of Various SRAM Topologies

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***Abstract* - The current fad of reducing the chip area and optimizing power dissipations of SRAM cells has led to rapid MOSFET channel length scaling down. But stability remains a factor to be considered. Optimizing parameters like Static Noise margin, Read Margin, Write Margin are paramount to obtain desirable characteristics of SRAM cells. This paper presents the parametric analysis of different configurations of SRAM memory cells such as – 6T, 7T, 8T, 9T and 10T. The parameters analyzed are Static Noise Margin (SNM), Write Margin, Read Margin and Data Retention Voltage (DRV). The analysis is done using Tanner EDA Tool on 250nm technology at a supply voltage of 5.0 volts.**

***Index terms*- Cell Ratio, DRV, Pull-up Ratio, Read Margin, SRAM Topologies, 6T, 7T, 8T, 9T, 10T, SNM, DRV, Write Margin.**

I. INTRODUCTION

Presently SRAM cells are widely being used in cache memories because of their high speed and volatile performance. SRAMs provide us a greater efficiency to store and retrieve information within fraction of seconds. With unrelenting technology scaling, stability and noise margin of SRAM are substantially affected. Application specific designing of SRAM cells require parameter optimization of different SRAM topologies. This is achieved by manipulating the cell ratio and pull up ratio, as these are the only design parameters in the hands of the designers.

Section 2 discusses the parametric analysis of different SRAM topologies followed by the comparative study in section 3 and lastly paper presents the derived conclusions.

II. PARAMETERS UNDER STUDY

As a designer the only parameters which can be varied are cell ratio and pull-up ratio which correspondingly affects static noise margin and stability of the SRAM circuits.

A. Cell Ratio (CR)

The cell ratio (CR) is defined as the W/L ratio of driver transistor to access transistor during the read operation as shown in Fig.1. CR= (W1/L1)/ (W5/L5) (during read operation). If cell ratio is changed then corresponding size of the transistor also increases and, hence, current also increases.

B. Pull-up Ratio (PR)

The pull up ratio can also be defined as the W/L ratio of load transistor to access transistor during the write operation as shown in fig a. PR= (W4/L4)/ (W6/L6) (during write operation).

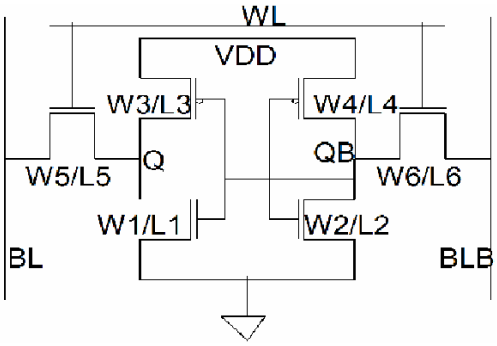

Fig. a Basic 6T Cell

C. Write Margin

Write margin is the minimum noise that a circuit can tolerate during the write operation. Or it can describe as the minimum bit line voltage required to flip the state of any SRAM cell. Write margin is calculated by sweeping the BL and BLB analysis as shown in Fig. b. The value of write margin can vary up to below or equal to 1.5.

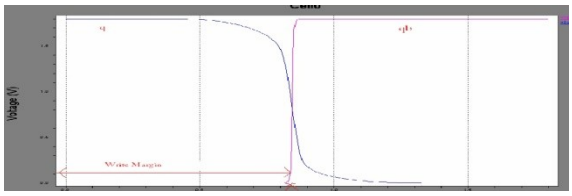

Fig. b Curve Showing Write Margin of a Cell

D. Read Margin and Static Noise Margin

The SRAM read stability is also a function of transistor's threshold voltage and power supply voltage variations. It is directly proportional to cell ratio. The static noise margin can be described as the minimum noise that a circuit can tolerate. We have used the conventional butterfly curve method to obtain the read margin and corresponding static noise margin. The process of measuring the read margin is same as the noise margin as shown in Fig. c.

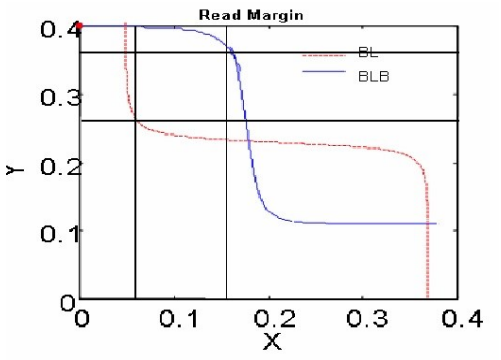

Fig c Curve Depicting Read Margin of Cell

E. Data Retention Voltage

Data retention voltage may be defined as the lowest power supply voltage which is required to retain the data inside the SRAM cell. In SRAM cells, the cross-coupled inverters have a positive feedback which may be weakened because of low supply voltages and thus the SRAM cell will spuriously flip states. For obtaining the Data retention voltage, the value of V_{DD} is varied from 5.0volts to 0.5volts until and unless the voltage curve degrades to such a level that static noise margin of SRAM reduces to approximately zero.

III. COMPARATIVE STUDY

A. SRAM Topologies

A. 6T SRAM Cell

The basic 6T cell consists of two cross-coupled inverter and two NMOS access transistors connected at word line (WL) by their gate terminals and bit lines at their source/drain terminals, respectively. Using word line a cell can be selected and bit lines are used for read and write operations as shown in Fig. d.

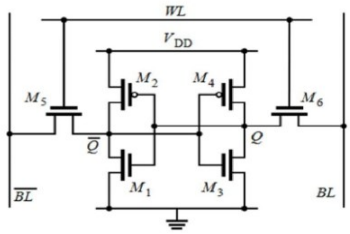

Fig. d Basic 6T Cell

B. 7T SRAM Cell

The working of 7T SRAM is much similar to the 6T cell. It has same read and write signals but has one extra NMOS transistor acting as a control transistor NMOS-5 for read-disturb free operation Fig. e.

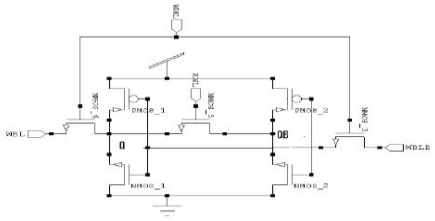

Fig. e 7T SRAM Cell

C. 8T SRAM Cell

8T cell was proposed to overcome the disadvantage of 6T cell in which also separate read/write bit lines and word lines are used which ultimately separates the data retention voltage and output element Fig. f.

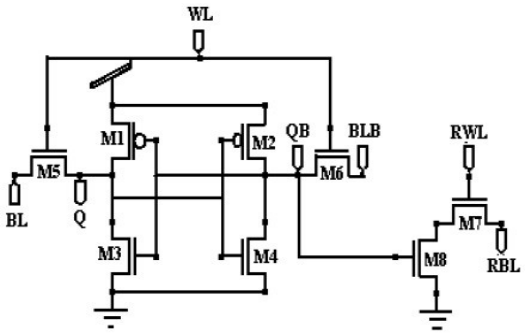

Fig. f. 8T SRAM Cell

D. 9T SRAM Cell

The 9T SRAM cell is used to achieve enhanced data stability by completely isolating the data from the bit lines during the read operation as shown in Fig. g.

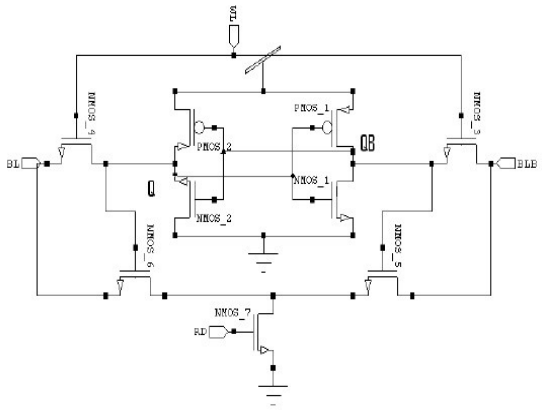

Fig. g 9T SRAM Cell

E. *10T SRAM Cell*

The dual port 10T SRAM cells is shown in Fig. h in which it has only one read or write can occur per cycle due to which it can perform in threshold region.

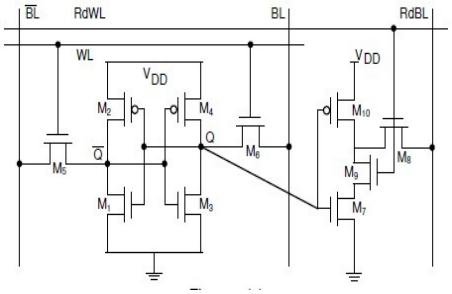

Fig. h 10T SRAM Cell

B. Parametric Analysis

A. *Write Margin*

Table 1: Analysis of Write Margin of Different SRAM Cell

PR	6T SRAM	7T SRAM	8T SRAM	9T SRAM	10T SRAM
2.8	0.428	0.382	0.689	0.750	0.550
3.0	0.431	0.432	0.689	0.753	0.556
3.2	0.435	0.432	0.690	0.768	0.580
3.4	0.437	0.440	0.705	0.780	0.580
3.6	0.439	0.480	0.710	0.785	0.590
3.8	0.439	0.482	0.721	0.790	0.591

A. Read Margin

Table 2: Analysis of Read Margin of SRAM Topologies

CR	6T SRAM (Volts)		7T SRAM (Volts)		8TSRAM (Volts)		9T SRAM Volts)		10T SRAM (Volts)	
	RNM	SNM	RNM	SNM	RNM	SNM	RNM	SNM	RNM	SNM
1.0	1.05	1.48	1.20	1.69	1.85	2.61	1.65	2.33	1.90	2.68
1.2	1.05	1.48	1.20	1.69	1.85	2.61	1.70	2.40	1.90	2.68
1.4	1.08	1.52	1.23	1.73	2.0	2.83	1.70	2.40	1.90	2.68
1.6	1.10	1.55	1.23	1.73	2.0	2.83	1.72	2.43	2.05	2.89
1.8	1.10	1.55	1.26	1.78	2.0	2.83	1.82	2.57	2.05	2.89
2.0	1.11	1.56	1.26	1.78	2.05	2.89	2.05	2.89	2.10	2.96
2.2	1.12	1.58	1.26	1.78	2.05	2.89	2.10	2.96	2.15	3.05

B. Data Retention voltage

Table 3: Analysis of Data Retention of Various Cell

SRAM Topology	DRV (volts)
6T	0.4
7T	1.2
8T	1.5
9T	0.56
10T	1.8

IV. CONCULSION

The write noise margin of conventional 6T SRAM, 7T SRAM, 8T SRAM don't show substantial variations. The 10T SRAM has WNM lying within 6T and 8T WNM values. However, the WNM of 9T SRAM shows sufficient increase.

The read SNM value of 6T SRAM cell is less due to which judicious trade-offs between RNM and cell area is not possible. The 8T and 10T SRAMs provide higher RNM due to the two read buffer being used. The RNM for 9T SRAM cell is also high.

Thus, it can be concluded that 6T SRAM is robust, can be easily implemented and has least chip area. The 8T cell provides for better read operation but chances of write operation failure do exist. The 10T SRAM implements read buffers and can be used for the same. The 9T SRAM configuration, with a high RNM and WNM, shows better stability compared to the remaining configurations.

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