Efficient Design of Arithmetic Logic Unit using Reversible Logic Gates

Ravi Raj Singh, Sapna Upadhyay, Saranya S, Soumya, Jagannath KB, Hariprasad SA

Abstract— **Reversible logic is gaining wide importance as a logic design style for modern nanotechnology and quantum computing with minimal heat generation because the existing irreversible designs are reaching their physical limits. The reversible approach, therefore, results in improved computer architecture and arithmetic logic unit designs. An important block in the microprocessors is Arithmetic and Logic Unit (ALU). This paper proposes the design of ALU which have better performance in terms of quantum cost and transistor cost. The proposed ALU is realized using a carry save adder block which does not involve the propagation of carry bits. The proposed work leads to an improvement of 20% and 17% in terms of gate count and quantum cost respectively, as compared to earlier works in reversible ALU designs. The simulation and verification of the ALU is done using Cadence, Xilinx and Revkit tools.**

Index Terms— **ALU, Adder, Reversible Logic, Quantum Cost, Transistor Cost.**

I. INTRODUCTION

Since the demand for more compact system designs with portability and higher speed is increasing, the need for improving the capabilities of these entities has been a major research area for example, in hand held devices. These devices must also operate at low power levels. Landauer proved that using irreversible logic gates always lead to energy dissipation regardless of the underlying technology. Exactly, $k \cdot T \cdot \ln 2$ Joule of energy is dissipated for each "lost" bit of information during the irreversible operation(where $k=1.38*10^{-23} JK^{-1}$ is the Boltzmann constant and T is the temperature in Kelvin)[1].C. H. Bennett showed that energy dissipation problem can be avoided if circuits are built using reversible logic gates [2]. For this to be true, the circuit should be both physically and logically reversible. Practically, there will be power dissipation less than the K.T.ln2 limit in CMOS irreversible circuits. A gate realizing a certain reversible logic function is called a reversible logic gate. A circuit made by concatenating these gates is called a reversible logic circuit. An irreversible logic gate can also be expressed in terms of reversible gates and such circuits can be synthesized with minimum energy consumption or zero entropy gain [3].Due to the one to one mapping between input and output, the power dissipation in the reversible circuits is minimum. Thus, reversible designs are gaining wide importance in the fields of quantum computing, nano technology, low power CMOS design and other advanced applications. The goals of reversible logic design are mainly to minimize the quantum cost, delay as well as the ancillary inputs and garbage outputs [4].

From the above discussion it is clear that reversible logic is the upcoming field in low power technology. The reversible logic is, therefore, being used for the design of the ALUs. The following work has been done in design of the reversible ALU:

A. Rao N.S. et.al

They have proposed 1-bit ALU utilizing P-gate and Fredkin gate in 2012 [5].The gate count, transistor cost and quantum cost was found to be 11,120 and 31 respectively.

B. Vinod Kapse et.al

They have also proposed a 1-bit ALU utilizing a reversible control unit and a D-Peres gate in 2012[6]. The gate count, quantum cost was found to be 10 and 29 respectively.

C. Zhijin Guan et.al

They have proposed 1-bit ALU in which gate count and quantum cost was found to be 10 and 29 respectively in 2011. [7].

In this paper, we propose the implementation of an Arithmetic and Logic Unit in which the inputs have been adjusted to satisfy reversibility. We have found that the gate count, transistor cost and quantum cost can further be reduced by design of ALU that we have proposed in this paper.

The paper is organized as follows: Section II deals with the necessity of this domain, section III deals with the concept involved in reversible logic, section IV introduces the basic fundamentals of reversible logic, section V deals with the basic reversible gates, section VI deals with related work followed by proposed work in section VII and finally conclusion and future work in section VIII.

II. NEED FOR REVERSIBLE COMPUTING

Since, the present technologies are reaching their limits in terms of power and area, a new paradigm is needed. Reversible computing provides low power design and

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***Ravi Raj Singh**, ECE Department, BMS Institute of Technology, Bangalore, India,*
***Sapna Upadhyay**, ECE Department, BMS Institute of Technology, Bangalore, India,*
***Saranya S**, ECE Department, BMS Institute of Technology, Bangalore, India,*
***Soumya**, ECE Department, BMS Institute of Technology, Bangalore, India,*
***Jaganath KB**, ECE Department, BMS Institute of Technology, Bangalore, India,*
***Dr. Hariprasad SA**, ECE Department, BMS Institute of Technology, Bangalore, India,*

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improves the performance of the system. It increases portability of the device by reducing the element size to atomic size. It is an emerging trend in nanotechnology and QCA domain. This clearly shows that the reversible logic is future in VLSI.

III. The Concept

The basic principle of reversible computing is that a bijective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the probability that the particle of system reaches every possible state is the same, resulting in no heat dissipation. Reversibility simply implies that information about computational states is not being lost. [8]

Thus, reversibility can be explained by the basic idea of one to one mapping between the input and output where the number of input is equal to the number of output for the system. A reversible circuit with n inputs and outputs is known as n*n reversible circuit. A reversible circuit is composed of reversible gates.

IV. Reversible Logic Fundamentals

A. Definition I

The multiple output Boolean function $f(x1, x2\ldots\ldots,xn)$ of n Boolean variables is called reversible if:

1. The number of outputs is equal to the number of inputs;
2. Every output pattern has a unique pre-image.

Thus, reversible functions are those that perform permutations of the set of input vectors [9].

B. Definition II

Garbage outputs are the number of outputs added to make an n-input k-output function ((n, k) function) reversible.

C. Definition III

A constant input denotes the fixed valued inputs that were added to an (n, k) function to make it reversible.

The following is the formula that shows the relation between the number of garbage outputs and constant inputs:

$$\text{Input} + \text{constant input} = \text{output} + \text{garbage} \quad (1)$$

D. Definition IV

The Quantum cost denotes the effort needed to transform a reversible circuit to a quantum circuit and is calculated by counting the number of V, V+ and CNOT gates [10]. Some of the basic reversible gates are Feynman gate, Toffoli gate, Peres gate, Fredkin gate.

V. Reversible Logic Gates

A. Feynman Gate

It is a 2*2 reversible gate as shown in fig 1. The input vector is I(A,B) and the output vector is O(P,Q). The outputs are defined by P=A, Q=A B. Quantum cost of Feynman gate is 1. It is used as a copy gate in duplication of required outputs in sequential circuits.

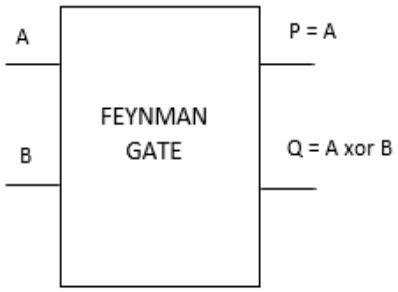

Fig 1: Feynman Gate

B. Toffoli Gate

It is 3*3 reversible gate as shown in fig 2. The outputs of P and Q are directly generated from inputs A and B respectively. The quantum cost of this gate is 5.

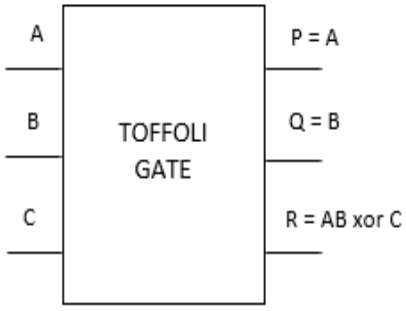

Fig 2: Toffoli Gate

C. Peres Gate

It is a 3*3 reversible gate as shown in fig 3. The output P is same as A. The quantum cost of Peres gate is 4 since it requires 2 controlled-V+ gates, 1 controlled-V gate and 1 CNOT gate in its design.

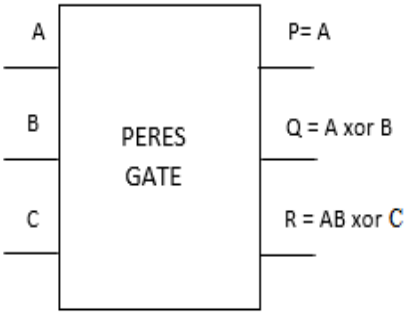

Fig 3: Peres Gate

D. Fredkin Gate

It is a 3*3 reversible gate. The input vector is I(A,B,C) and the output vector is O(P,Q,R). The quantum cost of this gate is 5.

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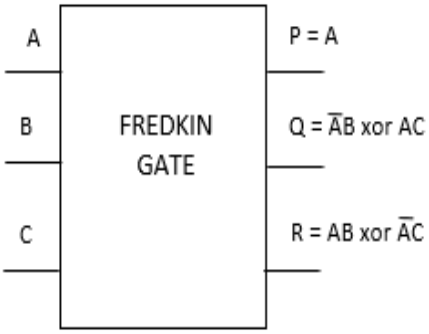

Fig 4: Fredkin Gate

VI. Proposed Work

The proposed 1-bit ALU is designed using adder block, Toffoli gate, Fredkin gate, Cnot gate and Not gate. There are multiple techniques to perform addition operation such as carry save, carry skip, ripple carry, carry look ahead etc. In this approach carry save technique [11] is applied. In order to make a reversible carry save adder there is a need to add another output line. But adding one bit cannot distinguish among 3 values. Therefore, two bits have to be added, which indicates addition of two output lines making the carry save adder a 4x4 reversible gate.

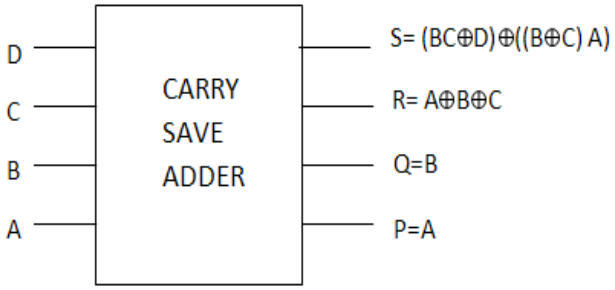

Fig. 5. Carry Save Adder Block

This carry save adder is comparatively lower in quantum cost and number of gates. This adder can be used to design an ALU with lower quantum cost, constant inputs and garbage output. The fig 6 and fig 7 is the block diagram and quantum circuit of proposed 1-bit ALU, respectively.

The design of 1-bit ALU is verified and simulated using Verilog in Xilinx as shown in fig 8. The quantum cost, transistor cost, line count, garbage output and constant inputs are calculated in Revkit -1.2.1, as shown in Table II. After synthesis of above design in Cadence, the power dissipation in proposed ALU is found to be 2950.833 nW, The two input lines are constant and given logic 0 as input (fig 6). The variable 'c' acts as an input as well as control and variable 'ctrl' is utilized as a control line. The various functions the proposed ALU performs are shown in Table I.

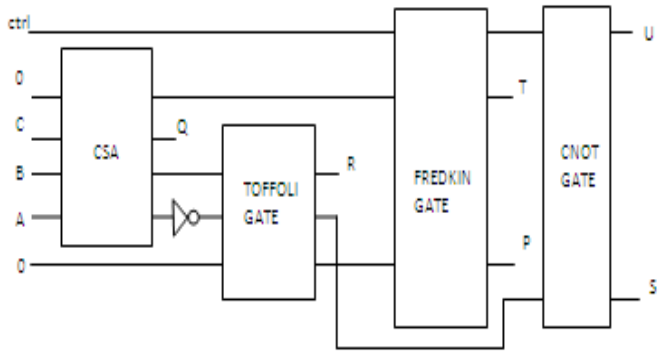

Fig. 6. ALU Block Diagram

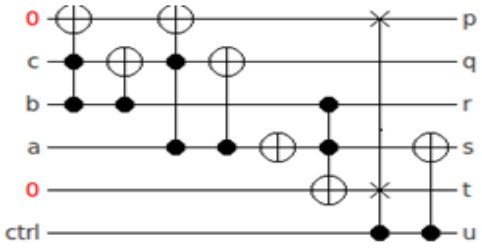

Fig 7: Quantum circuit of ALU

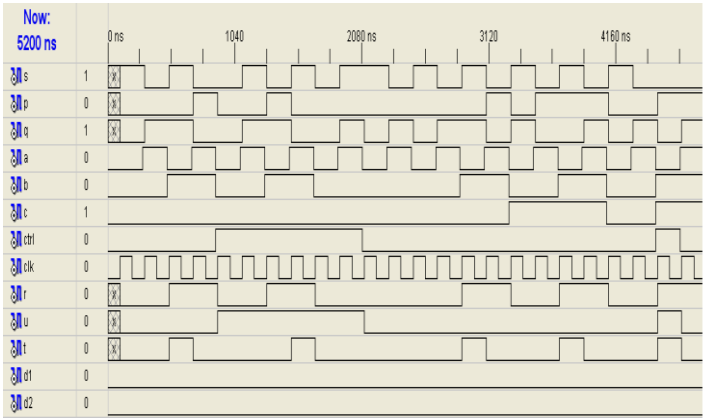

Fig. 8. ALU Simulation

TABLE I. ALU Operations

Arithmetic Operations				
C	Cntrl	P	Q	S
0	0	Carry	Sum	X
0	1	Borrow	Difference	X
X	1	-	-	Buffer
X	0	-	-	Complement
Logical Operations				
0	0	A and B	A xor B	-
1	0	A or B	A xnor B	-

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TABLE II. COMPARISON RESULTS

	Proposed Improve-ment w.r.t [7]	Existing [5]	Existing [6]	Existing [7]
Gate Count	8 [20%]	11	22	10
Quantum Cost	24 [17%]	31	53	29
Transistor Cost	80	120	-	-
Garbage Output	1 [87.5%]	2	12	8
Constant Input	2 [50%]	1	10	4
Line Count	6	5	-	-

VII. CONCLUSION AND FUTURE WORK

The reversible logic is an upcoming area for low power circuit design. Therefore, Reversibility finds applications in various emerging fields like quantum computing, quantum cellular automata, DNA computing, optical computing, and cryptography.

In this paper, we have proposed a novel design of an ALU with the use of a full adder. The adder circuit in the proposed work is more effectively utilized than previous literature works. Thus, it can be clearly seen that there is a considerable improvement in the quantum cost (17%) and gate count (20 %) compared to the previous works. However, this improvement is achieved at the cost of an extra line count. But there is a scope for further realization of higher bit ALU using more efficient adder blocks.

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Ravi Raj Singh Currently pursuing B.E in the stream of Electronics and Communication Engineering at BMS Institute of Technology, Bangalore, India. The areas of research that interests him are low power design based on reversible logic. He is working on development of low power reversible sequential circuits.

Sapna Upadhyay is an undergraduate B.E. scholar in Electronics and communication Engineering Department, BMS Institute of Technology, Bangalore, India. The low power VLSI and Embedded designs are her areas of interest. Her current work is in efficient design of low power reversible circuits.

Saranya S is a final year B.E student in Department of ECE, BMS Institute of Technology, Bangalore, India. Her areas of interest are VLSI, Embedded designs and Signal processing. Her current research is in the field of low power reversible logic designs.

Soumya is final year B.E student in Electronics and Communication stream of B.M.S Institute of Technology, Bangalore, India. Her research interests are in Low Power VLSI Design. She is currently carrying out work in reversible logic circuits design.

Jagannath KB Received the BE degree from Sapthagiri college of engineering, Bangalore, Karnataka and M-tech from NIT Calicut, Kerala, India. He is Assistant professor in department of ECE, BMS Institute of Technology, Bangalore, India. He has published papers in various national, international conferences and journals. His research interests are in reversible logic and QCA.

Dr. Hariprasad SA received B.E in Electronics and Communication Engineering from Mysore University, Mysore, India and M.E in ECE from Bangalore University, B.M.S college of Engineering, Bangalore. He has received Phd in ECE from Avinashilingam University for Women, Coimbatore, India in the year 2011 and D.Sc in ECE from Tumkur University, Tumkur, India in the year 2013 for the thesis titled "Performance Analysis of Viterbi Decoders".He is a Vice-Principal and HOD of ECE department in BMS Institute of Technology, Bangalore, India. He has published papers in various national, international conferences and journals. His research interests are in the area of embedded system and microwave systems.

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